AN-288 System-Oriented DC-DC Conversion Techniques

ABSTRACT

This application note discusses the operation of system-oriented DC-DC conversion techniques.

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1 Introduction

In many electronic systems, the need arises to generate small amounts of power at voltages other than the main supply voltage. This is especially the case in digital systems where a relatively small amount of analog circuitry must be powered. A number of manufacturers have addressed this requirement by offering modular DC-DC converters which are PC mountable, offer good efficiency and are available in a variety of input and output voltage ranges. These units are widely applied and, in general, are well engineered for most applications. The sole problem with these devices is noise, in the form of high frequency switching spikes which appear on the output lines. To understand why these spikes occur, it is necessary to examine the operation of a converter.

A typical DC-DC converter circuit is shown in Figure 1. The transistors and associated components combine with the transformer primary to form a self-driven oscillator which provides drive to the transformer. The transformer secondary is rectified, filtered and regulated to obtain the outputs required. Typically, the transistors switch in saturated mode at 20 kHz, providing high efficiency square wave drive to the transformer. The output filter capacitors are relatively small compared to sine wave driven transformers and overall losses are quite low. The high speed, saturated switching of the transistors does, however, generate high frequency noise components. These manifest themselves as short duration current spikes drawn from the converter's input supply and as high speed spikes which appear on the output lines. In addition, the transformer can radiate noise in RF fashion. Manufacturers have dealt with these problems through careful converter design, including attention to input filter design, transformer construction and package shielding. Figure 2 shows typical output noise of a good quality commercial DC-DC converter. The spikes are approximately 10 mV–20 mV in amplitude and occur at each transition of the switching transistors. In many applications this noise level is acceptable, but in data acquisition and other systems which work at 12-bit and higher resolutions, problems begin to crop up. In these situations, special system-oriented DC-DC converter techniques must be employed to insure against the problems outlined above.

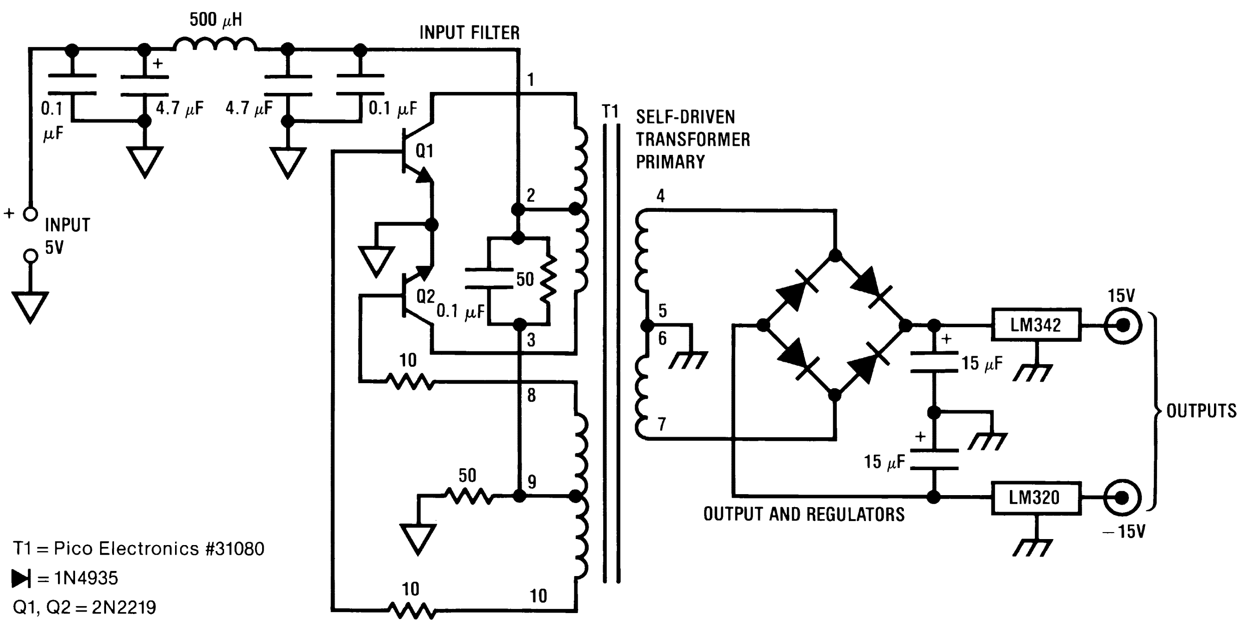

Figure 1. Typical DC-DC Converter

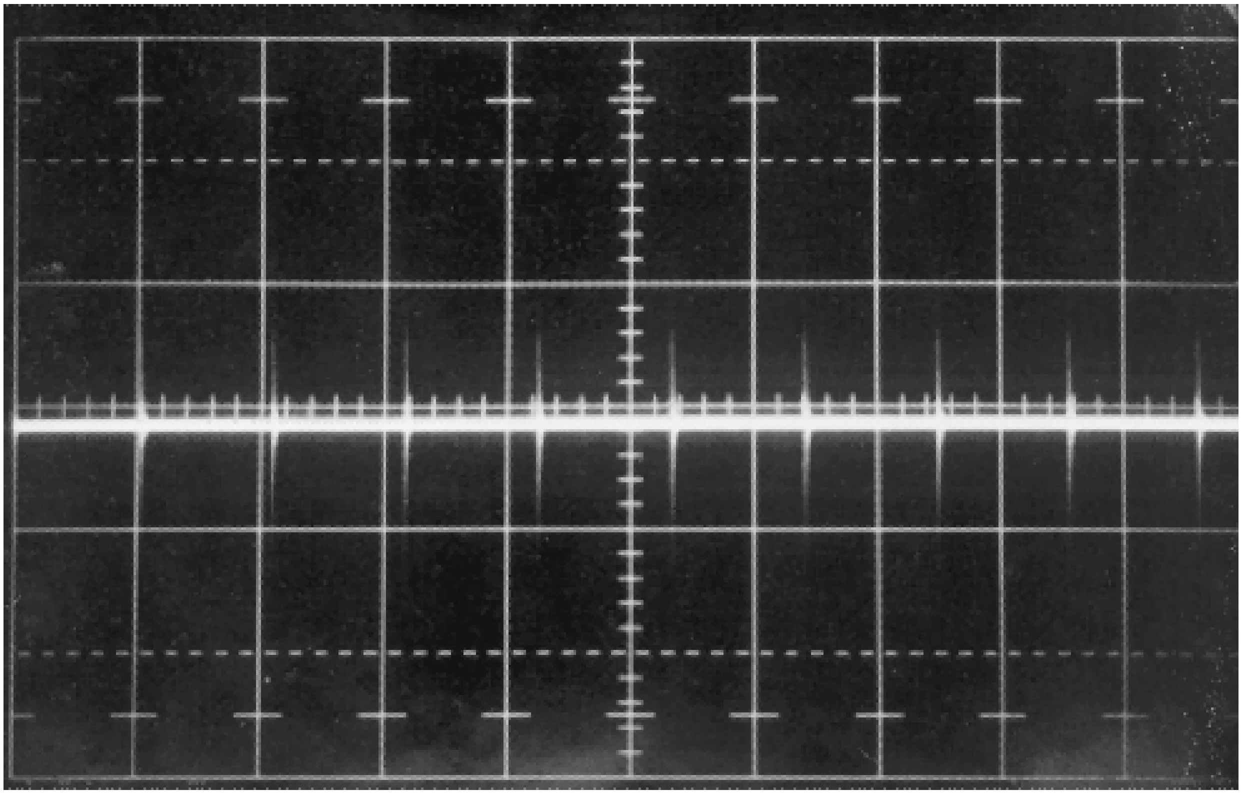

Figure 2. Typical Output Noise of Commercial DC-DC Converter

2 Blank Pulse Converter

Figure 3 shows a converter which will supply 100 mA at ±15V from a 5V input. This design attacks the noise problem in two ways. The LM3524 switching regulator chip provides non-overlapping drive to the transistors, eliminating simultaneous conduction which helps keep input current spiking down. The LM3524 operates open loop. Its feedback connection (pin 9) is tied high, forcing the chip's outputs to full duty cycle. Internal logic in the LM3524 prevents the transistors from conducting at the same time. The components at pins 6 and 7 set the switching frequency. The LM3524's timing ramp biases the LM311 comparator to generate a blank pulse which “brackets” the output noise pulse. Figure 4 shows the switching transistor waveforms (trace A and B) and the blank pulse (trace C) which is issued at each switching transition. The converter's output noise is shown in trace D. The blank pulse is used to alert the system that a noise spike is imminent. In this fashion, a critical A/D conversion or sample-hold operation can be delayed until the converter's noise spike has settled. This technique is quite effective, because it does not allow the system to “see” noise spikes during critical periods. This not only insures good system performance, but also means that a relatively simplistic converter design can be employed. The expense associated with low output noise (e.g., shielding, special filtering, etc.) can be eliminated in many cases. Figure 5 details a converter design which uses a different approach to solving the same problem.

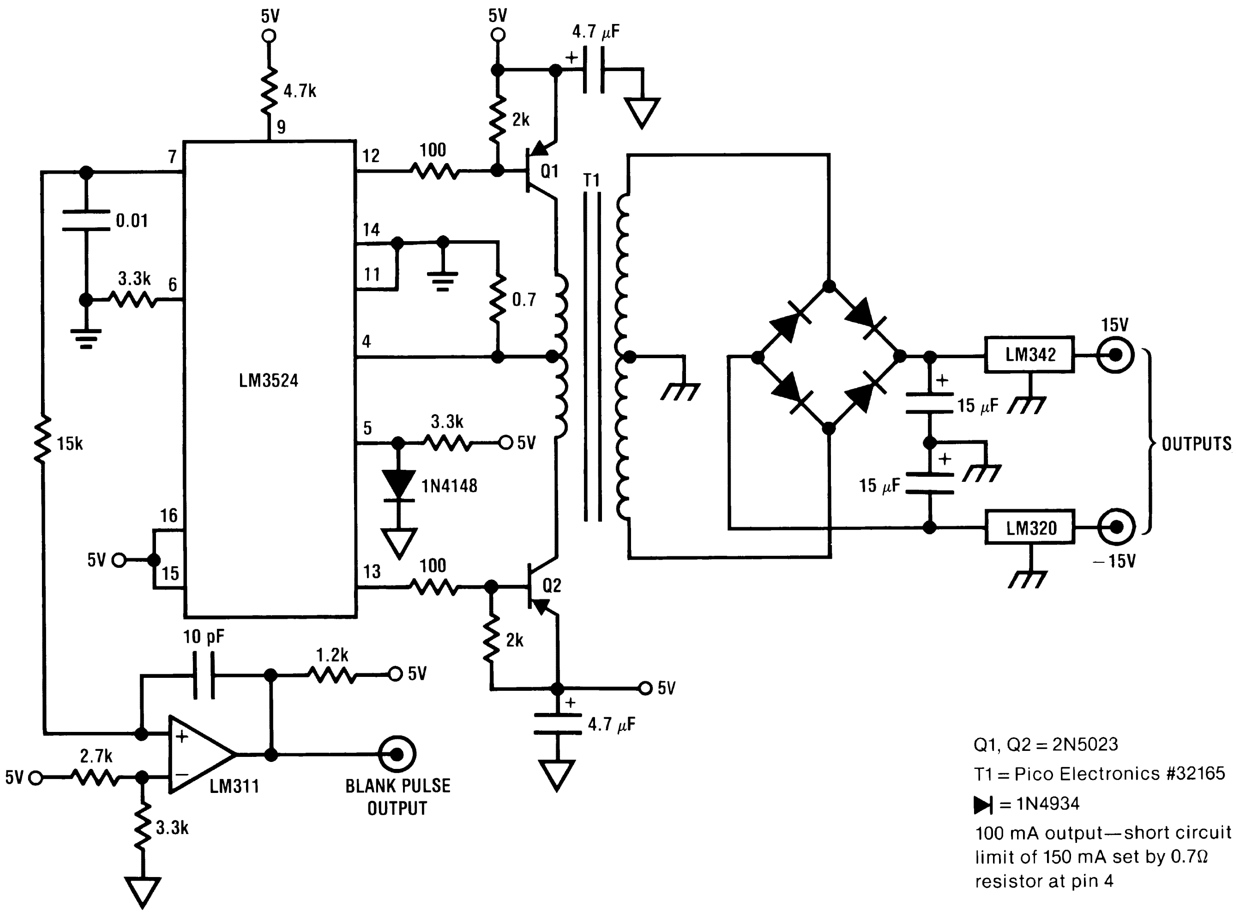

Figure 3. Blank Pulse Converter

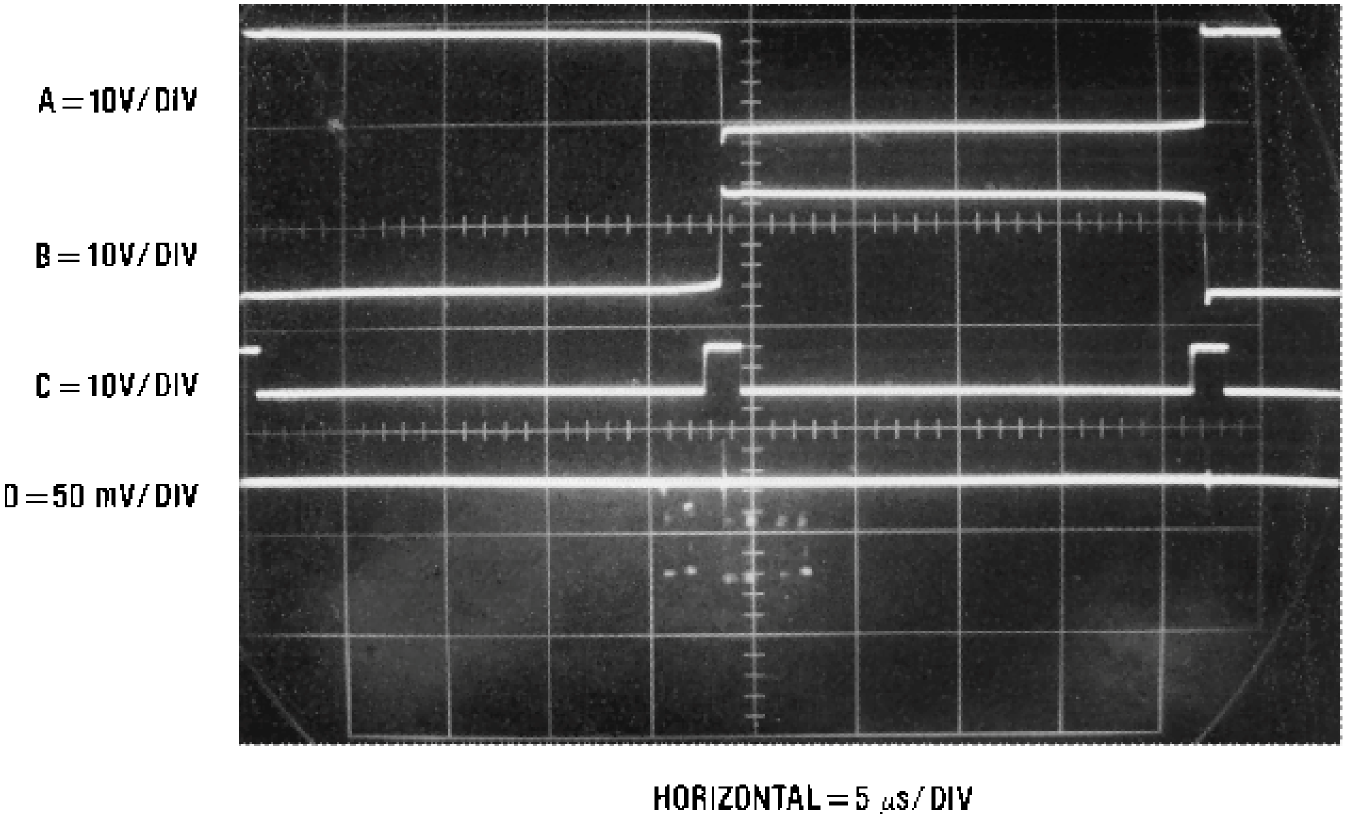

Figure 4. Switching Transistor Waveforms (A and B),Blank Pulse (C), and Converter Output Noise (D)

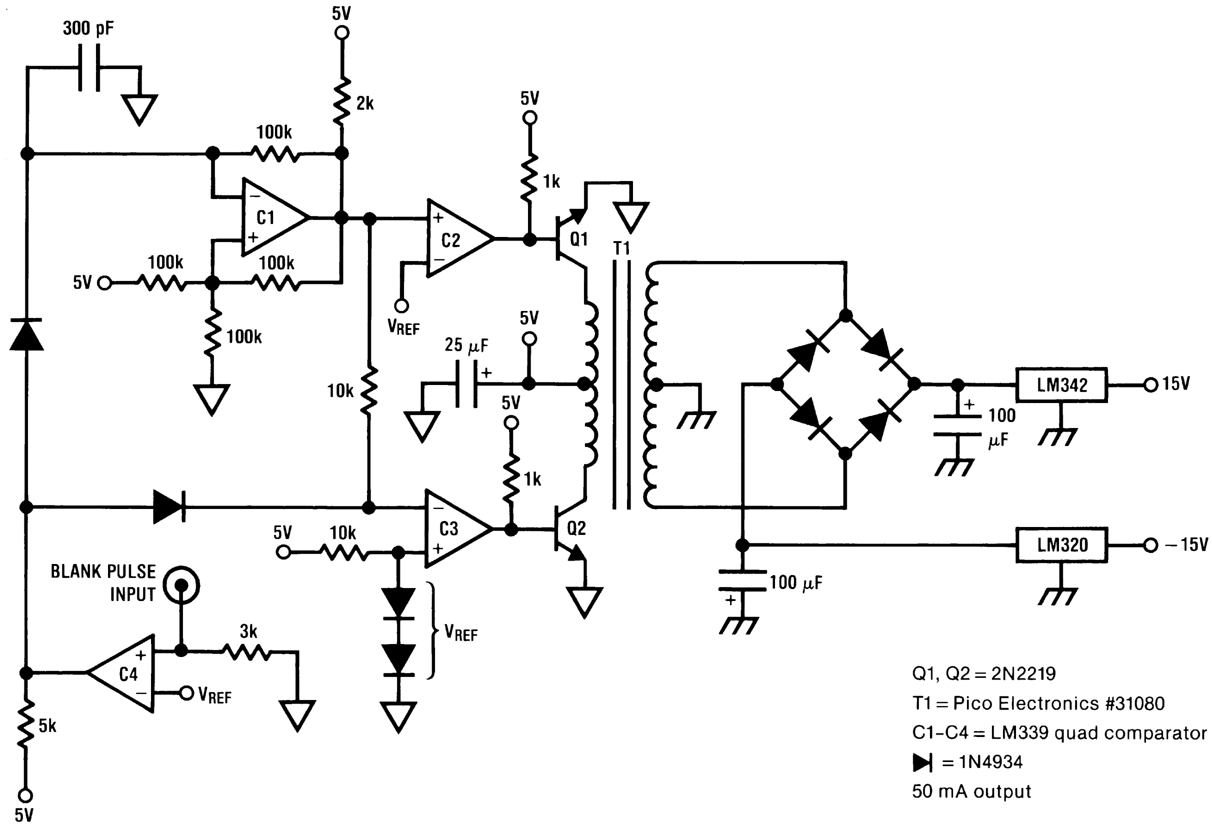

Figure 5. Externally Strobed Converter Design

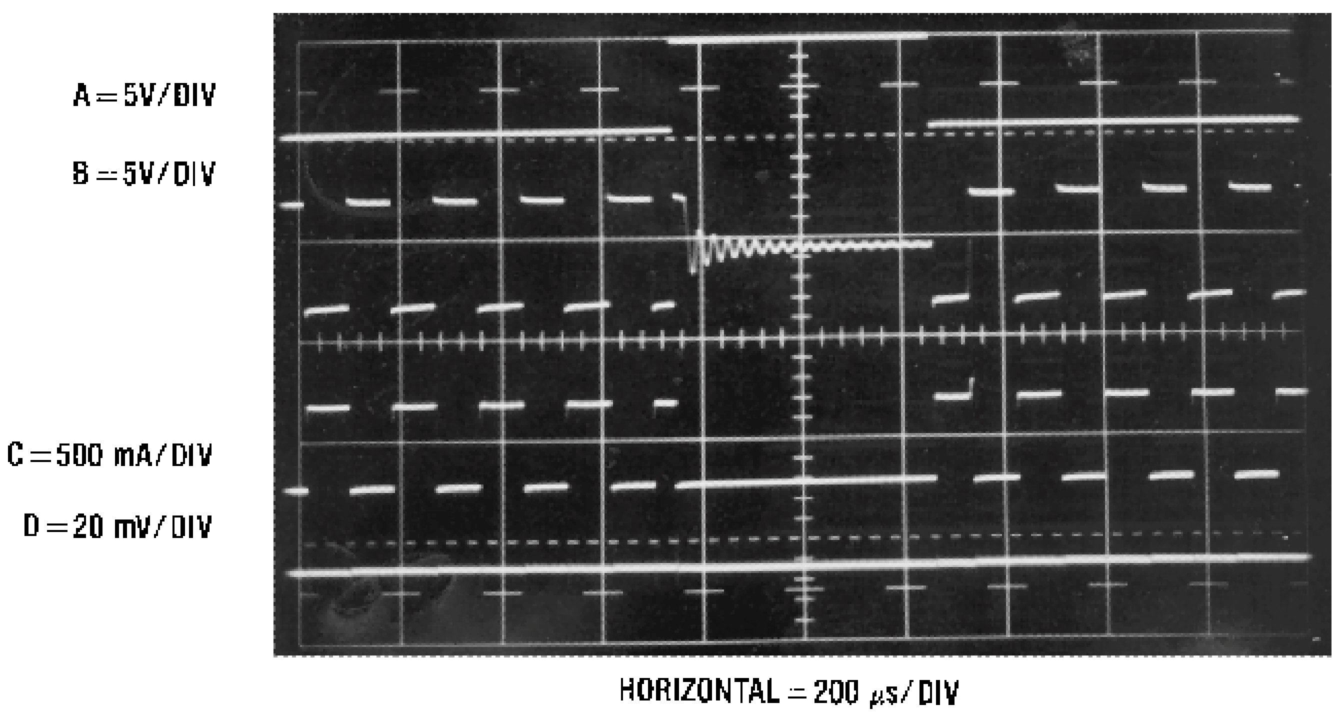

Figure 6. Externally Strobed Converter Waveforms

3 Externally Strobed Converter

In Figure 5 the system controls the converter, instead of the converter issuing blank commands. This arrangement uses an LM339 quad comparator to provide the necessary drive to the converter. C1 functions as a clock which provides drive to C2 and C3. These comparators drive the transistors (trace B, Figure 6 is Q1's collector voltage waveform, while trace C details its current) to provide power to the transformer. When a critical system operation must occur, an external blank pulse (trace A) is applied to C4. C4's output goes high, shutting off all transformer drive. Under these conditions, the transformer current ceases (note voltage ringing on turn-off in trace B) and output noise (trace D) virtually disappears because the output regulators are powered only by the 100 μF filter capacitors. The value of these capacitors will depend directly on the output load and the length of the blank pulse. If synchronization to the system is desired, a system-derived 20 kHz square wave may be applied at C1's negative input through 2k, after removing the 300 pF capacitor and the 100k feedback resistor. The low noise during the blank pulse period affords ideal conditions for sensitive system operations. Although this approach allows great flexibility, the amount of off time is limited by the storage capacity of the output filter capacitors. In most systems this is not a problem, but some cases may require a converter which supplies low noise outputs at 100% duty cycles.

4 Sine Wave Driven Converter

Figure 7 diagrams a converter which sacrifices the efficient saturated-switch mode of operation to achieve an inherently low noise output at a 100% duty cycle. In this converter, sine wave drive is used to power the transformer. Q1 functions as a 20 kHz phase shift oscillator with Q2 providing an emitter-followed output. A1 and A2 are used to drive the transformer in complementary-bridge fashion (traces A and B, Figure 8). The high current output capability of the amplifiers, in combination with the transformer's paralleled primaries, results in a high power transformer drive. The transformer output is rectified, filtered and regulated in the usual fashion. Because the sine wave drive contains little harmonic content and current spiking, output noise is well below 1 mV (trace C, Figure 8). To adjust this circuit, ground the wiper arm of the 1k potentiometer and adjust the 100k value for minimum power supply drain. Next, unground the 1k potentiometer wiper arm and adjust it so that both A1 and A2's outputs are as large as possible without clipping. This circuit yields a low noise output on a 100% available basis but efficiency degrades to about 30%. In relatively low power converters such as this one (for example, 50 mA output current) this is often acceptable.

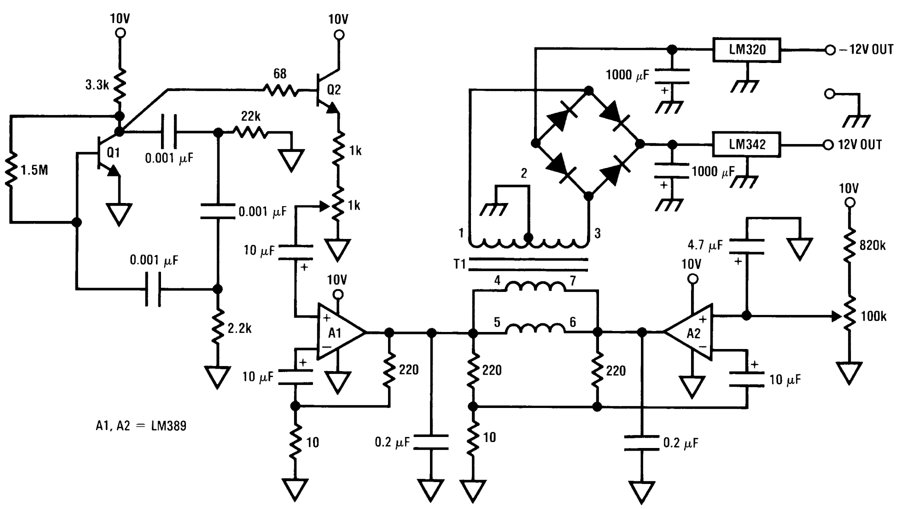

Figure 7. Sine Wave Driven Converter

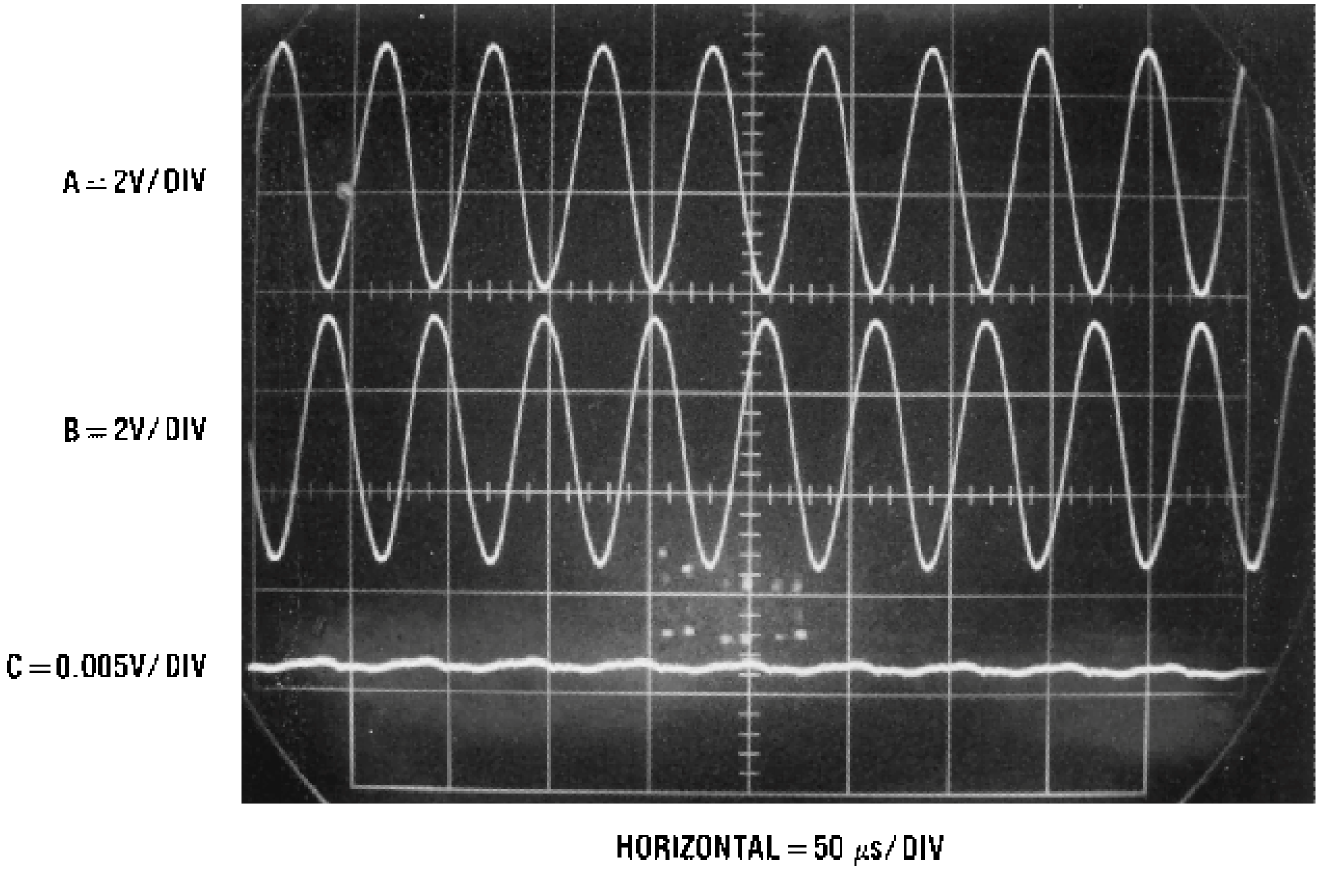

Figure 8. Sine Wave Driven Converter Waveforms

5 Low Power Converter

Figure 9 shows a converter which operates from very low power. This circuit will provide 7.5V output from a 1.5V D cell battery. With a 125 μA load current (typically 20 CMOS ICs) it will run for 3 months. It may be externally strobed off during periods where lowest output noise is desired and it also issues a “converter running” pulse. This circuit is unusual in that the amount of time required for Q1 and Q2 to drive the transformer is directly related to the load resistance. The converter's output voltage is sensed by an LM10 op amp reference IC, which compares the converter output to its own internal 200 mV reference via the 5.1M-160k voltage divider. Whenever the converter output is below 7.5V, the LM10 output goes high, driving the Q1-Q2 pair and the transformer which form an oscillator. The transformer output is rectified and used to charge the 47 μF capacitor. When the capacitor charges to a high enough value, the LM10 output goes low and oscillation ceases. Trace A, Figure 10 shows the collector of Q1, while trace B shows the output voltage across the 47 μF capacitor (AC coupled). It can be seen that each time the output voltage falls a bit the LM10 drives the oscillator, forcing the voltage to rise until it is high enough to switch the LM10 output to its low stage. The frequency of this regulating action is determined by the load on the converter output. To prevent the converter from oscillating about the trip point, the 0.1 μF unit is used to provide hysteresis of response. Very low loading of the converter will result in almost no on time for the oscillator while large loads will force it to run almost constantly. Loop operating frequencies of 0.1 Hz to 40 Hz are typical. The LM10 output state may be used to alert the system that the converter is running. A pulse applied to the LM10 negative input will override normal converter operation for low noise operation during a critical system A/D conversion.

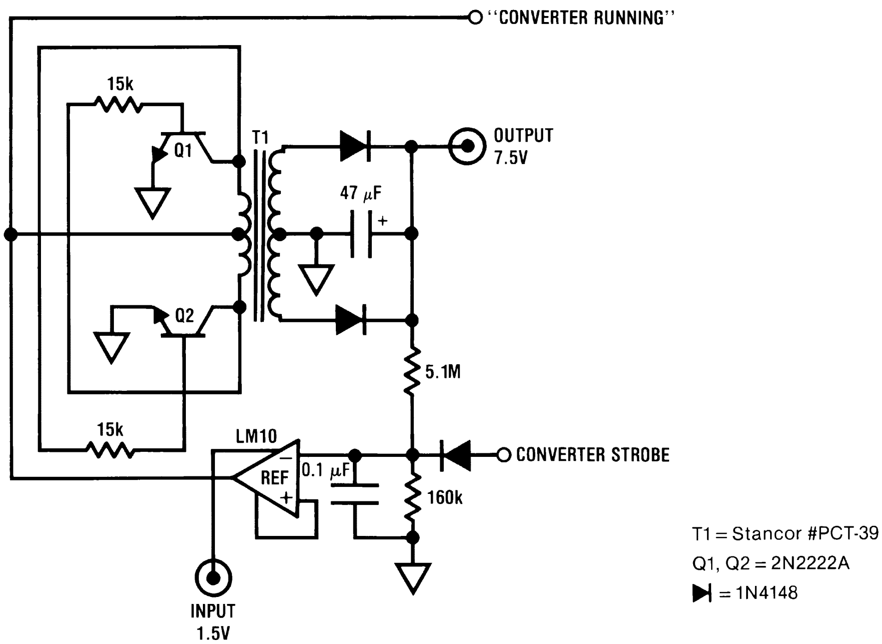

Figure 9. Low Power Converter

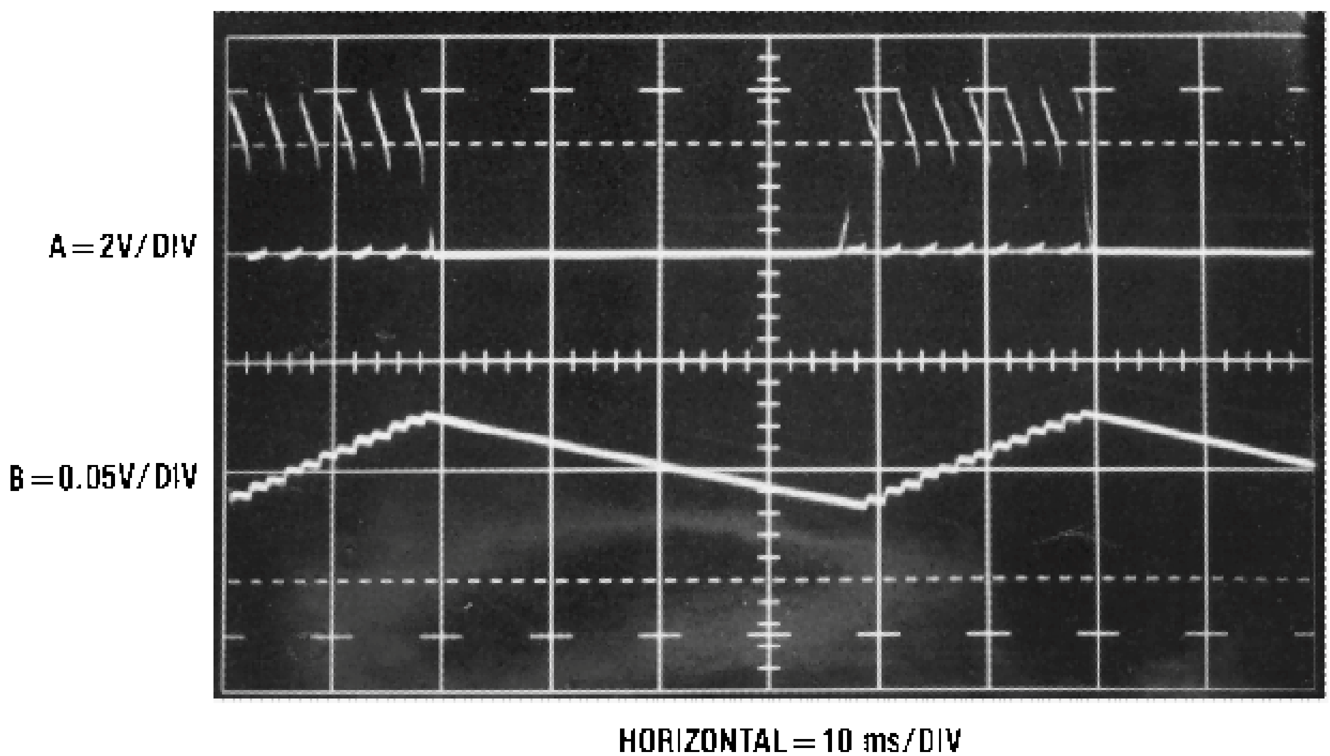

Figure 10. Low Power Converter Waveforms

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