LM108

Application Note 241 Working with High Impedance Op Amps

Literature Number: SNOA664

Working with High Impedance Op Amps

National Semiconductor
Application Note 241
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February 1980

Abstract. *New developments have dramatically reduced the error currents of IC op amps, especially at high temperatures. The basic techniques used to obtain this peformance are briefly described. Some of the problems associated with working at the high impedance levels that take advantage of these low error currents are discussed along with their solutions. The areas involved are printed-circuit board leakage, cable leakage and noise generation, semiconductor-switch leakages, large-value resistors and capacitor limitations.*

INTRODUCTION

A new, low cost op amp reduces dc error terms to where the amplifier may no longer be the limiting factor in many practical circuits. FET bias currents are equalled at room temperature; but unlike FETs, the bias current is relatively stable even over a −55˚C to 125˚C temperature range. Offset voltage and drift are low because bipolar inputs and on-wafer trimming are used. The 100 µV offset voltage and 25 pA bias current are expected to advance the state of the art for high impedance sensors and signal conditioners.

BIAS CURRENTS

There has been a continual effort to reduce the bias current of IC op amps ever since the µA709 was introduced in 1965. The LM101A, announced in 1968, dropped this current by an order of magnitude through improved processing that gave better transistor current gain at low operating currents. In 1969, super-gain transistors (see appendix) were applied in the LM108 to beat FET performance when temperatures above 85˚C were involved.

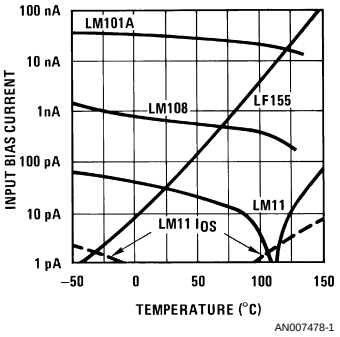

FIGURE 1. Comparison of typical bias currents for various types of IC op amps. New bipolar device not only has lower bias current over practical temperature ranges but also lower drift. Offset current is unusually low with the new design.

In 1974 FETs were integrated with bipolar devices to give the first FET op amp produced in volume, the LF155. These devices were faster than general purpose bipolar op amps and had lower bias current below 70˚C. But FETs exhibit higher offset voltage and drift than bipolars. Long-term stability is also about an order of magnitude worse. Typically, this drift is 100 µV/year, but a small percentage could be as bad as 1 mV. Laser trimming and other process improvements have lowered initial offset but have not eliminated the drift problem.

The new IC is an extension of super-gain bipolar techniques. As can be seen from *Figure 1*, it provides low bias currents over a −55˚C to 125˚C temperature range. The offset current is so low as to be lost in the noise. This level of performance has previously been unavailable for either low-cost industrial designs or high reliability military/space applications.

This low bias current has not been obtained at the expense of offset voltage or drift. Typical offset voltage is under a millivolt and provision is made for on-water trimming to get it below 100 µV. The low drift exhibited in *Figure 2* indicates that the circuit is inherently balanced for exceptionally low drift, typically 1 µV/˚C below 100˚C.

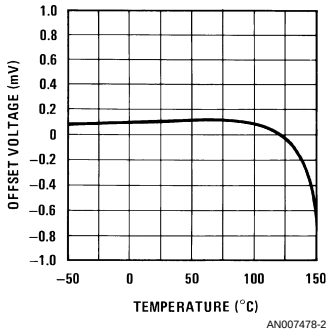

FIGURE 2. Bipolar transistors have inherently low offset voltage and drift. The low drift of the LM11 over a wide temperature range shows that there are no design problems degrading performance.

THE NEW OP AMP

The LM11 is, in essence, a refinement of the LM108. A modified Darlington input stage has been added to reduce bias currents. With a standard Darlington, one transistor is biased with the base current of the other. This degrades dc amplifier performance because base current is noisy, subject to wide variation and generally unpredictable.

Supplying a bleed current greater than the base current, as shown in *Figure 3*, removes this objection. The 60 nA provided is considerably in excess of the 1 nA base current. The bleed current is made to vary as absolute temperature to maintain constant impedance at the emitters of Q1 and Q2. This stabilizes frequency response and also reduces the

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thermal variation of bias current. Parasitic capacitances of the current generator have been bootstrapped so that the 0.3 V/µs slew rate of the basic amplifier is unaffected.

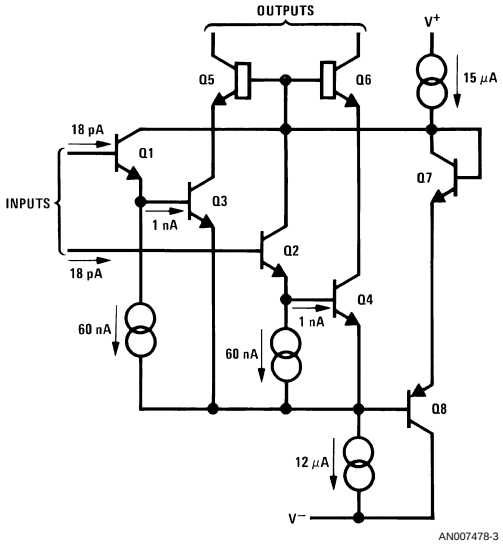


FIGURE 3. Modifying Darlington with bleed current reduces offset voltage, drift and noise. Unique circuitry provides well-controlled current with minimal stray capacitance so that speed of the basic amplifier is unaffected.

Results to date suggest that the base currents of this modified Darlington input are better matched than the simple differential amplifier. In fact, offset current is so low as to be unmeasurable on production test systems. Therefore, guaranteed limits are determined by the test equipment rather than the IC.

NOISE

Operating transistors at very low currents does increase noise. Thus, the LM11 is about a factor of four noisier than the LM108. But the low frequency noise, plotted in *Figure 4*, is still slightly less than that of FET amplifiers. Long-term measurements indicate that the offset voltage shift is under 10 µV.

In contrast to the noise voltage, low frequency noise current is subject to greater unit-to-unit variation. Generally, it is below 1 pA, peak-to-peak, about the same magnitude as the offset current.

With the LM11, both voltage and current related dc errors have been reduced to the point where overall circuit performance could well be noise limited, particularly in limited temperature range applications.

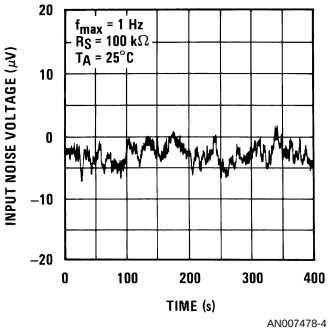


FIGURE 4. Lower operating currents increase noise, but low frequency noise is still slightly lower than IC FET amplifiers. Long-term stability is much improved.

RELIABILITY

The reliability of the LM11 is not expected to be substantially different than the LM108, which has been used extensively in military and space applications. The only significant difference is the input stage. The low current nodes introduced here might possibly be a problem were they not bootstrapped, biased and guarded to be virtually unaffected by both bulk and surface leakages. This opinion is substantiated by preliminary life-test data.

This IC could, in fact, be expected to improve reliability when used to replace discrete or hybrid amplifiers that use selected components and have been trimmed and tweaked to give the required performance.

From an equipment standpoint, reliability analysis of insulating materials, surface contamination, cleaning procedures, surface coating and potting are at least as important as the IC and other components. These factors become more important as impedance levels are raised. But this should not discourage designers. If poor insulation and contamination cause a problem when impedance levels are raised by an order of magnitude, it is best found out and fixed.

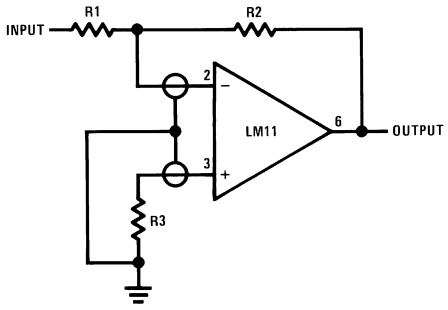
Even so, it may not be advisable to take advantage of the full potential of the LM11 in all cases, especially when hostile environments are involved. For example, there should be no great difficulty in finding an LM11 with offset current less than 5 pA over a −55˚C to 125˚C temperature range. But anyone

designing high-reliability equipment that is going to be in trouble if combined leakages are greater than 10 pA at 125°C had best know what he is about.

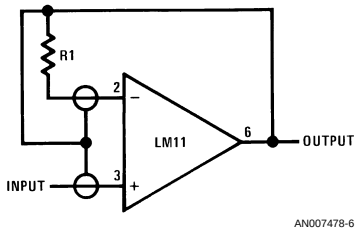
ELECTRICAL GUARDING

The effects of board leakage can be minimized using an old trick known as guarding. Here the input circuitry is surrounded by a conductive trace that is connected to a low impedance point at the same potential as the inputs. The electrical connection of the guard for the basic op amp configurations is shown in *Figure 5*. The guard absorbs the leakage from other points on the board, drastically reducing that reaching the input circuitry.

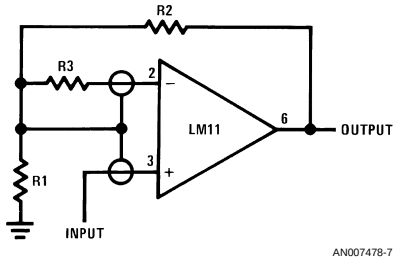
To be completely effective, there should be a guard ring on both sides of the printed-circuit board. It is still recommended for single-sided boards, but what happens on the unguarded side is difficult to analyze unless Teflon inserts are used on the input leads. Further, although surface leakage can be virtually eliminated, the reduction in bulk leakage is much less. The reduction in bulk leakage for double-sided guarding is about an order of magnitude, but this depends on board thickness and the width of the guard ring. If there are bulk leakage problems, Teflon inserts on the through holes and Teflon or kel-F standoffs for terminations can be used. These two materials have excellent surface properties without surface treatment even in high-humidity environments.



a. inverting amplifier



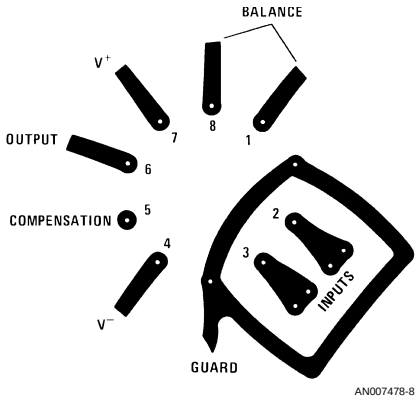
b. follower



c. non-inverting amplifier

FIGURE 5. Input guarding for various op amp connections. The guard should be connected to a point at the same potential as the inputs with a low enough impedance to absorb board leakage without introducing excessive offset.

An example of a guarded layout for the metal-can package is shown in *Figure 6*. Ceramic and plastic dual-in-line packages are available for critical applications with guard pins adjacent to the inputs both to facilitate board layout and to reduce package leakage. These guard pins are not internally connected.



Bottom View

FIGURE 6. Input guarding can drastically reduce surface leakage. Layout for metal can is shown here. Guarding both sides of board is required. Bulk leakage reduction is less and depends on guard ring width.

SIGNAL CABLES

It is advisable to locate high impedance amplifiers as close as possible to the signal source. But sometimes connecting lines cannot be avoided. Coaxially shielded cables with good insulation are recommended. Polyethelene or virgin (not reconstituted) Teflon is best for critical applications.

In addition to potential insulation problems, even short cable runs can reduce bandwidth unacceptably with high source resistances. These problems can be largely avoided by bootstrapping the cable shield. This is shown for the follower connection in *Figure 7*. In a way, bootstrapping is positive feedback; but instability can be avoided with a small capacitor on the input.

CABLE BOOTSTRAPPING

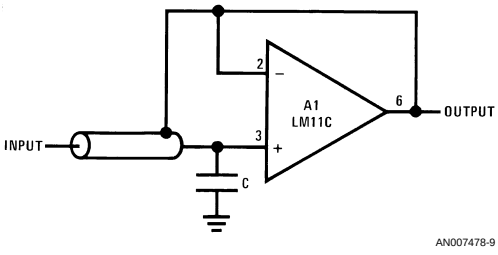


FIGURE 7. Bootstrapping input shield for a follower reduces cable capacitance, leakage and spurious voltages from cable flexing. Instability can be avoided with small capacitor on input.

With the summing amplifier, the cable shield is simply grounded, with the summing node at virtual ground. A small feedback capacitor may be required to insure stability with the added cable capacitance. This is shown in *Figure 8*.

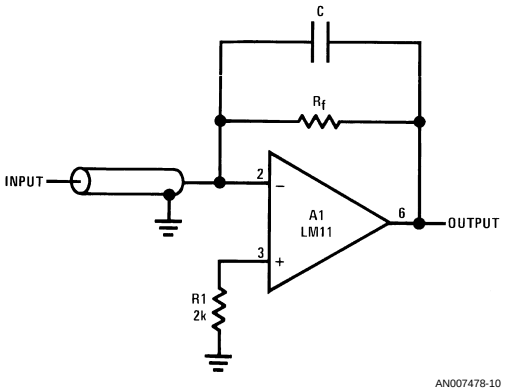


FIGURE 8. With summing amplifier, summing node is at virtual ground so input shield is best grounded. Small feedback capacitor insures stability.

An inverting amplifier with gain may require a separate follower to drive the cable shield if the influence of the capacitance, between shield and ground, on the feedback network cannot be accounted for.

High impedance circuits are also prone to mechanical noise (microphonics) generated by variable stray capacitances. A capacitance variation will generate a noise voltage given by

$$e_n = \frac{\Delta C}{C} V,$$

where V is the dc bias on the capacitor. Therefore, the wiring and components connected to sensitive nodes should be mechanically rigid.

This is also a problem with flexible cables, in that bending the cable can cause a capacitance change. Bootstrapping the shield nearly eliminates dc bias on the cable, minimizing the voltage generated. Another problem is electrostatic charge created by friction. Graphite lubricated Teflon cable will reduce this.

SWITCH LEAKAGE

Semiconductor switches with leakage currents as low as the bias current of the LM11 are not generally available when operation much above 50˚C is involved. The sample-and-hold circuit in *Figure 10* shows a way around this problem. It is arranged so that switch leakage does not reach the storage capacitor.

Isolating leakage current requires that two switches be connected in series. The leakage of the first, Q1, is absorbed by R1 so that the second, Q2, only has the offset voltage of the op amp across its junctions. This can be expected to reduce leakage by at least two orders of magnitude. Adjusting the op

amp offset to zero at the maximum operating temperature will give the ultimate leakage reduction, but this is not usually required with the LM11.

MOS switches with gate-protection diodes are preferred in production situations as they are less sensitive to damage from static charges in handling. If used, D1 and R2 should be included to remove bias from the protection diode during hold. This may not be required in all cases but is advised since leakage from the protection diode depends on the internal geometry of the switch, something the designer does not normally control.

A junction FET could be used for Q1 but not Q2 because there is no equivalent to the enhancement mode MOSFET. The gate of a JFET must be reverse biased to turn it off, and leakage on its output cannot be avoided.

HIGH-VALUE RESISTORS

Using op amps at very high impedance levels can require unusually large resistor values. Standard precision resistors are available up to 10 MΩ. Resistors up to 1 GΩ can be obtained at a significant cost premium. Larger values are quite expensive, physically large and require careful handling to avoid contamination. Accuracy is also a problem. There are techniques for raising effective resistor values in op amp circuits. In theory, performance is degraded; in practice, this may not be the case.

With a buffer amplifier, it is sometimes desirable to put a resistor to ground on the input to keep the output under control when the signal source is disconnected. Otherwise it will saturate. Since this resistor should not load the source, very large values can be required in high-impedance circuits.

Figure 9 shows a voltage follower with a 1 GΩ input resistance built using standard resistor values. With the input disconnected, the input offset voltage is multiplied by the same factor as R2; but the added error is small because the offset voltage of the LM11 is so low. When the input is connected to a source less than 1 GΩ, this error is reduced. For an ac-coupled input, a second 10 MΩ resistor could be connected in series with the inverting input to virtually eliminate bias current error; bypassing it would give minimal noise.

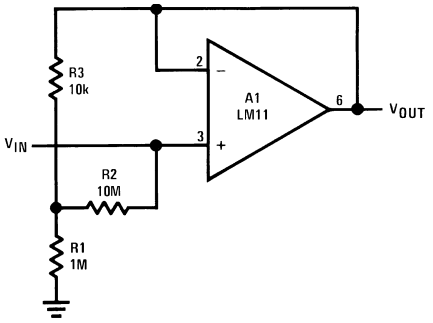
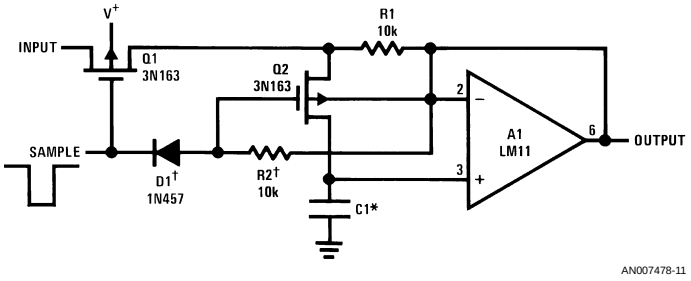


FIGURE 9. Follower input resistance is 1 GΩ. With the input open, offset voltage is multiplied by 100, but the added error is not great because the op amp offset is low.

The voltage-to-current converter in *Figure 11* uses a similar method to obtain the equivalent of a 10 GΩ feedback resistor. Output offset is reduced because the error can be made dependent on offset current rather than bias current. This would not be practical with large value resistors because of cost, particularly for matched resistors, and because the summing node would be offset several hundred millivolts from ground. In *Figure 11*, this offset is limited to several millivolts. In addition, the output can be nulled with the usual balance potentiometer. Further, gain trimming is easily done.



* polystyrene or Teflon

† required if protected-gate switch is used

FIGURE 10. Switch leakage in this sample and hold does not reach storage capacitor. If Q2 has an internal gate-protection diode, D1 and R2 must be included to remove bias from its junction during hold.

Resistance Multiplication

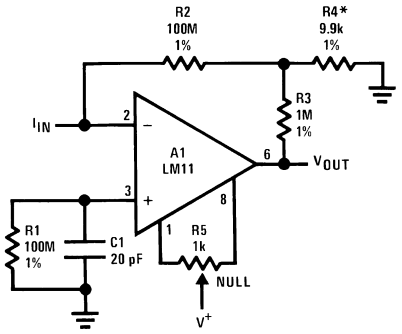


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FIGURE 11. Equivalent feedback resistance is 10 GΩ, but only standard resistors are used. Even though the offset voltage is multiplied by 100, output offset is actually reduced because error is dependent on offset current rather than bias current. Voltage on summing junction is less than 5 mV.

This circuit would benefit from lower offset current than can be tested and guaranteed with automatic test equipment. But there should be no problem in selecting a device for critical applications.

CAPACITORS

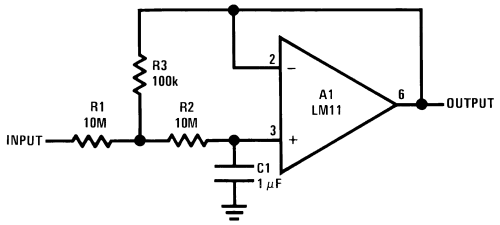
Op amp circuits impose added requirements on capacitors, and this is compounded with high-impedance circuitry. Frequency shaping and charge measuring circuits require control of the capacitor tolerance, temperature drift and stability with temperature cycling. For smaller values, NPO ceramic is best while a polystyrene-polycarbonate combination gives good results for larger values over a −10˚C to 85˚C range.

Dielectric absorption can also be a problem. It causes a capacitor that has been quick-charged to drift back toward its previous state over many milliseconds. The effect is most noticeable in sample-and-hold circuits. Polystyrene, Teflon and NPO ceramic capacitors are most satisfactory in this regard. Choice depends mainly on capacitance and temperature range.

Insulation resistance can clearly become a problem with high-impedance circuitry. Best performer is Teflon, with polystyrene being a good substitute below 85˚C. Mylar capacitors should be avoided, especially where higher temperatures are involved.

Temperature changes can also alter the terminal voltage of a capacitor. Because thermal time constants are long, this is only a problem when holding intervals are several minutes or so. The effect is reported to be as high as 10 mV/˚C, but Teflon capacitors that hold it to 0.5 mV/˚C are available*.

An op amp with lower bias current can ease capacitor problems, primarily by reducing size. This is obvious with a sample-and-hold because the capacitor value is determined by the hold interval and the amplifier bias current. The circuit in *Figure 12* is another example. An RC time constant of more than a quarter hour is obtained with standard component values. Even when such long time constants are not required, reducing capacitor size to where NPO ceramics can be used is a great aid in precision work.



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$$\tau = \frac{R1\,C}{R3}(R2 + R3)$$

$$\Delta V_{OUT} = \frac{R1 + R3}{R3}(I_B\,R2 + V_{OS})$$

FIGURE 12. This circuit multiplies RC time constant to 1000 seconds and provides low output impedance. Cost is lowered because of reduced resistor and capacitor values.

Note: *Component Research Co., Inc., Santa Monica, California.

CONCLUSIONS

A low cost IC op amp has been described that not only has low offset voltage but also advances the state of the art in reducing input current error, particularly at elevated temperatures. Designers of industrial as well as military/space equipment can now work more freely at high impedance levels.

Although high-impedance circuitry is more sensitive to board leakages, wiring capacitances, stray pick-up and leakage in other components, it has been shown how input guarding, bootstrapping, shielding and leakage isolation can largely eliminate these problems.

ACKNOWLEDGMENT

The author would like to acknowledge the assistance of the staff at National Semiconductor in implementing this design and sorting out the application problems. Discussions with Bob Dobkin, Bob Pease, Carl Nelson and Mineo Yamatake have been most helpful.

APPENDIX

SUPER-GAIN TECHNIQUES

Super-gain transistors are not new, having been developed for the LM102/LM110 voltage followers in 1967 and later used on the LM108 general-purpose op amp. They are similar to regular transistors, except that they are diffused for high current gains (2,000–10,000) at the expense of breakdown voltage. A curve-tracer display of a typical device is shown in *Figure 13*. In an IC, super-gain transistors can be

made simultaneously with standard transistors by including a second, light base predeposition that is diffused less deeply.

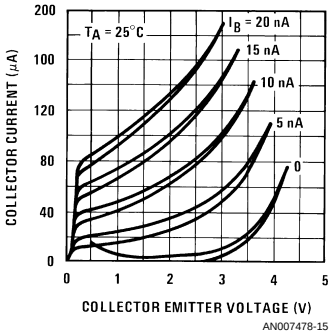

FIGURE 13. Curve tracer display of a super-gain transistor

Super-gain transistors can be connected in cascode with regular transistors to form a composite device with both high gain and high breakdown. The simplified schematic of the LM108 input stage in *Figure 14* shows how it is done. A common base pair, Q3 and Q4, is bootstrapped to the input transistors, Q1 and Q2, so that the latter are operated at nearly zero collector-base voltage, no matter what the input common-mode. The regular NPN transistors are distinguished by drawing them with wider base regions.

Operating the input transistors at very low collector-base voltage has the added advantage of drastically reducing collector-base leakage. In this configuration bipolar transistors are affected little by the leakage currents that limit performance of FET amplifiers.

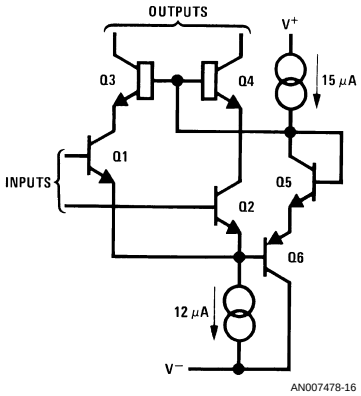

FIGURE 14. A bootstrapped input stage

***See Addendum at the End of Application Note 242.**

Book Extract End

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