Application Report
SNOA486B–March 2007–Revised May 2013

AN-1604 Decompensated Operational Amplifiers

ABSTRACT

This application report discusses the what, why, and where of decompensated op amps. This application report also describes external compensation techniques, such as reducing loop gain, to stabilize op amps operated at gains less than the minimum stable gain specified in the datasheet. A comprehensive treatment of input lead-lag compensation including examples is presented.

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1 Introduction to Decompensated Amplifiers

1.1 What is a Decompsensated Amplifier?

A decompensated operational amplifier has internal frequency compensation designed to work with external gain-setting resistors such that the resultant closed loop gain is restricted to a number that is greater than a specified minimum. This minimum gain is specified on the decompensated op amp's datasheet. Compensated op amps, or simply op amps, are traditionally designed to be stable for gains down to and including unity gain. Decompensated, or less compensated op amps, exhibit higher bandwidth and slew rate than op amps compensated for unity gain.

As shown in Figure 1, the reduced internal compensation of an op amp is such that the dominant pole f_d for the unity-gain stable op amp is moved to the position f_1 in the case of the decompensated op amp. The change in internal compensation increases the bandwidth capability of the op amp for the same amount of power consumed. That is, the decompensated op amp has an increased bandwidth to power ratio when compared to a unity gain stable op amp of equivalent geometry.

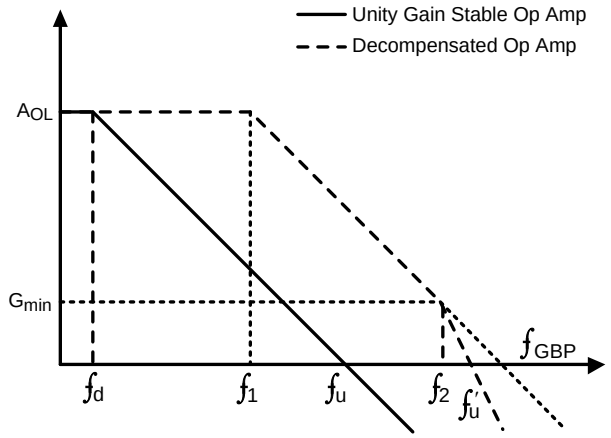

Figure 1. Gain vs. Frequency Characteristics for a Unity Gain Stable Op Amp and a Decompensated Op Amp

Compared with the unity gain stable amplifier, the decompensated version has the following advantages:

1. An open-loop gain which extends to a higher frequency.
2. A higher frequency closed-loop bandwidth.
3. A better slew rate.

1.2 Why Use a Decompensated Op Amp?

A decompensated amplifier is designed to maximize bandwidth performance. It exhibits an increase in small signal bandwidth, slew rate, and full power bandwidth when compared to an equivalent unity-gain stable op amp. Full power bandwidth is the maximum frequency at which an undistorted sine wave is reproduced at the output of the op amp.

Full power bandwidth is calculated with the formula:

$$FPBW = \frac{SR}{2\pi V_P} \tag{1}$$

where SR is the slew rate, and V_P is the peak amplitude of the output.

Consequently an increased slew rate results in an increased full power bandwidth. Slew rate determines the maximum frequency attainable for a minimum-distortion signal at the output for a specified output swing. A decompensated op amp exhibits a better bandwidth-to-supply current ratio than an equivalent unity-gain stable op amp.

1.3 Where are Decompensated Op Amps Used?

Decompensated op amps should be used in high-gain applications, where the ratio of supply current to overall bandwidth is important. The compensation techniques are effective in maintaining circuit stability when an op amp is used at gains below the minimum specified by the manufacturer.

2 Using External Compensation to Stabilize Decompensated Gains Below the Minimum Specified

2.1 Introduction

This section discusses the problem of instability in an op amp operated below a specified minimum gain, provides a procedure for determining the feedback function, and develops a compensation technique by reducing the loop gain.

2.2 Determining the Feedback Function

The feedback function (F) of an arbitrary electronic circuit, such as that shown in Figure 2, is the ratio of the signal that is fed back to the input from the output to the output of the same circuit.

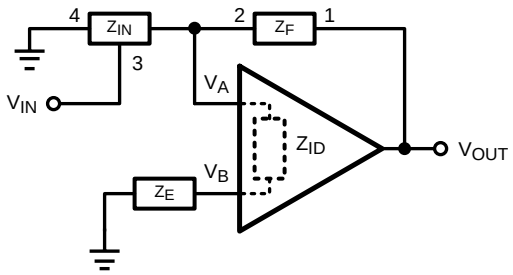

Figure 2. Three-Terminal Network Circuit

The feedback function (F) for the three-terminal network above is the feedback voltage $V_A - V_B$ across the op amp input terminals relative to the op amp output voltage, V_{OUT}.

That is:

$$F = \frac{V_A - V_B}{V_{OUT}} \quad (2)$$

2.3 Reducing the Loop Gain

2.3.1 Analysis

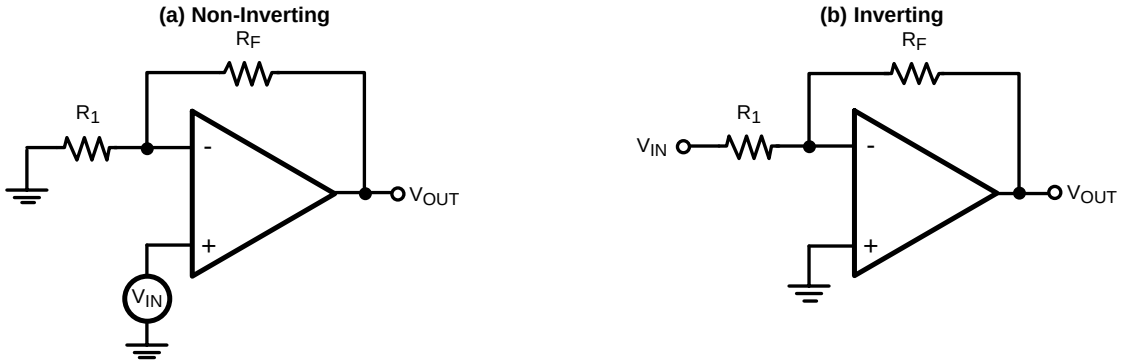

Figure 3. Op Amp with Resistive Feedback

For the op amps shown in Figure 3:

$$\frac{1}{F} = 1 + \frac{R_F}{R_1} \tag{3}$$

The closed loop gain for the non-inverting configuration is:

$$A_{CL} = 1 + \frac{R_F}{R_1} = \frac{1}{F} \tag{4}$$

The closed loop gain for the inverting configuration is:

$$A_{CL} = - \frac{R_F}{R_1} = 1 - \frac{1}{F} \tag{5}$$

The minimum closed loop gain as specified on the datasheet of a particular op amp is shown as G_{min} in Figure 1. For best practice stable operation, the minimum value of 1/F must be equal to or greater than G_{min}.

The minimum closed loop gain for a non-inverting configuration that assures op amp stability is:

$$A_{CL}\ (min) = G_{min} \tag{6}$$

and for an inverting configuration:

$$|A_{CL}|(min) = G_{min} - 1 \tag{7}$$

If R_1 and R_F are chosen so that the closed loop gain is lower than the minimum gain required for stability, then 1/F intersects with the open loop gain at a value that is lower than G_{min}. For example, the G_{min} equal to 10 V/V (20 dB) condition is shown as the dashed line in Figure 4. The resistor choice of $R_F = R_1 = 2\ k\Omega$ makes 1/F equal 2 V/V (6 dB), shown in Figure 4 as the solid line. This system example has less than 45° of phase margin and may show symptoms of instability. The significance of the A and 1/F intercept is that it represents the frequency for which the loop gain magnitude is exactly "1" (0 dB). Consequently, the total phase shift around the loop at the frequency of this intercept determines the phase margin and the overall system stability.

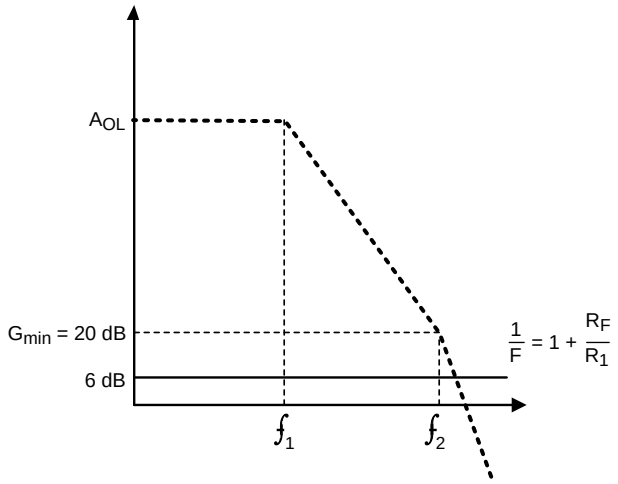

Figure 4. 1/F for $R_F = R_1$ and Open Loop Gain Plot

One approach to stabilizing the system is to assign a value to 1/F such that the 1/F line intercepts the open loop gain at a value in dB that is equal to or greater than G_{min}. This realizes a phase margin of 45° or greater. A straightforward way to implement this is to add a resistor, R_c, between the inverting and the non-inverting inputs as shown in Figure 5.

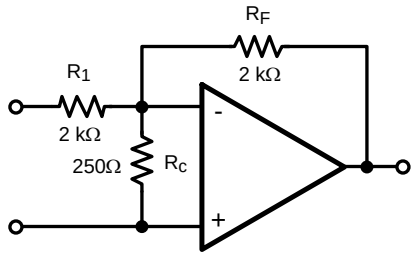

Figure 5. Op Amp with Compensation Resistor Between Inputs

The 1/F function of this circuit is:

$$\frac{1}{F} = 1 + \frac{R_F}{R_1 \,||\, R_c} = 1 + \frac{R_F}{R_1} + \frac{R_F}{R_c} \tag{8}$$

Proper selection of the value of R_c results in the shifting of the 1/F function to G_{min} or greater, thus fulfilling the manufacturer's datasheet condition for circuit stability. The compensation technique of reducing the loop gain may be used to stabilize the circuit for the values given in the previous example, that is G_{min} = 20 dB and = 2 kΩ. A resistor value of 250Ω applied between the amplifier inputs shifts the 1/F curve to the value G_{min} (20 dB) as shown by the dashed line in Figure 6. This results in overall stability for the circuit.

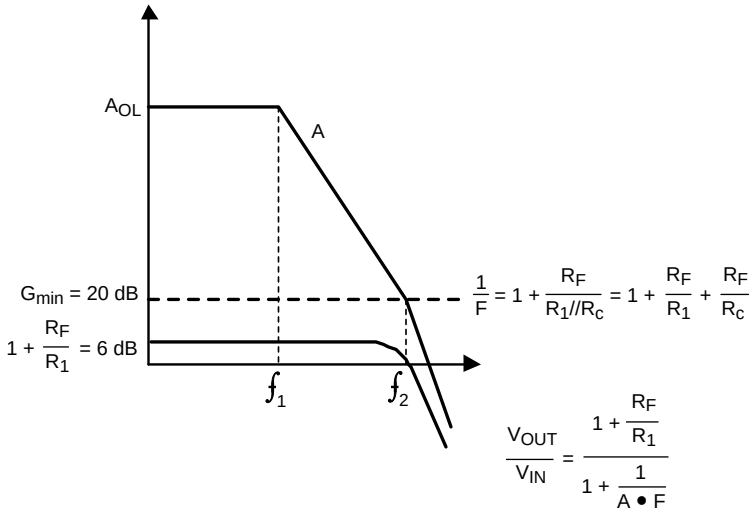

Figure 6. Compensation with Reduced Loop Gain

2.4 R_C Effect on the Closed Loop Gain

The example given above represented by Figure 4 and Figure 5 was generic in the sense that the G_{min} as specified did not distinguish between inverting and non-inverting configurations. Also, note that Figure 4 does not include a closed loop gain plot.

The technique of reducing loop gain to stabilize a decompensated op amp circuit will be illustrated using the non-inverting configuration shown in Figure 7. This example illustrates the effect on the circuit of the choice of R_c.

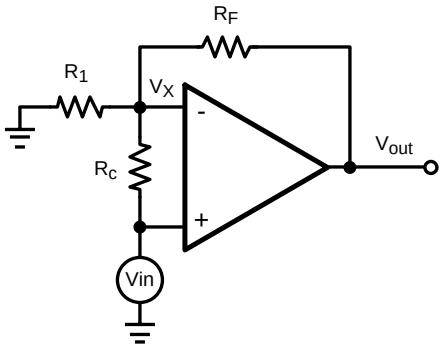

Figure 7. Closed Loop Gain Analysis of the Circuit with R_c

Assume the voltage at the inverting input of the op amp is V_X.

Then:

$$(V_{IN} - V_X) \cdot A = V_{OUT} \tag{9}$$

$$\frac{V_X}{R_1} + \frac{V_X - V_{in}}{R_c} = \frac{V_{out} - V_X}{R_F} \tag{10}$$

Combining Equation 9, Equation 10, and Equation 8 produces the following equation for closed loop gain:

$$\frac{V_{out}}{V_{in}} = \frac{1 + \frac{R_F}{R_1}}{1 + \frac{1}{A \bullet F}} \tag{11}$$

By inspection of Equation 11, R_c does not affect the ideal closed loop gain. In this example where $R_F = R_1$, the closed loop gain remains at 6 dB as long as AF >> 1. The closed loop gain curve is shown as the solid line in Figure 6.

The addition of R_c affects the circuit in the following ways:

1. 1/F is moved to a higher gain, resulting in overall system stability.

   However, adding R_c results in reduced loop gain and increased noise gain. Recall that noise gain is defined as the inverse of the feedback factor, F. In effect, loop gain is traded for stability.
2. The ideal closed loop gain retains the same value as the circuit without the compensation resistor R_c.

3 Input Lead-Lag Compensation

3.1 Introduction

A useful technique for compensating a non-unity gain stable amplifier for gain settings less than the minimum specified is input lead-lag compensation. The compensation components added to the op amp circuit shape the feedback function in a way that insures sufficient phase margin when loop gain is 0 dB. This section will analyze input lead-lag compensation for op amps, provide a procedure for calculating the compensation components, and present inverting and non-inverting design examples using this procedure.

Texas Instruments LMH6624 is an example of an op amp with a minimum stable gain specification. The LMH6624 can be compensated using the input lead-lag technique to establish circuit stability in low gain applications.

The LMH6624 is a dual 1.5 GHz op amp with an input referred voltage noise specification of just 0.92 nV/$\sqrt{\text{Hz}}$. Figure 8 is the open loop Bode plot approximation for the LMH6624. This amplifier has a dominant pole at approximately 100 kHz and a second pole at 100 MHz. The LMH6624 datasheet specifies that it is stable for gains equal to or greater than 10 V/V. For the 20 dB gain point (10 V/V) the device exhibits a phase margin of 45° if the external circuitry does not add additional phase shift. Gain settings below 20 dB have the potential for instability even with resistive feedback components.

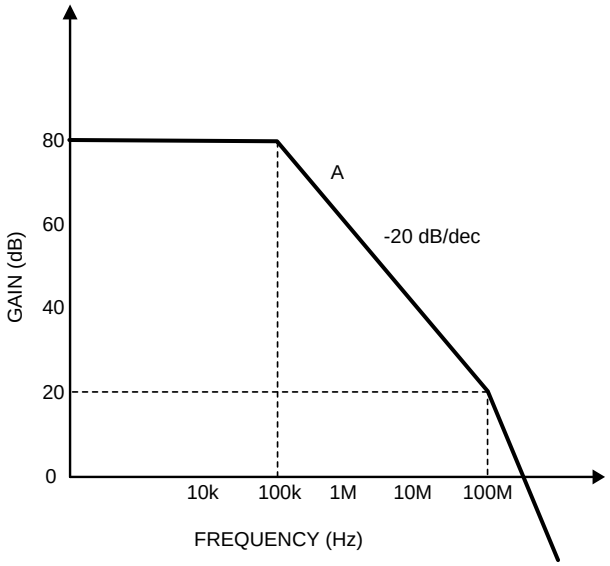

Figure 8. Bode Plot Approximation for National's LMH6624 Op Amp

3.2 Analysis

To maintain a phase margin equal to or greater than 45°, the LMH6624 must be compensated for stability when 1/F is set below 20 dB. Recall that 1/F is related to closed loop gain as defined in Equation 4 and Equation 5.

Figure 9 provides the lead-lag circuit that will be used to compensate the LMH6624.

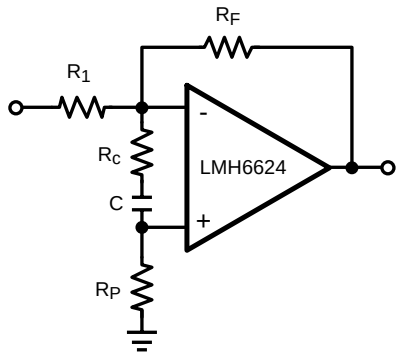

Figure 9. LMH6624 with Lead-Lag Compensation for Inverting Input

The inverse of the feedback factor for this circuit is:

$$\frac{1}{F} = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{1 + s(R_c + R_1 \parallel R_F + R_P)C}{1 + sR_cC}\right) \quad (12)$$

Where $\frac{1}{F}$'s pole is located at $f_p = \frac{1}{2\pi R_cC}$ (13)

and $\frac{1}{F}$'s zero is located at $f_z = \frac{1}{2\pi(R_c + R_1 \parallel R_F + R_P)C}$ (14)

$$\left.\frac{1}{F}\right|_{f=0} = 1 + \frac{R_F}{R_1} \quad (15)$$

$$\left.\frac{1}{F}\right|_{f=\infty} = \left(1 + \frac{R_F}{R_1}\right)\left(1 + \frac{R_P + R_1 \parallel R_F}{R_c}\right) \quad (16)$$

From Equation 12 to Equation 16 the following is evident:

1. The 1/F zero is located at a lower frequency than is the 1/F pole.
2. For low frequencies the value of 1/F is $1 + R_F/R_1$.
3. The intersection point (IP) of 1/F and the open loop gain A is determined by the choice of resistor values for R_P and R_c if the values of R_1 and R_F are set before compensation.
4. This procedure results in the creation of a pole-zero pair, the positions of which are interdependent.
5. This pole-zero pair is used to:
   - Raise the 1/F to a greater gain in the region immediately to the left of its intercept with the A function in order to meet the G_{min} requirement.
   - Achieve the preceding with no additional loop phase delay.

6. The location of the 1/F zero is completely determined once the following conditions are met:
   - The value of 1/F at low frequency is set.
   - The value of 1/F at the intersection point is selected.
   - The location of 1/F's pole is fixed.

Note that the constraint 1/F ≥ G_{min} must be satisfied only in the vicinity of the intersection of A and 1/F ; 1/F can be shaped elsewhere as needed.

Two rules must be satisfied in order to maintain adequate phase margin:

- **Rule 1:** The plot of 1/F should intersect with the plot of open loop gain A at G_{min}. At that point, the open loop gain A has 135° of phase shift. This positioning assures a phase margin of 45°.

  The 45° phase margin intersection point for the LMH6624 is at 100 MHz. The location f_2 in Figure 10 illustrates the proper intersection point for the LMH6624 using the circuit of Figure 9. The intersection of A and 1/F at the op amp's second pole location is the 45° phase margin reference point. To over compensate the amplifier design, the intersection point should be set below the frequency of the op amp's second pole location. This will result in a 1/F value which is greater than G_{min} at the intersection point with open loop gain, A. Remember that G_{min} is the minimum gain for stability specified on the datasheet.
- **Rule 2:** The 1/F pole (see Figure 10) should be positioned at the frequency that is at least one decade below the intersection point of 1/F and A. This positioning takes full advantage of the 90° of phase lead brought about by the 1/F pole.

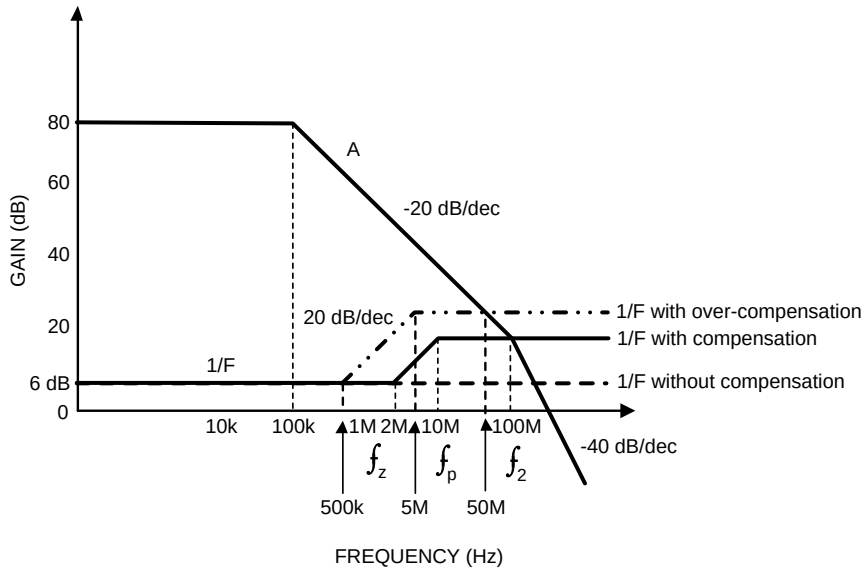

Figure 10. Bode Plots of LMH6624 Open Loop Gain A and 1/F With and Without Compensation

4 Input Lead-Lag Compensation for Inverting Configurations

4.1 Analysis

The input lead-lag compensation method can be applied to a unity gain application using the LMH6624 in an inverting configuration. A gain of one is well below the LMH6624's minimum stable gain of 10 V/V or 20 dB as specified on the datasheet. Without external lead-lag compensation, the inverse of the feedback factor is found by using Equation 3 which applies to both inverting and non-inverting configurations. Unity gain implementation for the inverting configuration means $R_F = R_1$. Therefore, 1/F = 2 V/V or 6 dB, which is shown in Figure 10 as a dashed line.

One effective method of calculating stability is to determine the rate of closure (ROC). This is done by observing the slopes of A and 1/F at their intersection point and deciding the magnitude of their difference. ROC is used to estimate phase margin and therefore stability.

In this example, the rate of closure of the open loop gain A plot and the 1/F = 6 dB plot is 40 dB/dec. The system has less than 45° of phase margin and is unstable.

4.2 Design Example: Procedure

The compensation circuit shown in Figure 9 was implemented and the 1/F function was reshaped as shown by the solid line in Figure 10. The 1/F plot is 6 dB at low frequencies. At higher frequencies, it is made to intersect the open loop gain A at frequency f_2 with gain amplitude of 20 dB. This follows the dictates of **Rule 1**, which was given previously. 20 dB is the minimum gain specified in the manufacturer's datasheet for stability. The 1/F pole f_p is set at one decade below the intersection point as stated in **Rule 2**.

After applying the compensation circuit of Figure 9, the rate of closure is 30 dB/dec. The Bode representation in Figure 10 is an approximation. The actual response of open loop gain A shows a smooth transition with a −30 dB/dec slope at f_2. The resulting system has approximately 45° of phase margin, based upon the fact that the open loop gain's dominant pole and the second pole are more than one decade apart and that the open loop gain has no other pole within one decade of its intersection point with 1/F. If there is a third pole on the open loop gain A at a frequency greater than f_2 and if it occurs less than a decade above that frequency, then there will be an effect on phase margin.

Steps in calculating the values of the compensation components:

1. Use Equation 16 and set 1/F equal to the minimum stable gain. Recall that for the LMH6624 example the minimum gain is 10 V/V or 20 dB. To set the needed relationship between R_P and R_c, choose a value for either R_P or R_c and then calculate the value necessary for the other component.
2. Set the 1/F pole one decade below the intersection point. In the situation where the LMH6624 is used, one decade below the intersection point is 10 MHz. Now use Equation 13 to solve the value for C in relation to R_c.

This method uses Bode plot approximation. For more accuracy, "fine tuning" may be needed to arrive at the most optimum results.

4.3 Design Example: Calculations

As described in Step 1 use Equation 16:

$$\left.\frac{1}{F}\right|_{f=\infty} = \left(1 + \frac{R_F}{R_1}\right)\left(1 + \frac{R_P + R_1 \,||\, R_F}{R_c}\right) = 10 \text{ V/V} \tag{17}$$

Now substitute $R_F/R_1 = 1$ into the equation above since this is a unity gain inverting amplifier, then:

$$R_P + R_1 \,||\, R_F = 4R_c \tag{18}$$

According to Step 2 use Equation 13:

$$f_p = \frac{1}{2\pi R_c C} = 10 \text{ MHz} \tag{19}$$

which leads to:

$$C = \frac{10^{-7}}{2\pi R_c} \tag{20}$$

The range of choices for C, R_c and R_P which will yield combinations that satisfy both conditions specified in Equation 18 and Equation 20 is very broad.

To minimize the possibility of shunt capacitance across high value resistors producing a negative effect on high frequency operation, choose a value of R_F that is below 2 kΩ. If $R_F = R_1 = 2$ kΩ, then $R_F \,||\, R_1 = 1$ kΩ.

A useful method for arriving at acceptable value combinations is to create a spreadsheet of possible choices along with the combinations produced as shown in Table 1. An ascending sequence of choices for R_c is recorded in one column of this table. The adjacent columns are filled in using R_c to calculate the value of R_P according to Equation 18. The value of C is then calculated using Equation 20. According to Equation 18 it is necessary to start with a value of R_c which is larger than one-fourth of the value of $R_1 \,||\, R_F$, otherwise R_P will be negative as shown by the data listed for Design 1.

Table 1. Design Example for Inverting Configuration

Design	R_c (Ω)	R_P(Ω)	C (pF)	Comments
1	160	negative		R_P is negative because R_c is too low
2	340	160	47	
3	590	1.36k	27	
4	1.6k	5.4k	10	

Designs 2, 3, and 4, all produce usable results. It is best to choose those solutions which produce capacitance values which are significantly higher than the parasitic capacitances associated with passive components and board layout. In this example, Design 4 is not the optimum choice because a C of 10 pF starts to approach parasitic capacitance levels. Therefore, Design 2 and Design 3 are viable first choices.

An alternative approach for choosing values for the compensation components is to start with a value of R_P which is equal to the value of $R_1 \,||\, R_F$. This choice replicates standard op amp design practice and helps to reduce DC errors due to input bias current. The drawback is that if the resultant R_P is a high value then it may combine with the input stray capacitance to affect the overall stability of the circuit.

Fine-tuning of the phase margin in the laboratory is recommended for best results. Replacing C with a trimmer capacitor will allow easy fine-tuning of the phase margin and overall circuit response. Note that according to Equation 13 and Equation 14, 1/F 's pole and 1/F 's zero move proportionately. Therefore, replacing C with a trimmer capacitor enables easy fine-tuning by moving the pole and zero values in tandem, while changing the relative position of 1/F's pole to the op amp's second pole.

Figure 11 shows the bench testing results with the component values derived previously.

The top waveform shows ringing and overshoot of almost 50% in the step response when there is no external compensation.

The bottom waveform is the step response using the compensation values from Design 2. The response is reasonably well behaved and the overshoot is less than 10%. Note that the closest 5% standard resistor values have been used instead of the exact values in the table, that is, 330Ω for R_c and 390Ω for R_P.

The waveform in the middle shows the step response when C is reduced to 10 pF. As C is reduced, the relative position between 1/F's pole and the second pole of the op amp's open loop response is less than a decade. With this solution the circuit sees less than the full 90° of phase lead brought by 1/F 's pole. This causes a reduced phase margin and an increased overshoot as observed.

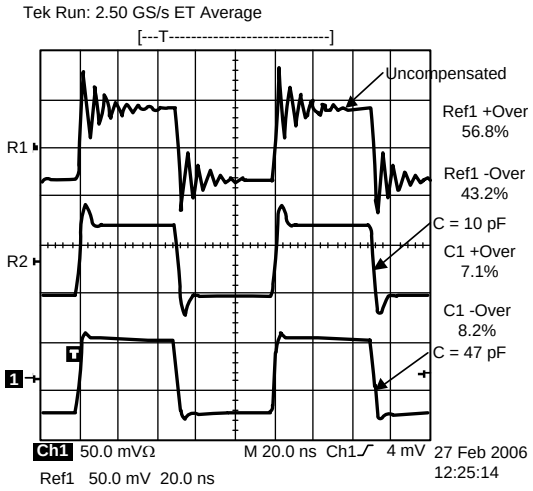

Figure 11. Bench Results for the LMH6624 in an Inverting Configuration

5 Input Lead-Lag Compensation for Non-Inverting Configurations

The overall procedure for calculating compensation values for the non-inverting configuration is very similar to the procedure detailed in Section 4. This section will discuss these minor differences.

In the inverting configuration shown in Figure 9, the non-inverting input is tied to ground via R_P, so that the inverting input is essentially at virtual ground. This is true at least for low frequencies provided the value of R_c is within a certain range of values that will not upset the operation of the virtual ground. In the case of the non-inverting configuration as shown in Figure 12, the summing point (the inverting input) moves with the input signal as long as there is adequate loop gain. Because of this operational difference, the non-inverting configuration may require over-compensation in order to achieve the same level of performance (stability) as that of the inverting configuration.

Overcompensation may be desirable as a means of achieving greater phase margin in an application circuit. Instead of compensating to the particular value indicated on the datasheet for stability – 20 dB minimum for the LMH6624 – choose a value that is greater than G_{min} and repeat the calculations. That is, set G_{min} to 26 dB instead of 20 dB as specified in the previous example for the inverting configuration.

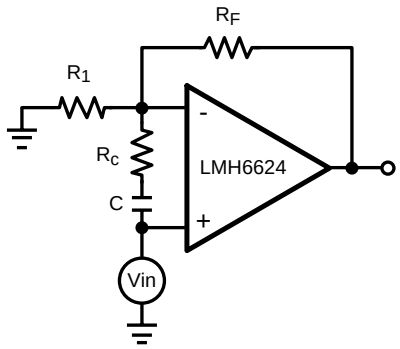

Figure 12. LMH6624 with Lead-Lag Compensation for a Non-Inverting Configuration

Now, let 1/F intersect with A at a value of 26 dB instead of 20 dB. This is shown as the dashed and dotted line in Figure 10.

By shifting the 1/F function to a greater dB value and setting the pole of 1/F at one decade below the intersection point, the total loop phase, which is influenced by the op amp's second pole (among other factors), will be reduced. This produces a greater phase margin when compared to the compensation performance that was achieved in the previous section for the inverting configuration.

To over-compensate the LMH6624:

1. Use Equation 16 and set 1/F to 26 dB. For the non-inverting application of Figure 12, R_P, the input signal equivalent source impedance, is zero. This simplifies Equation 16 for calculating R_c.
2. Recall that the second pole of the LMH6624's open loop gain A occurs at 100 MHz with an open loop gain of 20 dB. The 1/F plot is moved up an additional 6 dB to 26 dB for the over-compensated case. This causes the intersection point of A and 1/F to occur at 50 MHz. Using the one decade rule, set the 1/F's pole at 5 MHz. Solve for the value of C using Equation 13.

A large input resistor should never be applied to the non-inverting input. The low pass filter formed by this large input resistor and the stray capacitance of the op amp slows down the sharp edge of the input. This is especially true for high bandwidth systems.

6 Summary of Input Lead-Lag Compensation

The op amp input and feedback resistor value selection is very important. Without a clear circuit requirement, a large resistor should not be specified. The feedback resistor works with the input stray capacitance to create a pole in the loop gain. Using a larger resistor value will lower the pole frequency. If this pole occurs in the bandwidth of interest, instability may result because of the additional phase lag.

The application of input lead-lag compensation to a decompensated op amp enables the realization of circuit gains of less than the minimum specified by the manufacturer. This is accomplished while retaining the advantageous speed vs. power characteristic of decompensated op amps. The drawback to this method is that the output response may not be as flat as is the response achieved by using the approach of reducing the loop gain described in Section 2.

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