Application Report
SNOA418A–May 2004–Revised May 2013

AN-1234 RSDS Flat Panel Display Design Guidelines Part 1

ABSTRACT

This application report outlines the total system solution that Texas Instruments provides for flat panel displays (FPDs). The described design uses an reduced swing differential signaling (RSDS) interface technology for reduced power, reduced board size, reduced component count, and reduced EMI. This document is currently applicable to XGA and SXGA notebook and monitor applications.

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1 RSDS Schematic and Layout Recommendations

The RSDS bus can provide reliable, low power, low EMI data transmission at rates that exceed the requirements of XGA systems with a 75Hz refresh rate. In order to build the most robust RSDS interface, certain precautions need to be taken. There are three main considerations for an RSDS-based application.

- RSDS Bus Structure
- RSDS Layout
- RSDS Bus Termination

2 RSDS Bus Structure

For XGA and SXGA panels, there are three common RSDS bus structures: the T-configuration, the L-configuration, and the dual bus configuration. All of the bus configurations should be implemented in 50 Ω impedance transmission lines. Each of them require slightly different terminations and supply currents, so picking the appropriate bus configuration is critical to good system design.

2.1 The T-Configuration

Description

In the T-configuration, the timing controller (TCON) is located in the center of the column driver board and the RSDS bus is routed in both directions as shown in Figure 1. The T-configuration is very common for panels with XGA resolution. Ideally, this configuration has the TCON in the center of the board (between column drivers 4 and 5 for an 8 driver XGA system), but it is also acceptable to have the TCON slightly off-center (between column drivers 3 and 4, for example).

Note than even though the RSDS bus connects from the center outward, the SP signal out of the TCON (DIOx into the column driver) must begin at one end of the panel in order to be able to properly daisy-chain the column drivers together. The SP pulse is latched into the column driver on the falling edge of the RSDS clock signal. Even though the SP pulse is a single-ended, TTL level signal that is routed from the end of the panel and the clock pulse is a differential, RSDS signal that is routed from the center of the panel, there is enough timing margin in a robust RSDS bus design to allow for proper latching of the SP pulse.

2.1.1 T-Configuration Termination and RSDS Current

The differential traces for the RSDS bus should each have 50 Ω impedance. The termination between differential pairs at the end of the bus should be 100 Ω. Because the T-configuration has 2 ends of the bus, there must be a termination resistor at each end. These termination resistors, R_{t1} and R_{t2} in Figure 2 should each be 100Ω to minimize reflections and termination related noise on the RSDS bus. The two 100 Ω resistors in parallel result in an effective resistance of 50 Ω on the TCON's RSDS outputs. In order to maintain a 200 mV swing between the differential pair, the RSDS current will have to be increased to approximately 4 mA per pair for a total of 40 mA of RSDS transmission current (4 mA x 10 pairs). For most Texas Instruments TCONs, this is can be accomplished by placing a 5.6 kΩ resistor between the PI pin and ground, but see the data sheet on your particular TCON to determine the correct method of RSDS current control.

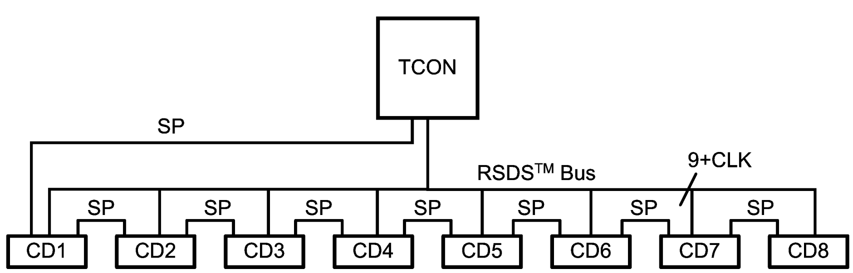

Figure 1. T-Configuration (XGA System)

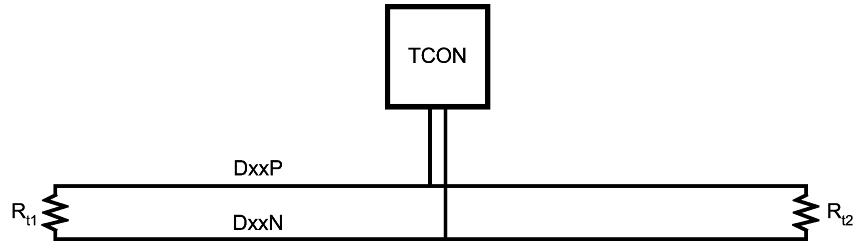

Figure 2. T-Configuration Termination Scheme

2.2 The L-Configuration

Description

In the L-configuration, the TCON is located at one end of the PCB and the RSDS bus is run in one direction across the panel as shown in Figure 3. This configuration is also popular in XGA systems. In an L-configuration, the TCON must be at one end of the column driver chain (either before column driver 1 or after column driver 8 in an XGA system). If the TCON is not at one end of the chain, then the configuration must be treated like a T-configuration. An unterminated stub may cause data errors on the RSDS bus, even if the stub is only a single column driver in length.

2.2.1 L-Configuration Termination and RSDS Current

Because the L-configuration only extends one direction from the TCON, the RSDS bus only needs to be terminated at one end. R_t should be 100 Ω in Figure 4. Because the TCON only sees a single 100 Ω resistor (as opposed to the two parallel 100 Ω resistors of the T-configuration), the RSDS current only needs to be per differential pair in order to maintain an RSDS swing of 200 mV. This results in a total RSDS transmission current of 20 mA. For most of Texas Instruments TCONs, this can be accomplished by placing a 13 kΩ resistor between the PI pin and ground, but check the data sheet on your particular TCON for the appropriate current control method. Because of the lower RSDS current, an L-configuration based panel will consume less power than a T-configuration based panel. The reason that T-configurations are popular is that it is often difficult to place the TCON at one end of the PCB and still maintain the required PCB size.

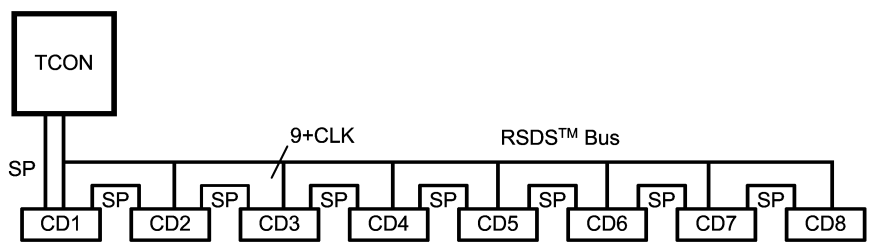

Figure 3. L-Configuration (XGA System)

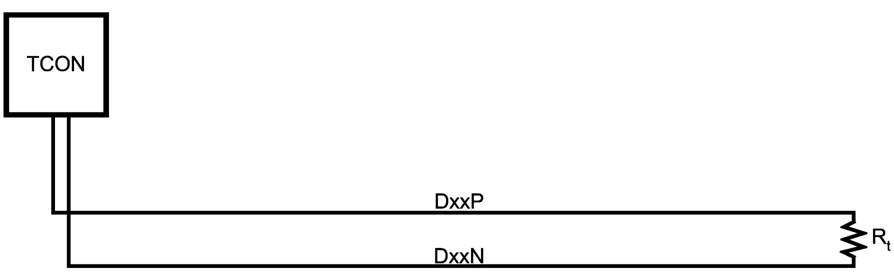

Figure 4. L-Configuration Termination Scheme

2.3 The Dual Bus Configuration

Description

In the dual bus configuration, the TCON is located at the center of the PCB and there are two separate RSDS buses: one that feeds the left half of the column driver chain and the other that feeds the right half as shown in Figure 5. From a PCB routing standpoint, the dual bus configuration looks very similar to the T-configuration, except that the right and left halves of the bus originate at separate pins on the TCON. The dual bus configuration is popular for SXGA and higher resolutions because it reduces the required data rate by a factor of 2 without increasing the bus width. In order to implement the dual bus configuration, an appropriate TCON with dual RSDS outputs must be used. The dual bus configuration currently uses two separate RSDS clocks for the right and left half of the column driver chain. There are also separate right and left half SP pulses.

Unlike the T-configuration, which allows the TCON to be slightly off-center if desired, in dual bus configuration the TCON must be placed exactly in the center of the column driver chain (between column drivers 5 and 6 in a 10 column driver SXGA system). If the TCON were off-center, the right half RSDS bus and the left half RSDS bus would be running at different data rates, and the output buffers of the TCON would have to be reconfigured to output the data in a non-symmetrical manner.

2.3.1 Dual Bus Termination and RSDS Current

Although from a routing standpoint the dual bus configuration resembles the T-configuration, from a termination standpoint, it more closely resembles the L-configuration. The dual bus configuration should be terminated as if it were two separate L-configurations. For each of the RSDS buses, 50 Ω transmission lines should be used, and the buses should be terminated with 100 Ω resistors. In Figure 6, R_{tL} and R_{tR} should be 100 Ω apiece. For each bus, the TCON will see 100 Ω impedance, it will take 2 mA of RSDS current to maintain a 200 mV swing, similar to the 2 mA RSDS current required by the L-configuration. However, because there are two RSDS buses, the total RSDS transmission current will be 40 mA (2 mA x 10 pairs x 2 buses), similar to that of the T-configuration.

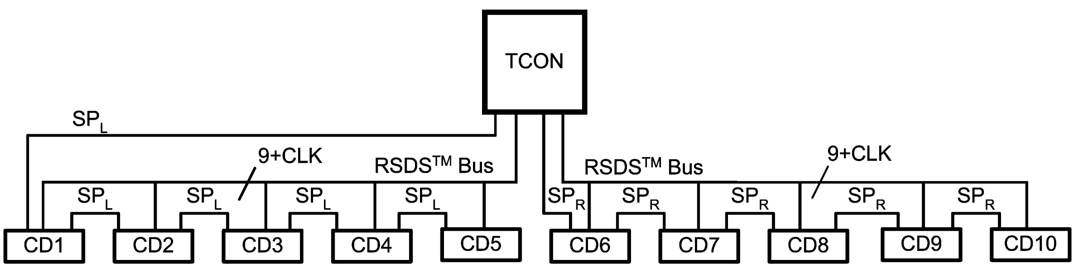

Figure 5. Dual Bus Configuration (SXGA System)

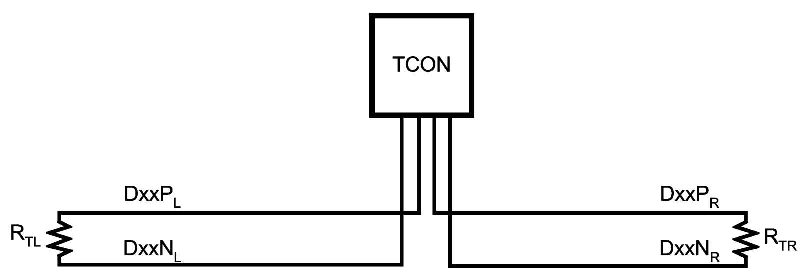

Figure 6. Dual Bus Configuration Termination Scheme

3 RSDS Layout

In general, routing RSDS buses does not require any special considerations outside of normal high speed differential signaling routing practices. The principles and guidelines found here are not specific to Texas Instruments and can be obtained from a wide variety of textbooks and articles on high speed differential signaling.

3.1 Impedance Calculations

The most basic characteristic of the trace is the impedance. It is important to control the impedance of the transmission lines as tightly as reasonably possible in order to minimize the noise due to impedance discontinuities. Texas Instruments recommends using microstrip traces and a solid ground plane on the adjacent layer in order to best control the RSDS bus impedance.

The equations that govern the characteristic impedance for microstrip are shown below. Equation 1 gives the impedance of single-ended trace and Equation 2 gives the corresponding differential impedance. All the equations are based on the dimension definitions shown in Figure 7 with ε_r representing the dielectric constant of the PCB material (typically between 4.0 and 4.5 for FR4). The space between one differential pair and the next should be at least 2s in order to minimize interaction from one pair to the next.

It is recommended that 50 Ω transmission lines be used for all of the RSDS routing.

Although not recommended, if it is necessary to use stripline traces for the RSDS bus, the impedance of the stripline can be calculated using Equation 3 and Equation 4 along with the dimensions defined in Figure 8. Generally, it will be more difficult to control the impedance of a stripline trace than a microstrip trace. Stripline will also be more likely to have other dynamic traces running on the layer either directly above or below the RSDS bus.

$$Z_0 = \frac{60}{\sqrt{0.475\varepsilon_r + 0.67}} \ln\left[\frac{4h}{0.67(0.8w + t)}\right] \text{ in ohms} \quad (1)$$

$$Z_{diff} = 2Z_0\left(1 - 0.48e^{-0.96\frac{s}{h}}\right) \text{ in ohms} \quad (2)$$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4h}{0.67\pi(0.8w + t)}\right] \text{ in ohms} \quad (3)$$

$$Z_{diff} = 2Z_0\left(1 - 0.374e^{-2.9\frac{s}{h}}\right) \text{ in ohms} \quad (4)$$

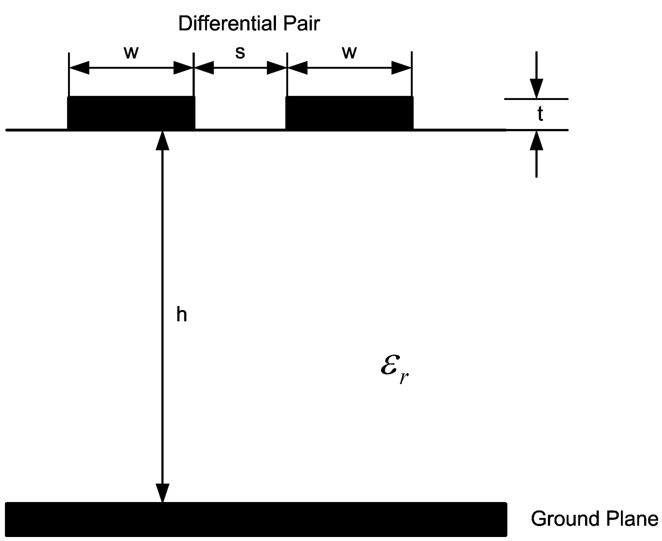

Figure 7. Dimensions for Calculating Microstrip Impedance

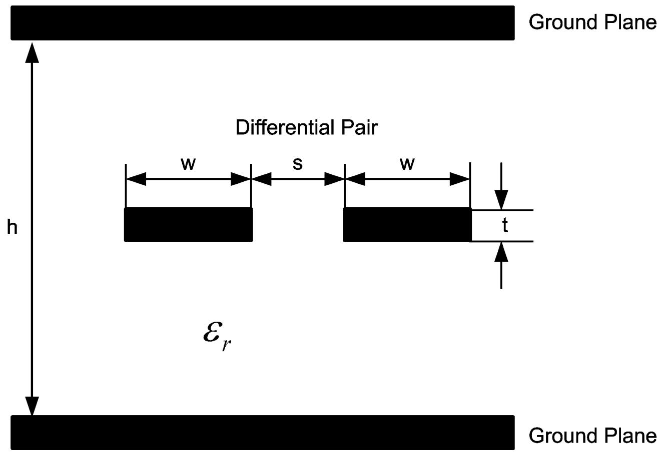

Figure 8. Dimensions for Calculating Stripline Impedance

3.2 General Routing Recommendations

An RSDS bus should be routed and layed-out with the same consideration as any high-speed differential bus. The following are some of the basic high-speed differential routing guidelines.

- Positive and negative traces of a differential pair should be the same length and routed as close together as possible
- Spacing between differential pairs should be double the spacing within a differential pair
- Changing layers along the bus should be minimized
- The number of vias attached to a bus should be minimized
- The bus should be electrically separated from other dynamic signals to minimize noise and cross talk
- Forty-five degree angles should be used instead of right angles when changing the bus direction

A very common approach to routing the RSDS bus is to use a serpentine path on the bottom layer of the PCB. The connection to the column driver is made using vias to top layer traces. An example of the 10 RSDS (9 data and 1 clock) pairs routed in a serpentine configuration is shown in Figure 9. An enlarged view of the RSDS bus and a potential location of the vias to the top layer are shown in Figure 10.

Figure 9 and Figure 10 are examples of practices that have been used in other flat panel displays. The method used in any particular flat panel display can vary quite a bit from these examples. However, the basic routing practices used with high speed differential signaling (such as LVDS or RSDS) should still be observed.

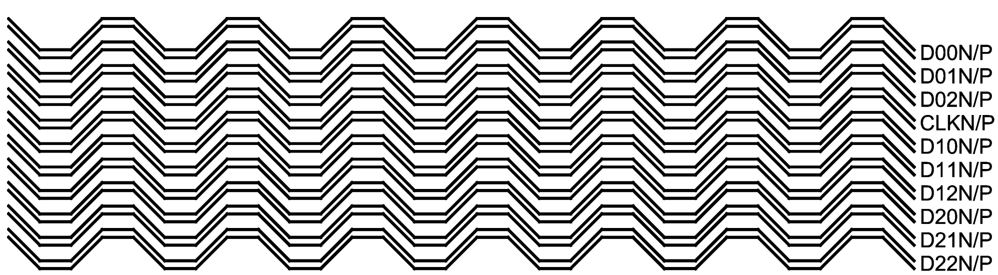

Figure 9. Common RSDS Bus Routing

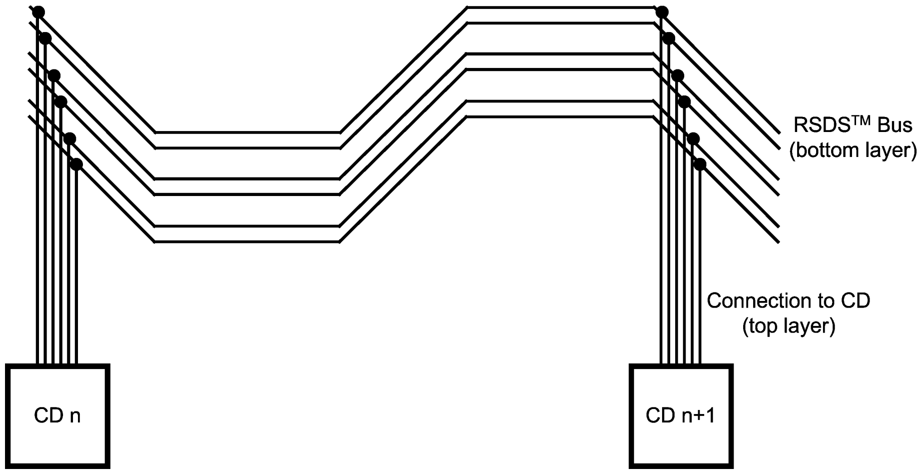

Figure 10. Enlarged View of RSDS Bus Routing

4 RSDS Bus Terminations

Using the general guidelines presented above will result in a robust data transmission scheme in almost all applications. However, the generalizations used are not exactly accurate and there will still be some inefficiency in the termination scheme.

The error is caused by the fact that the RSDS bus is loaded with connections to 8 or 10 column drivers, each of which can be approximated by a capacitive load on the bus line (typically 2-5pF per connection). The generic equations given above do not account for a loaded bus. Figure 11 shows an L-configuration with the column driver capacitive loading included. The net result of the capacitive loading is to decrease the effective impedance of the traces. In order to better match the reduced impedance, the termination resistor (R_t in the figure) may have to be lowered. Empirical evidence indicates that the termination resistor should be around 70Ω in order to provide the best impedance match to the differential traces. Equation 5 gives the equation used to calculate the single ended impedance of a loaded transmission line where Z_0 is the impedance of the unloaded trace, C_D is the capacitance per unit length on the trace, and T_D is the intrinsic propagation delay of the trace. C_D and T_D for microstrip and stripline traces are given in Equation 6, Equation 7, and Equation 8. The differential impedance for a loaded bus can be calculated from Equation 2 and Equation 4 by substituting Z_0' for Z_0.

$$Z_0' = \frac{Z_0}{\sqrt{\frac{C_D Z_0}{T_D} + 1}} \text{ in ohms} \quad (5)$$

$$C_D = \frac{(\#\,of\,CD) * (C\,per\,CD\,in\,pF)}{bus\,length\,(cm)} \text{ in pF/cm} \quad (6)$$

$$T_D = 33.36\sqrt{0.475\varepsilon_r + 0.67} \text{ in ps/cm for microstrip} \quad (7)$$

$$T_D = 33.36\sqrt{\varepsilon_r} \text{ in ps/cm for stripline} \quad (8)$$

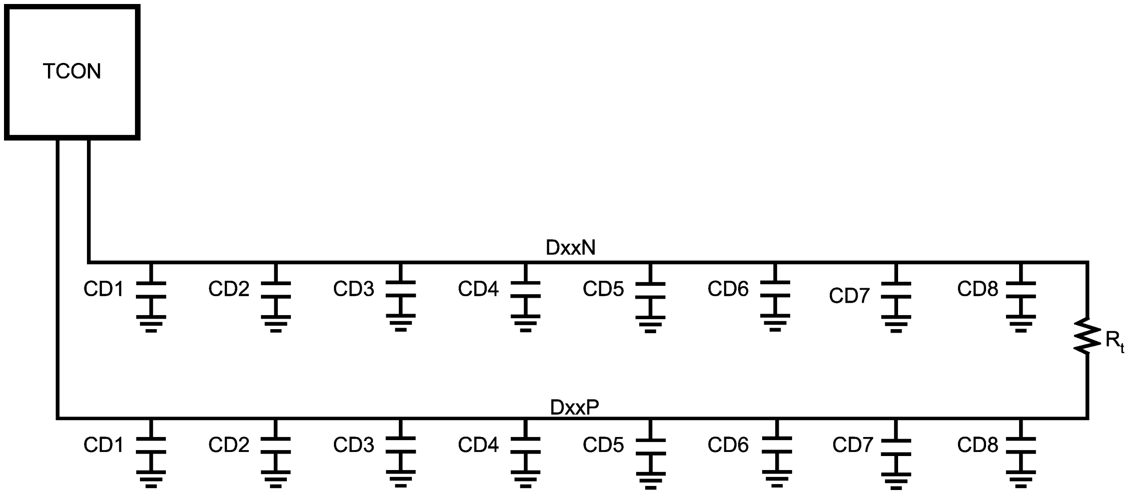

Figure 11. Loading of RSDS Bus

5 Printed Circuit Board Recommendations

The printed circuit board and layout used can vary greatly from application to application. The following is simply a PCB layout that has been implemented on several flat panel displays currently in production. The assumption is that the available PCB is a 4-layer FR4 board. A recommended layer stack-up is shown in Figure 12. The stack-up shows the bottom layer being used only for the RSDS bus routing. The layer immediately above the RSDS bus is a solid ground plane, ideally only broken when it is necessary to route signals between layers. The second layer from the top can be used for the remainder of the power routing and all of the TTL based control signals. The top layer is mainly used for component connections and brief routing.

Figure 13 shows how the components may be placed on a PCB for a typical T-configuration in an XGA design. The TCON would be approximately in the center, the power circuitry (DC-DC converter, tap point buffers, VCOM buffer, and so forth) are located next to the TCON, and the bottom half of the board is available for column driver connections and RSDS terminations. This is just an example that is meant to illustrate the average board. Many designs have been optimized to meet the space requirements of the particular application and have either smaller PCBs or PCBs with a different outline or component positioning.

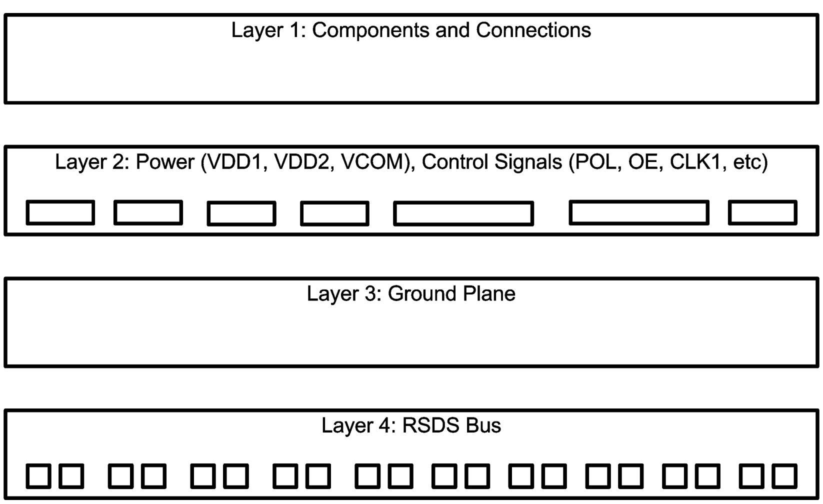

Figure 12. Recommended Layer Stack-up (traces into/ out of paper)

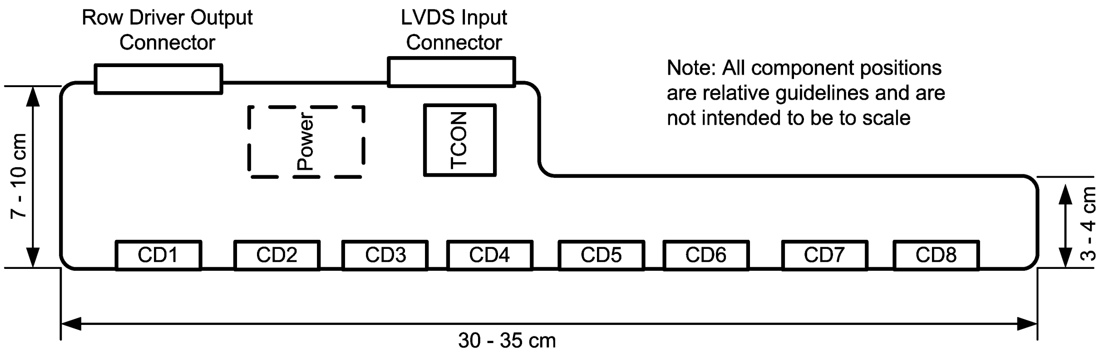

Figure 13. Typical PCB Size and Functional Grouping

6 Timing Controller

Texas Instruments provides customized timing controller solutions based on a standard chassis. These customized TCONs are designed to meet the custom requirements of individual applications without the typical design cycle time of a custom IC. For more information on taking advantage of National's custom TCONs, please contact your local Texas Instruments representative.

In addition to the custom requirements, there are a number of standard functional blocks that are included in almost every Texas Instruments TCON and flat panel display.

6.1 LVDS Interface

The main interface into a Texas Instruments TCON uses low voltage differential signaling (LVDS). LVDS is a standardized interface (ANSI/TIA/EIA-644-A) that provides the basis for both TI’s FPD-Link interface as well as open LVDS display interface (OpenLDI). Both FPD-Link and OpenLDI were developed by Texas Instruments to improve the power, EMI, and quality of the interface between the host and the display.

Proper termination of the LVDS interface is critical to maintaining signal integrity across the interface cabling. The LVDS bus consists of a differential clock and four differential pairs for single bus applications and eight differential pairs for dual bus applications. The LVDS signals should be terminated with a 100 Ω resistor between the positive and negative signals.

6.2 Power Supply Decoupling

In order to reduce noise within the IC, most of Texas Instruments TCONs use at least two separate power supplies and numerous power supply pins. It is recommended that every power supply pin should have its own decoupling capacitor as close as possible to the pin, and at least one of the power supply pins of each type should have multiple decoupling capacitors attached. A good default capacitor value is 0.1 µF, and if multiple capacitors are to be attached, it may help to have a range of values. Three capacitors of 100 pF, 0.1 µF, and 22 µF will work well for most applications.

6.3 Timing Definitions

Texas Instruments can create a custom TCON that meets your timing requirements without the need for external EEPROM coding or additional components on the PCB. For further information about developing a custom TCON, contact your Texas Instruments representative.

It is a good practice to transition as many of the TTL signals as possible during the horizontal blanking time. This will assure that there will be no corruption of the RSDS data due to coupling effects. In most applications, there is enough horizontal blanking time to transition the POL, OE, and STV pulses.

7 Column Driver

There are three main areas to look at when connecting the column drivers to the rest of the circuitry. These recommendations are meant for Texas Instruments FPD33684, FPD33584, and FPD33620 column drivers. To determine the applicability of these recommendations to one of Texas Instruments other column drivers, please contact your Texas Instruments representative.

7.1 RSDS Connection

The RSDS connection has been described in detail above. For the column driver, the main goal is to keep the stub length from the RSDS bus to the column driver as short as possible. Typically, anything less than 1.5cm is considered acceptable.

7.2 DIOx Connections

In order to daisy-chain the column drivers together, the output DIOx pin of one column driver must be connected to the input DIOx pin of the next column driver. The DIOx signal is latched in on the falling edge of the RSDS clock. The connection from one DIOx pin to the next should be as short and direct as possible to avoid adding any unnecessary propagation delay in the signal path.

7.3 Power Supply Decoupling

Like the timing controller, the column driver should have decoupling capacitors located as close as possible to each of the power pins. Typically, a 0.1µF capacitor on each power pin will meet the decoupling needs of the system.

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