Application Report
SNOA401R–September 2000–Revised May 2013

AN-1187 Leadless Leadframe Package (LLP)

ABSTRACT

This application report discusses the Leadless Leadframe Package (LLP).

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1 Introduction

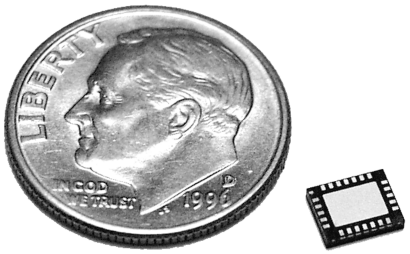
The Leadless Leadframe Package (LLP) is a leadframe based chip scale package (CSP) that may enhance chip speed, reduce thermal impedance, and reduce the printed circuit board area required for mounting. The small size and very low profile make this package ideal for high density PCBs used in small-scale electronic applications such as cellular phones, pagers, and handheld PDAs. The LLP package is offered in the Pullback and no Pullback configuration. In the Pullback configuration the standard solder pads are offset from the edge of the package by 0.1 mm. In the no Pullback configuration the standard solder pads extend and terminate at the edge of the package. This feature offers a visible solder fillet after board mounting.

The LLP has the following advantages:

- Low thermal resistance
- Reduced electrical parasitics
- Improved board space efficiency
- Reduced package height
- Reduced package mass

JEDEC Registration Information:

- Quad LLP Packages: MO-220
- Dual-in-line LLP Packages: MO-229



2 Package Overview

2.1 Key Attributes

- Construction of the LLP is Illustrated in Figure 1, Figure 2, and Figure 3.
- Terminal contacts:
  - The contact pads (or solder pad) are located peripherally in single row format depending on the specific number of pins and body size.
  - For certain specific applications, the packages are incorporated with common power and/or ground pins as shown in Figure 9.
  - All LLP contacts are plated with 85Sn/15Pb solder for ease of surface mount processing.
  - All Lead-Free LLP contacts are plated with matte tin solder for ease of surface mount processing.
- Printed Circuit Board (PCB) footprint:
  - Soldering the exposed die attach pad (DAP) to the PCB provides the following advantages:
    - Optimizes thermal performance.
    - Enhances solder joint reliability.
    - Facilitates package self alignment to the PCB during reflow.
- The LLP is offered in either dual-in-line (DIP) or quad configuration, and Pullback or No Pullback terminal contact designs.
- The LLP package also comes in different thicknesses. 0.8mm is the most prevalent thickness but the package is selectively available also in 0.6mm and 0.4mm thickness.

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- Coplanarity is not an area of concern for this package.
  - All LLP contacts are flush with the bottom of the package.
- Moisture Sensitivity Level (MSL).
  - MSL of specific applications, requiring large packages, may vary depending on die size, exposed DAP design, and number of downbonds.
- The LLP package with solder bumps is also offered in the Pullback option only. The bump LLP does not require a solder printing process during SMT. It can be mounted by flux dipping / dispensing to the PCB board and reflow. The solder bump on the package will melt and form the solder joint between the package and PCB board.

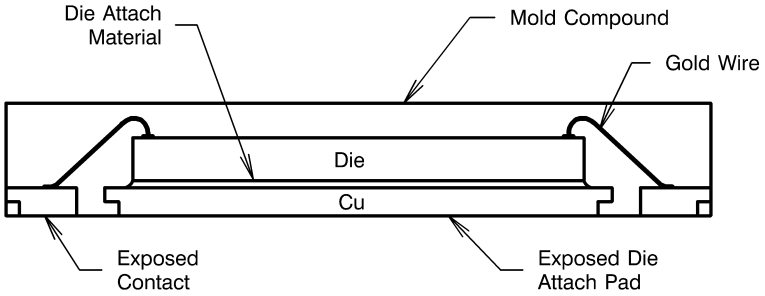

Figure 1. Pullback LLP Configuration

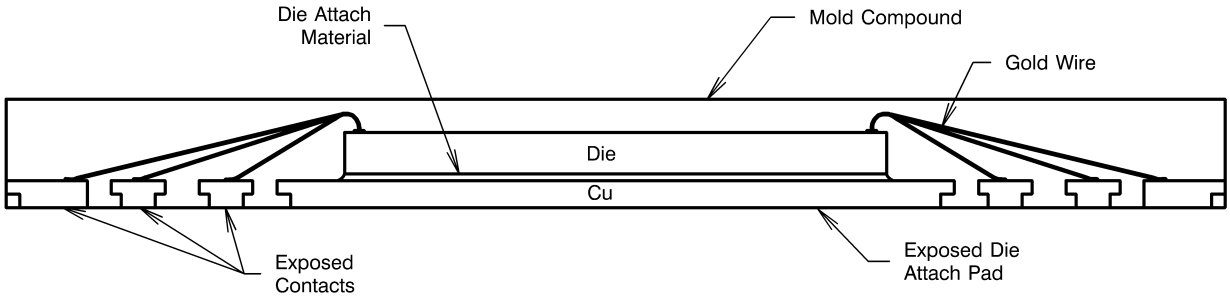

Figure 2. Pullback LLP Configuration with Power and Ground Rings

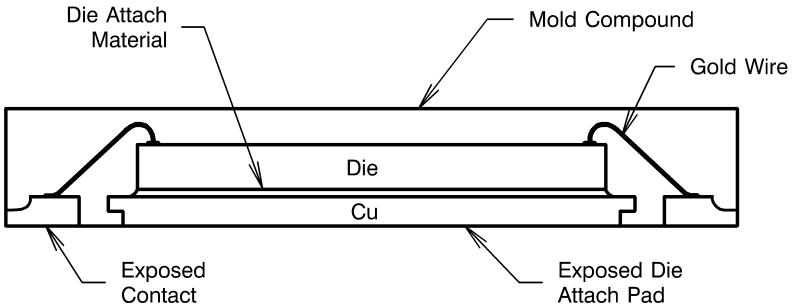

Figure 3. No Pullback LLP Configuration

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2.2 Package Offering

Table 1. Package Offering

Number	I/O Count	Body size (mm)	Terminal Pitch (mm)	Marketing Drawing
Pullback (DUAL)				
1	6	2.2 × 2.5	0.65	LDB06A
2	6	3 × 4	0.8	LDC06D
3	6	2.92 × 3.29	0.95	LDE06A
4	8	3 × 3	0.5	LDA08A
5	8	2.5 × 2.5	0.5	LDA08B
6	8	2.5 × 3	0.5	LDA08C
7	8	4 × 4	0.8	LDC08A
8	10	3 × 3	0.5	LDA10A
9	10	3 × 4	0.5	LDA10B
10	10	4 × 4	0.8	LDC10A
11	10	6 × 6	1.0	LDD10A
12	14	4 × 4	0.5	LDA14A
13	14	4 × 5	0.5	LDA14B
14	14	4 × 3	0.5	LDA14C
15	14	5 × 6	0.8	LDC14A
16	16	5 × 5	0.5	LDA16A
Pullback (QUAD)				
1	8	2 × 2	0.65	LQB08A
2	10	5 × 4	0.8	LQC10A
3	16	4 × 4	0.5	LQA16A
4	20	4 × 4	0.5	LQA20A
5	24	5 × 4	0.5	LQA24A
6	24	6 × 6	0.8	LQC24A
7	28	5 × 5	0.5	LQA28A
8	32	6 × 5	0.5	LQA32B
9	32	6 × 6	0.5	LQA32A
10	36	6 × 6	0.5	LQA36A
11	36	6 × 6	0.5	LQA36B
12	44	7 × 7	0.5	LQA44A
13	44	7 × 7	0.5	LQA44B
14	48	7 × 7	0.5	LQA48B
15	56	9 × 9	0.5	LQA56A
16	68	10 × 10 (PUNCH)	0.5	LQA68A
No Pullback (DUAL)				
1	4	1.5 × 1.5	1.0	SDD04A
2	6	2.2 × 2.5	0.65	SDB06A
3	6	3 × 3	0.95	SDE06A
4	8	2.5 × 2.5	0.5	SDA08B
5	8	2.5 × 3	0.5	SDA08C
6	8	3 × 3	0.5	SDA08A
7	8	4 × 4	0.8	SDC08A
8	10	3 × 3	0.5	SDA10A
9	10	4 × 4	0.8	SDC10A
10	12	3 × 3	0.4	SDF12A
11	14	4 × 3	0.5	SDA14A

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Table 1. Package Offering (continued)

Number	I/O Count	Body size (mm)	Terminal Pitch (mm)	Marketing Drawing
12	14	4 × 4	0.5	SDA14B
13	16	4 × 3	0.4	SDF16A
14	16	4 × 5	0.5	SDA16B
15	16	5 × 5	0.5	SDA16A
No Pullback (QUAD)				
1	16	4 × 4	0.5	SQA16A
2	16	4 × 4	0.65	SQB16A
3	20	3 × 3	0.4	SQF20A
4	24	4 × 4	0.5	SQA24A
5	24	5 × 4	0.5	SQA24B
6	28	5 × 5	0.5	SQA28A
7	32	5 × 5	0.5	SQA32A
8	36	6 × 6	0.5	SQA36A
9	38	7 × 4.5	0.5	SQA38A
10	40	5 × 5	0.4	SQF40A
11	40	6 × 6	0.5	SQA40A, SQA40B
12	48	6 × 6	0.4	SQF48A, SQF48B
13	48	7 × 7	0.5	SQA48A, SQA48B, SQA48C, SQA48D
14	54	10 × 5.5	0.5	SQA54A
15	60	7 × 7	0.4	SQF60A
16	60	9 × 9	0.5	SQA60A, SQA60B
17	64	9 × 9	0.5	SQA64A
18	80	12 × 12	0.5	SQA80A
No Pullback 0.6 mm Thin (QUAD)				
1	8	2 × 2	0.5	SPA08A
2	20	3 × 3	0.4	SPF20B
3	28	5 × 5	0.5	SPA28A
4	48	7 × 7	0.5	SPA48A
5	52	8 × 8	0.5	SPA52A
No Pullback 0.4 mm Ultra Thin (QUAD)				
1	28	5 × 5	0.5	SNA28A
2	40	6 × 6	0.5	SNA40A
3	48	7 × 7	0.5	SNA48A
4	48	6 × 6	0.4	SNF48A
Pullback with Solder Bump (DUAL)				
1	6	2.92 × 2.92	0.95	YDE06A
2	6	3 × 4	0.8	YDC06B
3	8	3 × 3	0.5	YDA08A
4	10	3 × 3	0.5	YDA10A
Pullback with Solder Bump (QUAD)				
1	24	4 × 5	0.5	YQA24A

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3 PCB Design Recommendations

3.1 NSMD VS. SMD Land Pattern

Two types of land patterns are used for surface mount packages:

- Non-Solder Mask Defined Pads (NSMD)
- Solder Mask Defined Pads (SMD)

NSMD has an opening that is larger than the pad, whereas SMD pads have a solder mask opening that is smaller than the metal pad. Figure 4 Illustrates the two different types of pad geometry.

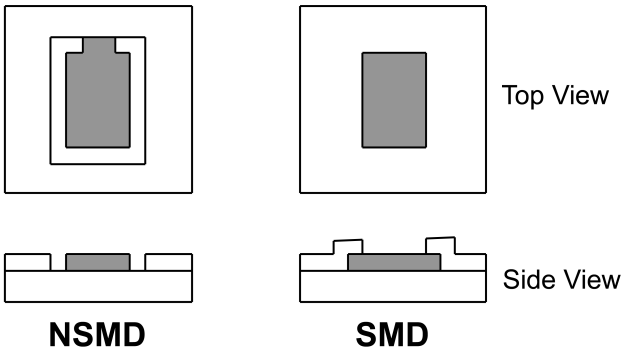

Figure 4. NSMD and SMD Pad Geometry

NSMD is preferred because the copper etch process has tighter control than the solder masking process. Moreover, the smaller size of the copper pad in the NSMD definition facilitates escape routing on the PCB when necessary.

NSMD pads require a ±0.075 mm (3 mils) clearance around the copper pad for mask registration tolerances.

SMD pad definition can introduce stress concentration points near the solder mask on the PCB side. Extreme environmental conditions such as large temperature variations may cause fatigue that leads to cracked solder joints and reliability problems.

For optimal reliability, Texas Instruments recommends a 1:1 ratio between the package pad and the PCB pad for the Pullback LLP. If probing of signal pad is required, it is recommended to design probe pads adjacent to signal pads as shown in Figure 5. The trace between the signal pad and the probe pad must be covered by solder mask.

For No Pullback LLP, we recommended the PCB terminal pads to be 0.2mm longer than the package pads to create a solder fillet to improve reliability and inspection, as shown in Figure 6.

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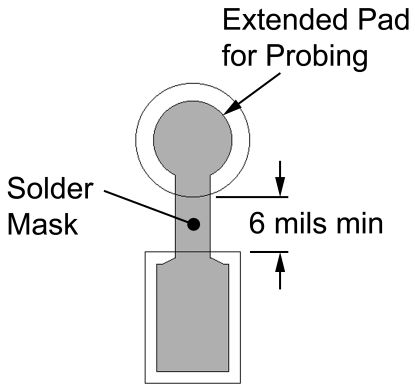

Figure 5. Recommended Pad Design for Probing

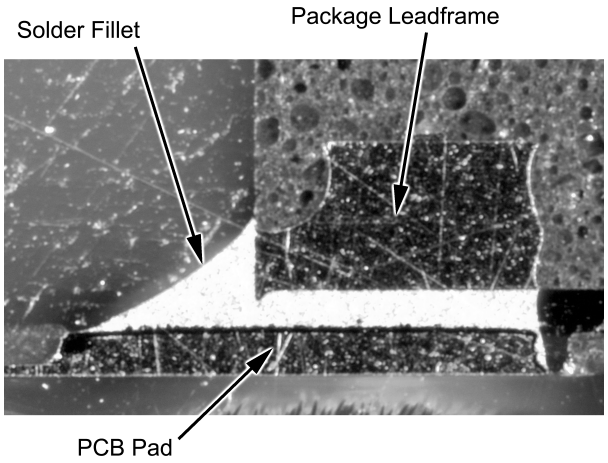

Figure 6. X-section of NO Pullback Solder Joint with Fillet

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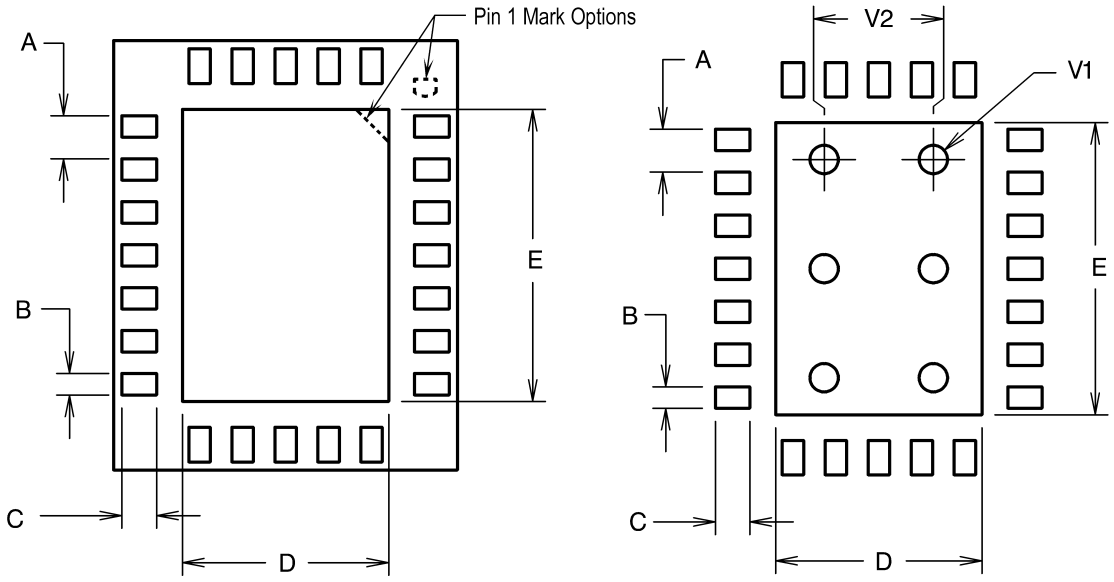

Dimensions A, B, C, D, and E of PCB are 1:1 ratio with package pad dimensions. For specific detailed package dimensions refer to respective marketing outlines.	
Terminal Pitch	A
Terminal Width	B
Terminal Length	C
Exposed DAP Width	D
Exposed DAP Length	E
Thermal Via Diameter. Recommended 0.2 - 0.33 mm	V1
Thermal Via Pitch. Recommended 1.27 mm	V2

Figure 7. Typical Recommended Printed Circuit Board for Pullback Packages

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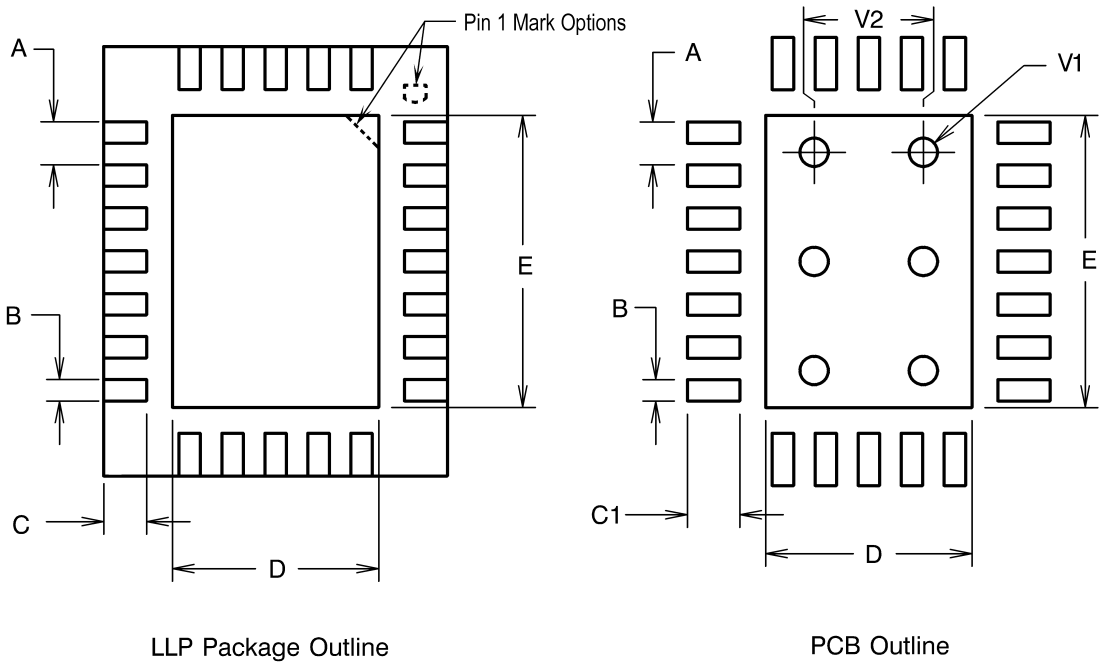

Dimensions A, B, D, and E of PCB are 1:1 ratio with package pad dimensions. For specific detailed package dimensions refer to respective marketing outlines.	
Terminal Pitch	A
Terminal Width	B
Terminal Length	C
PCB Pad Length C + 0.2 mm	C1
Exposed DAP Width	D
Exposed DAP Length	E
Thermal Via Diameter. Recommended 0.2 - 0.33 mm	V1
Thermal Via Pitch. Recommended 1.27 mm	V2

Figure 8. Typical Recommended Printed Circuit Board for No Pullback Packages

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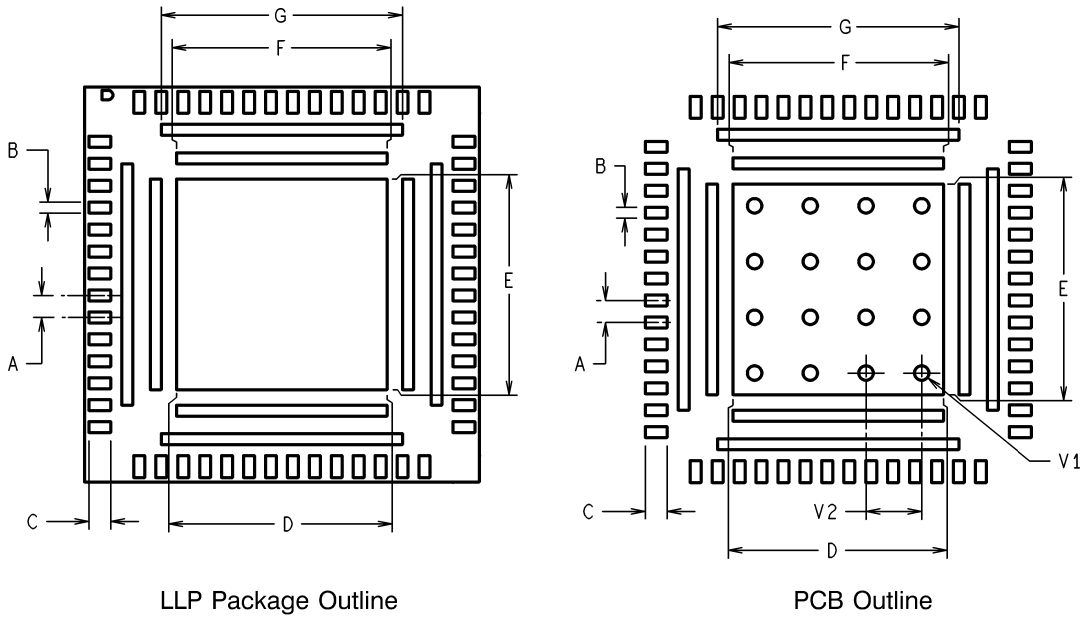

Dimensions A, B, C, D, E, F and G of PCB are 1:1 ratio with package pad dimensions. For specific detailed package dimensions refer to respective marketing outlines.	
Terminal Pitch	A
Terminal Width	B
Terminal Length	C
Exposed DAP Width	D
Exposed DAP Length	E
Ground Bar	F
Power Bar	G
Thermal Via Diameter	V1
Thermal Via Pitch	V2

Figure 9. Typical Recommended Printed Circuit Board for Pullback Packages with Ground and Power Bars

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3.2 Thermal Design Considerations

3.2.1 Thermal Land

The LLP thermal land is a metal (normally copper) region centrally located under the package and on top of the PCB. It has a rectangular or square shape and should match the dimensions of the exposed pad on the bottom of the package (1:1 ratio).

For certain high power applications, the PCB land may be modified to a "dog bone" shape that enhances thermal performance. The packages used with the "dog bone" lands will be a dual inline configuration. (See Figure 10).

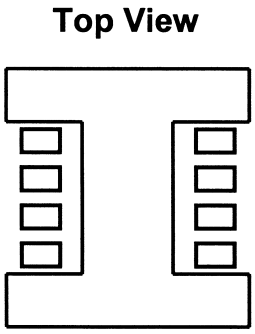

Figure 10. Dog Bone

3.2.2 Thermal Vias

Thermal vias are necessary. They conduct heat from the exposed pad of the package to the ground plane. The number of vias is application specific and is dependent upon electrical requirements and power dissipation.

An array of vias with a 1.27 mm pitch is shown in Figure 7. The via diameter should be 0.2 mm to 0.33 mm with 1oz. copper via barrel plating. It is important to plug the via to avoid any solder wicking inside the via during the soldering process. The thermal vias can be tented with solder mask on the top surface of the PCB. The solder mask diameter should be at least 75 microns (or 3 mils) larger than the via diameter. The solder mask thickness should be the same across the entire PCB.

A package thermal performance may be improved by increasing the number of vias. Figure 11 shows such effect for a 36L LLP with a 9 × 9 mm body and 7 × 7 mm pad. Two via diameters are illustrated, namely, 0.2 and 0.33 mm. Different patterns are also shown to depict possible layouts for specific numbers of vias. Two die sizes are shown in this example, 2.1 × 2.1 mm and 6.4 × 6.4 mm. For a given number of vias, placing the vias toward the periphery of the pad provides up to 5% improvement over centrally placed vias. There is diminishing improvement, however, as the number of vias increases beyond a critical number – 16 in this example.

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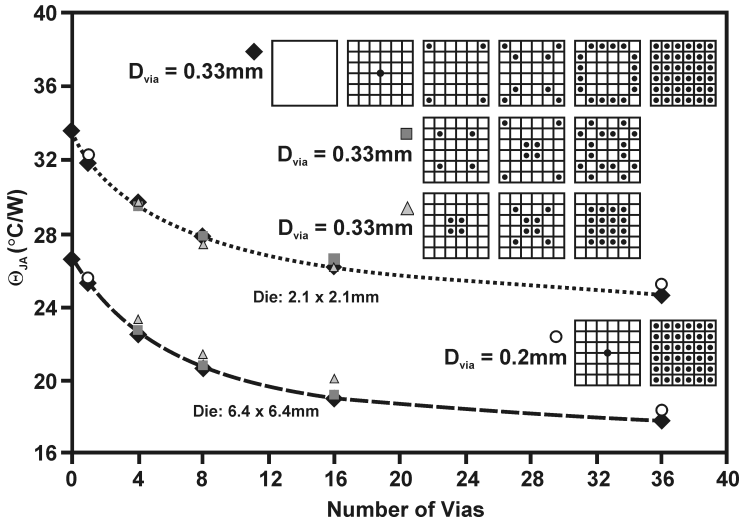

Figure 11. θ_{JA} vs. Number, Distribution and Diameter of Thermal Vias and Die Sizes for 36L LLP with 9 × 9 mm Body and 7 × 7 mm Pad

3.2.3 Effects of Solder Voids

A void in the solder joint (generated during the manufacturing process) could have a direct impact on heat dissipation. The effect is not significant unless the void volume exceeds a certain percentage of the corresponding material volume (see Figure 12).

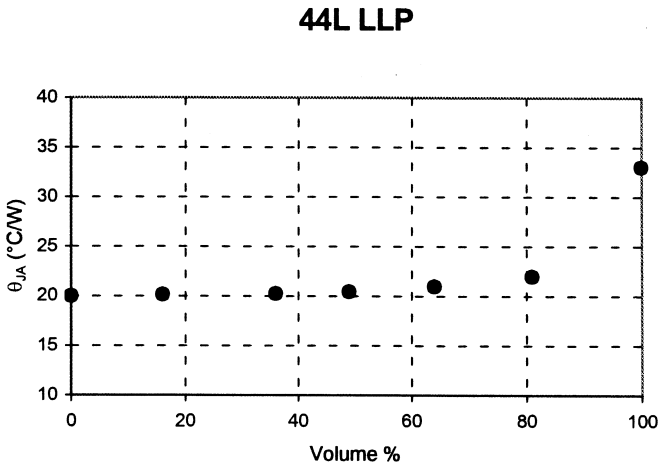

Figure 12. Thermal Voids Impact

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3.2.4 Thermal Layers in the PCB

Because of the small size and low profile, the majority of heat generated by the die within the LLP is dissipated through the exposed pad to PCB. Consequently, the PCB configuration and metal layers embedded in the PCB become important to achieve good thermal performance. In a 4-layer PCB (2 layers for signals and 2 layers for power/ ground), the area of the embedded copper layer connecting to the thermal vias has significant effect on the thermal performance of the package. Figure 13 shows simulation data of θ_{JA} vs. the embedded copper layer area for the 44L LLP. Increasing the copper layer area reduces the thermal resistance. However, in the similar manner, as the number of vias increases, the amount of thermal resistance improvement diminishes as the embedded copper area increases.

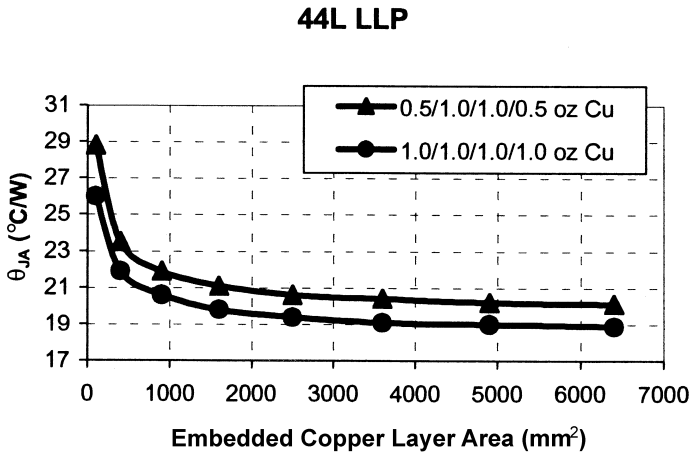

Figure 13. Effect of Thermal Layers on the LLP's Junction-to-Ambient Thermal Resistance

3.2.5 Theta JA on 4L and 2L JEDEC Boards

θ_{JA} is strongly dependent on the board on which packages are mounted. θ_{JA} of LLP packages on 4L JEDEC board with vias and 2L JEDEC boards are simulated and illustrated in Figure 14, Figure 15, Figure 16, and Figure 17, respectively.

The maximum via number is used when doing the simulation. LLP packages are classified into different groups (shown as rectangular bands) according to body size. For each body size, two pad sizes with largest and smallest areas are selected. For each pad size, two die sizes with the same as and one fourth of the exposed pad area are selected. This is shown by the inserts in Figure 14 through Figure 17.

As an example, consider Figure 14 depicting θ_{JA} values for six body sizes (2.5 × 2.5 mm, 2.5 × 3 mm, 3 × 3 mm, 2.92 × 3.29 mm, 3 × 4 mm, and 4 × 4 mm). The 2.5 × 3 body size shows the following θ_{JA} values at the four corners: 70.5°C/W for a die of the same size as a pad of 1.75 mm^2 (lower left corner of 2.5 × 3 block); 98°C/W for a die ¼ the area of a pad of 1.75 mm^2 (upper left corner of 2.5 × 3 block); 84°C/W for a die ¼ the area of a pad of 2.4 mm^2 (upper right corner of 2.5 × 3 block); 62.5°C/W for a die of the same size as the area of a pad of 2.4 mm^2 (lower right corner of 2.5 × 3 block). Die and pad size combinations falling within this 2.5 × 3mm body block will exhibit θ_{JA} values covered by this block.

When the body, pad and die sizes of a LLP package are given, the corresponding block can be used to get a quick evaluation for its θ_{JA} by interpolation according to pad and die sizes. It is noted that due to the nonlinear variation of θ_{JA} with pad sizes, die sizes, and I/O number, the θ_{JA} values in Figure 14 through Figure 17 may involve up to 15% error. If more accurate data are expected, a separate simulation or experimental test is necessary.

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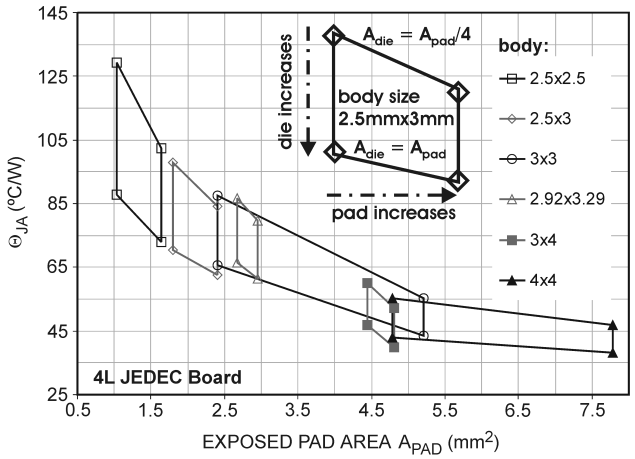

Figure 14. θ_{JA} vs. Body, Pad and Die Sizes for 4L JEDEC Board

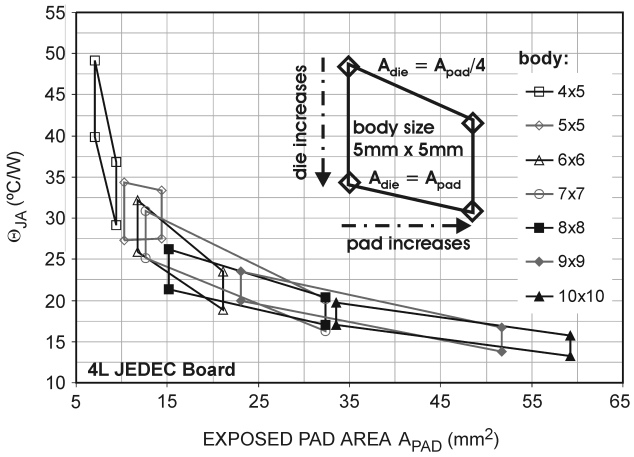

Figure 15. θ_{JA} vs. Body, Pad and Die Sizes for 4L JEDEC Board

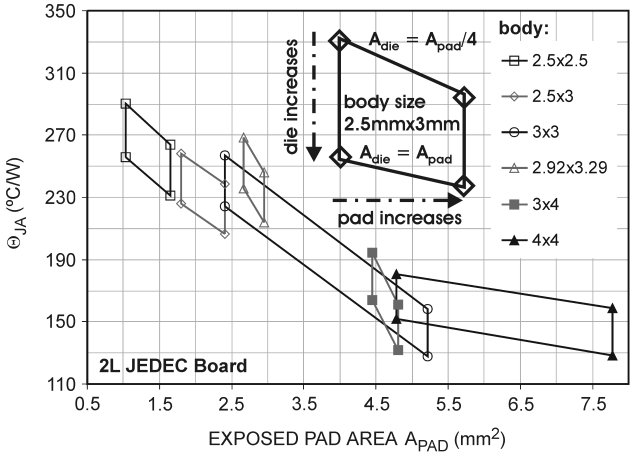

Figure 16. θ_{JA} vs. Body, Pad and Die Sizes for 2L JEDEC Board

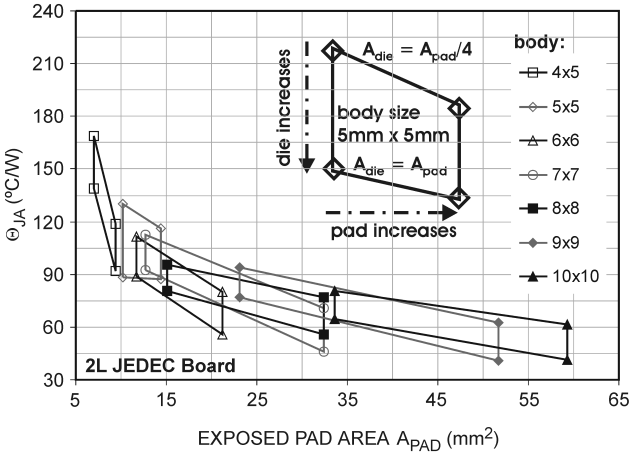

Figure 17. θ_{JA} vs. Body, Pad and Die Sizes for 2L JEDEC Board

4 SMT Assembly Recommendations

The LLP surface mount assembly operations include:

- PCB plating requirements
- Screen printing the solder paste on the PCB
- Monitor the solder paste volume (uniformity)
- Package placement using standard SMT placement equipment
- X-ray pre reflow check - paste bridging
- Reflow and cleaning (dependent upon the flux type)
- X-ray post reflow check - solder bridging and Voids

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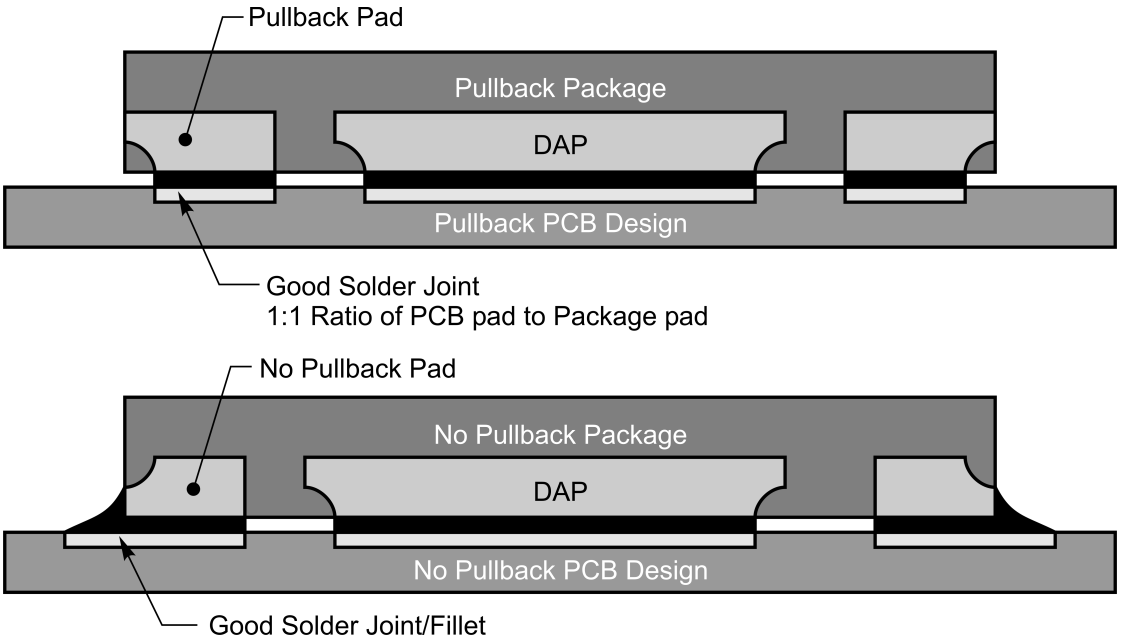

Figure 18. Recommended PCB Design

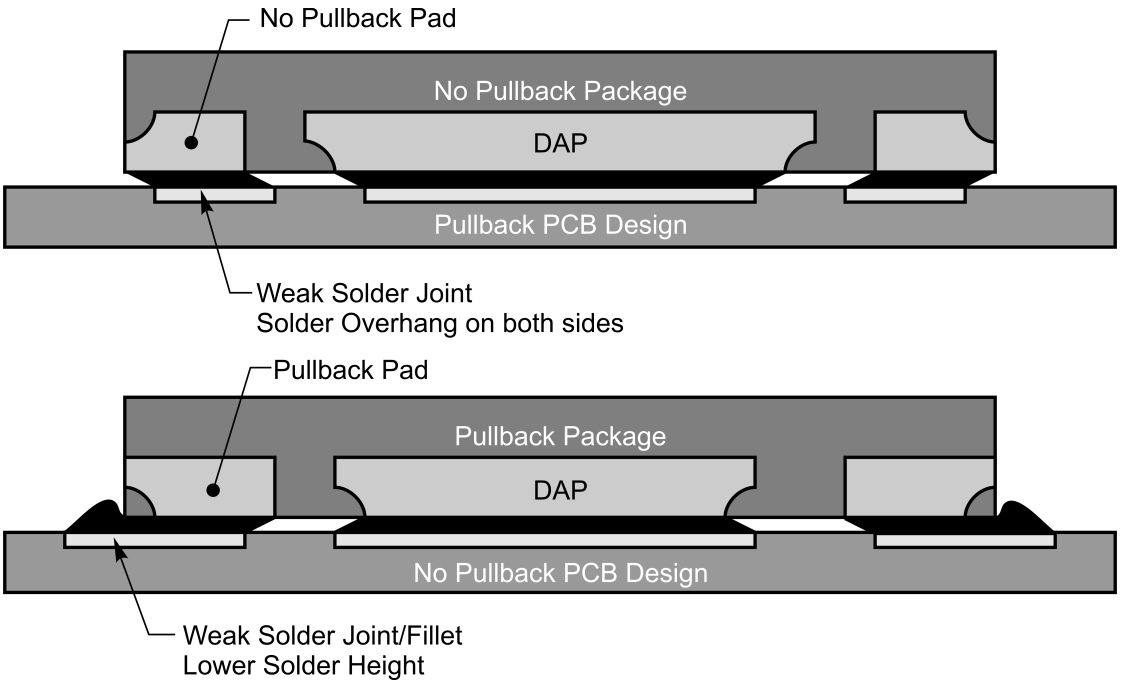

Figure 19. Not Recommended PCB Design

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4.1 PCB Surface Finish Requirements

A uniform PCB plating thickness is key for high assembly yield.

- For an electroless nickel immersion gold finish, the gold thickness should range from 0.05 µm to 0.20 µm to avoid solder joint embrittlement.
- Using a PCB with **O**rganic **S**olderability **P**reservative coating (OSP) finish is also recommended, as an alternative to Ni-Au.
- For a PCB with Hot Air Solder Leveling (HASL) finish, the surface flatness should be controlled within 28 micron.

4.2 Solder Stencil

This recommendation is not applicable to Bump LLP. Bump LLP requires flux dipping / dispensing on PCB DAP and terminal pads before mounting the component onto the board.

Solder paste deposition using a stencil-printing process involves the transfer of the solder paste through pre-defined apertures with the application of pressure. Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the LLP package is highly recommended to improve board assembly yields.

Laser cut stencil with electro polish is recommended. Tapered aperture walls (5° tapering) is recommended to facilitate paste release. Recommended stencil thickness is 127 µm for pitches ≥ 0.5 mm. The recommended stencil thickness is 100 µm for 0.4 mm pitch. In order to prevent solder bridging the stencil aperture openings need to be modified as follows:

- The terminal contact aperture openings should be offset by 0.1mm outward from the center of the package. For package with dual row terminal contacts, only the outer row terminal contacts require the 0.1mm offset.
- For exposed pad aperture, up to 2 mm, the opening should be reduced to 95% of the corresponding PCB exposed DAP dimensions.
- For exposed pad aperture with any side from 2 to 4 mm, the stencil opening should be split in two for any side.
- For exposed pad aperature greater than 4 mm but without ground and power bars, see Table 3.
- For exposed pad aperature greater than 4 mm with ground and power bars, refer to Figure 29.
- For Pullback LLP with single row terminal contacts, stencil aperture is 1:1 with 0.1 mm offset.
- For dual row packages, only the outer row will require the 0.1 mm offset.
- For No Pullback packages with single row terminal contacts, stencil aperture is 0.1mm longer than PCB pads with 0.1 mm offset away from the center of the package.
- For No Pullback packages with dual row terminal contacts, the inner row stencil aperture is 1:1 to the package pads without 0.1 mm offset. The outer row will be 0.1 mm longer than the package pads with 0.1 mm offset away from the center of the package.
- For better control of package flatness after reflow, the stencil aperture for the DAP is recommended as shown in Table 2.

Table 2. Recommended DAP Stencil Aperture

Package DAP Size	Number of Openings	Gap Between Openings	Percentage of Solder Coverage
Less than 2mm × 2mm	1	N/A	80 - 90%
2.1mm - 4.4mm	4	0.2 - 0.3mm	70 - 85%
> 4.4mm	Vary	0.2 - 0.3mm	65 - 85%

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Table 3. Pullback LLP Stencil Aperture Summary (1)

Pin Count	MKT Dwg	PCB I/O Pad Size (mm)	PCB Pitch (mm)	PCB DAP size (mm)	Stencil I/O Aperture (mm)	Stencil DAP Aperture (mm)	Number of DAP Aperture Openings	Gap Between DAP Aperture (Dim A mm)
6	ldb06a	0.25 × 0.4	0.65	1.2 × 0.75	0.25 × 0.4	1.1 × 0.7	1	N/A
6	ldc06d	0.3 × 0.5	0.8	2 × 2.2	0.3 × 0.5	1.8 × 1.98	1	N/A
6	lde06a	0.35 × 0.5	0.95	1.92 × 1.2	0.35 × 0.5	1.8 × 1.1	1	N/A
8	lda08a	0.25 × 0.5	0.5	1.8 × 1.2	0.25 × 0.5	1.7 × 1.1	1	N/A
8	lda08b	0.25 × 0.5	0.5	1.5 × 0.7	0.25 × 0.5	1.4 × 0.6	1	N/A
8	lda08c	0.25 × 0.5	0.5	1.5 × 1.2	0.25 × 0.5	1.4 × 1.1	1	N/A
8	ldc08a	0.3 ×0.5	0.8	3 × 2.2	0.3 × 0.5	1.3 × 0.9	4	0.2
8	lqb08a	0.4 × 0.3	0.65	0.8 × 0.8	0.4 × 0.3	0.7 × 0.7	1	N/A
10	lda10a	0.25 × 0.5	0.5	2 × 1.2	0.25 × 0.5	1.9 × 1.1	1	N/A
14	lda14b	0.25 × 0.5	0.5	3 × 3.2	0.25 × 0.5	1.3 × 1.4	4	0.2
14	ldc14a	0.4 × 0.5	0.8	4.35 ×3	0.4 × 0.5	1.9 × 1.3	4	0.2
16	lda16a	0.25 × 0.5	0.5	4 × 3.2	0.25 × 0.5	1.9 × 1.4	4	0.2
16	lqa16a	0.25 × 0.5	0.5	2.2 × 2.2	0.25 × 0.5	1.9 × 1.9	1	N/A
20	lqa20a	0.25 × 0.5	0.5	2.2 × 2.2	0.25 × 0.5	1.9 × 1.9	1	N/A
24	lqa24a	0.25 × 0.4	0.5	3.4 × 2.4	0.25 × 0.4	1.5 × 1.0	4	0.2
24	lqc24a	0.3 × 0.5	0.8	4.2 × 4.2	0.3 × 0.5	1.9 × 1.9	4	0.2
28	lqa28a	0.25 × 0.5	0.5	3.2 × 3.2	0.25 × 0.5	1.4 ×1.4	4	0.2
32	lqa32a	0.25 × 0.5	0.5	4.2 × 4.2	0.25 × 0.5	1.9 × 1.9	4	0.2
32	lqa32b	0.25 × 0.5	0.5	4.2 × 3.2	0.25 × 0.5	1.9 × 1.4	4	0.2
44	lqa44a	0.25 × 0.5	0.5	4.3 × 4.3	0.25 ×0.5	1.9 × 1.9	4	0.2
48	lqa48b	0.25 × 0.5	0.5	5.1 × 5.1	0.25 × 0.5	1.075 × 1.075	16	0.2
56	lqa56a	0.25 × 0.5	0.5	4.8 × 4.8	0.25 × 0.5	0.5 × 0.5	36	0.3

(1) See Figure 20.

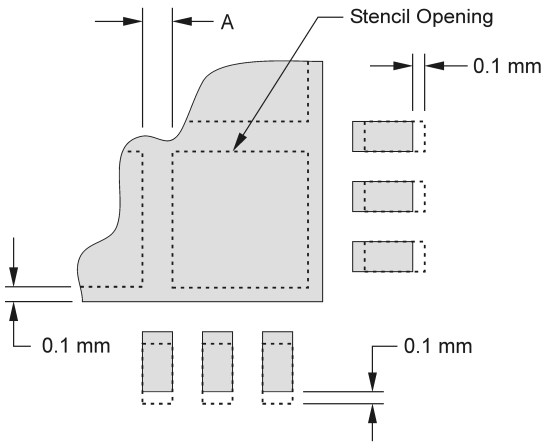

Figure 20. Pullback LLP, Single Row

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Table 4. No Pullback LLP Stencil Aperture Summary [(1)]

Pin Count	MKT Dwg	PCB I/O Pad Size (mm)	PCB Pitch (mm)	PCB DAP size (mm)	Stencil I/O Aperture (mm)	Stencil DAP Aperture (mm)	Number of DAP Aperture Openings	Gap Between DAP Aperture (Dim A mm)
6	sdb06a	0.25 × 0.6	0.65	1.2 × 0.75	0.25 × 0.7	1.14 × 0.71	1	N/A
6	sde06a	0.25 × 0.6	0.95	2.1 × 1.6	0.25 × 0.7	1.9 × 1.4	1	N/A
8	sda08a	0.25 × 0.6	0.5	2 × 1.6	0.25 × 0.7	1.9 × 1.52	1	N/A
8	sdc08a	0.3 × 0.6	0.8	3 × 2.6	0.3 × 0.7	1.3 × 1.1	4	0.2
10	sdc10a	0.3 × 0.6	0.8	3 × 2.6	0.3 × 0.7	1.3 × 1.1	4	0.2
14	sda14b	0.25 × 0.6	0.5	3 × 2.6	0.25 × 0.7	1.3 × 1.1	4	0.2
16	sda16a	0.25 × 0.6	0.5	4 × 3.6	0.25 × 0.7	1.8 × 1.6	4	0.2
16	sda16b	0.25 × 0.6	0.5	4 × 2.6	0.25 × 0.7	1.8 × 1.1	4	0.2
24	sqa24a	0.25 × 0.6	0.5	2.6 × 2.6	0.25 × 0.7	1.1 × 1.1	4	0.2
28	sna28a	0.25 × 0.6	0.5	3.6 × 3.6	0.25 × 0.7	1.6 × 1.6	4	0.2
28	spa28a	0.25 × 0.6	0.5	3.6 × 3.6	0.25 × 0.7	1.55 × 1.55	4	0.3
28	sqa28a	0.25 × 0.6	0.5	3.6 × 3.6	0.25 × 0.7	1.6 × 1.6	4	0.2
36	sqa36a	0.25 × 0.6	0.5	4.6 × 4.6	0.25 × 0.7	1.0 × 1.0	16	0.2
40	sna40a	0.25 × 0.6	0.5	4.6 × 4.6	0.25 × 0.7	1.0 × 1.0	16	0.2
40	sqf40a	0.20 × 0.6	0.4	3.6 × 3.6	0.2 × 0.8	1.6 × 1.6	4	0.2
48	sna48a	0.25 × 0.6	0.5	5.1 × 5.1	0.25 × 0.7	1.1 × 1.1	16	0.2
48	sqf48a	0.20 × 0.6	0.4	4.6 × 4.6	0.2 × 0.8	0.95 × 0.95	16	0.2
48	sqa48a	0.25 × 0.6	0.5	5.1 × 5.1	0.25 × 0.7	1.1 × 1.1	16	0.2
60	sqa60a	0.25 × 0.8	0.5	7.2 × 7.2	0.25 × 0.9	1.16 × 1.16	25	0.3
80	sqa80a	0.25 × 0.6	0.5	10.65 × 10.65	0.25 × 0.7	1.77 × 1.77	9	0.3

(1) See Figure 21.

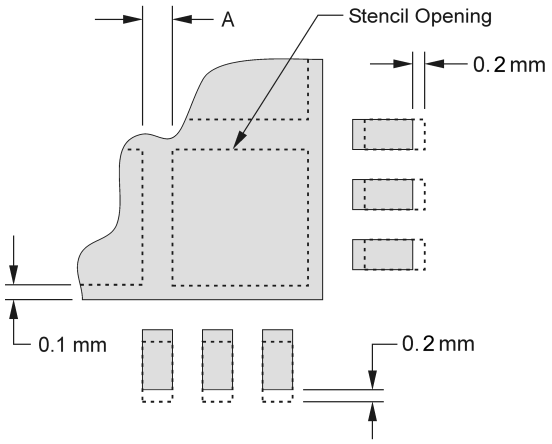

Figure 21. No Pullback LLP, Single Row

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4.3 Package Placement

LLP packages can be placed using standard pick and place equipment with an accuracy of ±0.05 mm. Component pick and place systems are composed of a vision system that recognizes and positions the component and a mechanical system that physically performs the pick and place operation. Two commonly used types of vision systems are:

- a vision system that locates a package silhouette
- a vision system that locates individual pads on the interconnect pattern

The second type renders more accurate place but tends to be more expensive and time consuming. Both methods are acceptable since the parts align due to a self-centering feature of the LLP solder joint during solder reflow.

It is recommended to release the LLP package 1 to 2 mils into the solder paste or with minimum force to avoid causing any possible damage to the thinner packages.

Please refer to Appendix C for Package on Substrate (POS) package placement detail.

4.4 Solder Paste

Type 3, water soluble, no clean, and lead-free solder pastes are acceptable.

4.5 Reflow and Cleaning

The LLP may be assembled using standard IR / IR convection SMT reflow processes without any special considerations. As with other packages, the thermal profile for specific board locations must be determined. Nitrogen purge is recommended during solder for no-clean fluxes. The LLP is qualified for up to three reflow cycles at 235°C peak (J-STD-020). The actual temperature of the LLP is a function of:

- Component density
- Component location on the board
- Size of surrounding components

It is recommended that the temperature profile be checked at various locations on the board. Figure 22 and Figure 23 illustrate typical reflow profiles.

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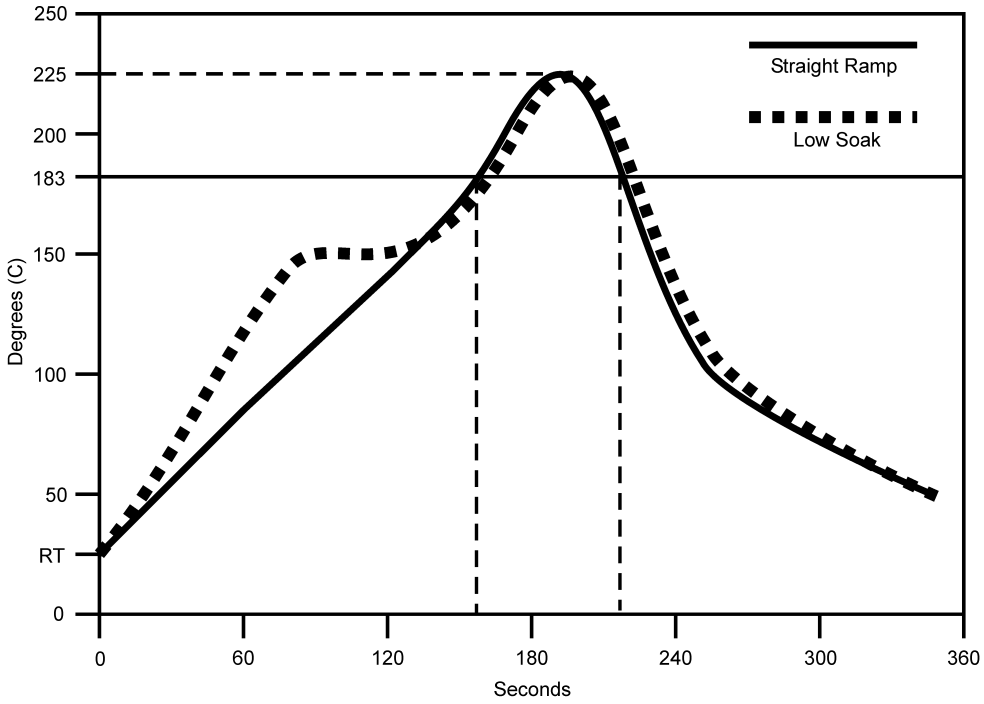

Profile Elements	Straight Line Profile	Low Soak Profile
Ramp rate	0.8 - 1.2 °C/s (RT to Peak temp)	1.5 - 2.0 °C/s (RT to 145 °C)
Dwell @ 145 to 160 °C	N/A	30 - 120 s
2nd Ramp rate	N/A	1.5 - 2.0 °C/s (to Peak Temp)
Time above liquidus (183 °C)	45 - 75 seconds	
Peak temperature range	210 - 225 °C typical, (240 °C max)	
Ramp-down rate to RT	1 - 3 °C/s typical, (6 °C/s max)	
Note: For details, please refer to solder paste manufacturer's recommendation.		

Figure 22. Typical Reflow Profile for Eutectic (63Sn/37Pb) Solder Paste

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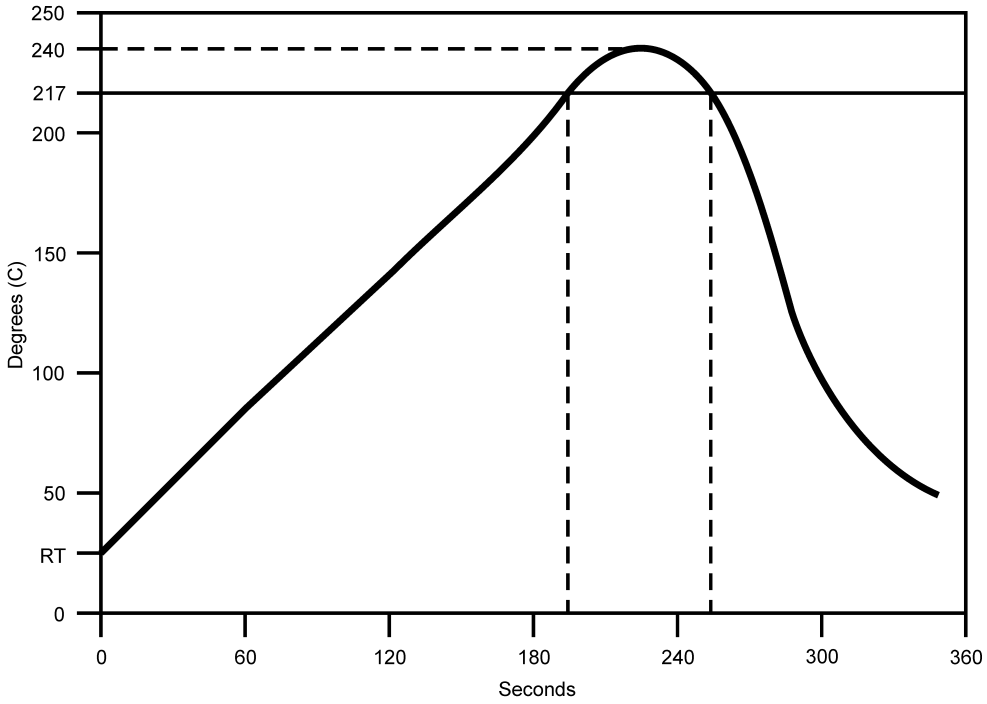

Profile Elements	Convection or IR
Ramp rate (RT to Peak temp)	0.8 - 1.2 °C/s
Time above liquidus (217 °C)	35 - 80 seconds
Peak temperature range	235 - 240 °C typical, (260 °C max)
Ramp-down rate to RT	1 - 2°C/s typical, (6 °C/s max)
Note: For details, please refer to solder paste manufacturer's recommendation.	

Figure 23. Typical Reflow Profile for Lead-Free (SAC305 or SAC405) Solder Paste

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4.6 Solder Joint Inspection

After surface mount assembly, transmission X-ray should be used for **sample** monitoring of the solder attachment process. This identifies defects such as solder bridging, shorts, opens and voids.

NOTE: Voids typically do not have an impact on reliability. Figure 24 shows a typical X-ray photograph after assembly.

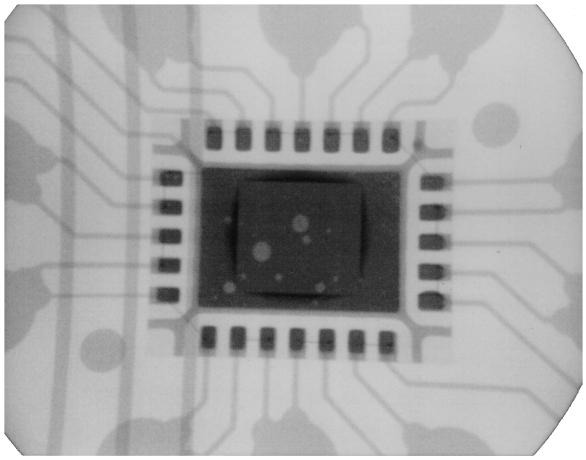

Figure 24. Typical X-ray After Process

In the process setup, it is recommended to use side view inspection in addition to X-ray to determine if there are 'Hour Glass' shaped solder existing. The 'Hour Glass' solder shape is not a reliable joint. 90° mirror projection can be used for side view inspection. See Figure 25.

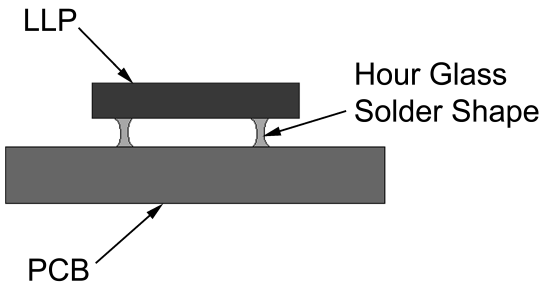

Figure 25. Pullback LLP Hour Glass Solder Joint

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4.7 Replacement and Rework

The quality of the rework is controlled by:

- Directing the thermal energy through the component body to solder without over-heating the adjacent components.
- Heating should occur in an encapsulated, inert, gas-purged environment where the temperature gradients do not exceed ±5°C across the heating zone.
- Using a convective bottom side pre-heater to maximize temperature uniformity.
- Interchangeable nozzles designed with different geometries will accommodate different applications to direct the airflow path

NOTE: Standard SMT rework systems are capable of these elements.

Removal of the LLP Removing the LLP from the PCB involves heating the solder joints above the liquidus temperature of eutectic (63Sn-37Pb) solder using a vacuum gas nozzle. Baking the PCB at 125°C for 4 hours is recommended PRIOR to any rework. Doing this removes any residual moisture from the system, preventing moisture induced cracking or PCB delamination during the demount process.

A 1.27 mm (50 mil) keep-out zone for adjacent components is recommended for standard rework processing. If the adjacent components are closer than 1.27 mm, custom tools are required for the removal and rework of the package.

It is recommended that the reflow profile used to reflow the LLP be as close to the PCB mount profile as possible. Preheat the PCB area, through the bottom side of the board, to 100°C before heating the LLP to ensure a controlled process. Once the liquidus temperature is reached, nozzle vacuum is automatically activated and the component is removed. After removing the package, the pads may be heated with the nozzle to reflow any residual solder, which may be removed using a Teflon tipped vacuum wand.

Site Preparation Once the LLP is removed, the site must be cleaned in preparation for package attachment. The best results are achieved with a low-temperature, blade-style conductive tool matching the footprint area of the LLP in conjunction with a de-soldering braid. No-clean flux is needed throughout the entire rework process. Care must be taken to avoid burn, lift-off, or damage of the PCB attachment area. See Figure 26.

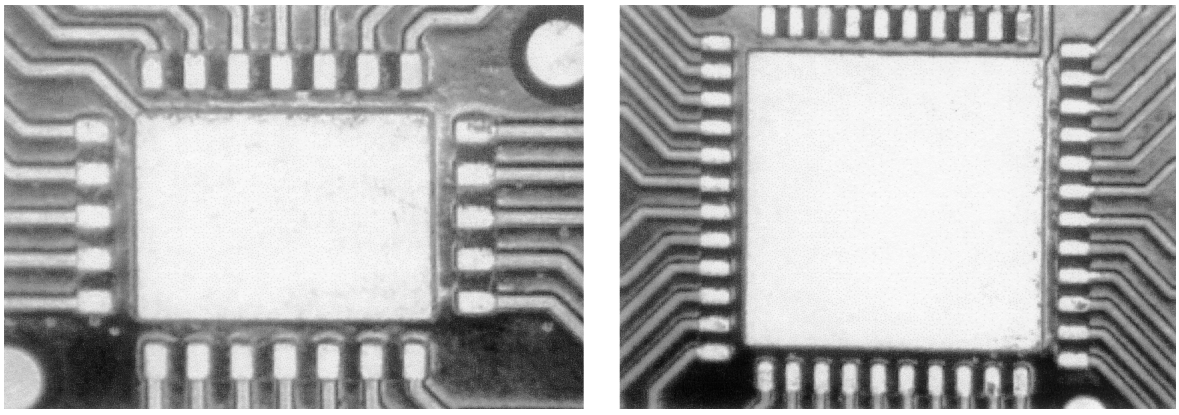

Figure 26. Pads After Removing Components and Cleaning

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Solder Paste Deposition Because the LLP is a land area type package, solder paste is required to insure proper solder joint formation after rework. A 127 µm (5 mil) thick mini-stencil is recommended to deposit the solder paste patterns prior to replacement of the LLP. See Figure 27.

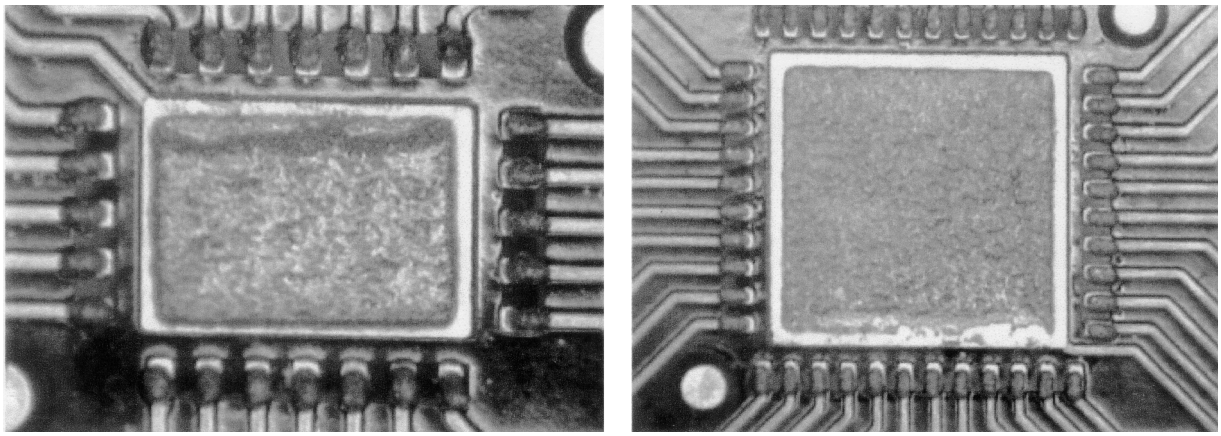

Figure 27. Solder Paste Printing of LLP 24 and LLP 44 Using 127 µm (5 mil) Thick Stencil

Component Placement Most CSP rework stations will have a pick and place feature for accurate placement and alignment. Manual pick and place, with only eye-ball alignment, is not recommended. It is difficult or impossible to achieve consistent placement accuracy. Improper handling or excessive pressure may cause damage to some of the thinner packages.

Component Reflow It is recommended that the reflow profile used to reflow the LLP be as close to the PCB mount profile as possible. Preheat the PCB area, through the bottom side of the board, to 100°C before heating the LLP to ensure a controlled process. Once the liquidus temperature is reached, the solder will reflow and the LLP will self align. Figure 28 shows a cross section of a solder joint after rework.

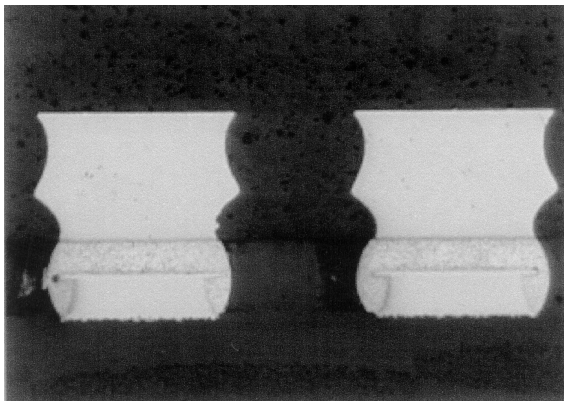

Figure 28. X-section Across Solder Joints

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Appendix A Board Level Reliability Test Data

A.1 Temperature Cycle Test

Test Conditions:

- Temperature Range: −40 to 125°C
- Cycle Duration: 1 hour (15 minute ramp/15 minute Dwell)
- Test Board Dimension: 142.5 mm × 142.5 mm × 1.6 mm
- Test Board Finish: Ni-Au 0.05 µm to 0.2 µm gold thickness
- Dummy die in package
- Package is bonded with a Daisy Chain Circuit

Failure Determination: Change of 10% in Net Resistance

Results:

I/O Count	Body Size (mm)	Exposed DAP Size (mm)	Die Size (mm)	Solder	DAP Soldered	PCB Surface Finish	15/15/15/15		
							Failure Cycle		Beta
							First	63.2%	
LLP - Pullback, Dual Row [1]									
80	8 × 8 × 0.8	3.9 × 3.9	3.8 × 3.8	63Sn/37Pb	Yes	NiAu	1469	2350	8.6
LLP - Pullback, Single Row [1]									
56	9 × 9 × 0.8	4.8 × 4.8	4.06 × 3.76	63Sn/37Pb	Yes	NiAu	Pass 1050x No Failure		
					No	NiAu	Pass 1050x No Failure		
					Yes	OSP	Pass 1050x No Failure		
				SAC305	No	NiAu	Pass 1050x No Failure		
					No	OSP	Pass 1050x No Failure		
44	7 × 7 × 0.8	4.3 × 4.3	3.25 × 3.08	63Sn/37Pb	Yes	NiAu	Pass 1050x No Failure		
					No	NiAu	Pass 1050x No Failure		
24	5 × 4 × 0.8	3.4 × 2.4	2.31 × 1.4	63Sn/37Pb	Yes	NiAu	Pass 1050x No Failure		
					No	NiAu	Pass 1050x No Failure		
LLP - Pullback, Single Row [2]									
14	6 × 5 × 1.0	4.35 × 3.0	4.29 × 2.95	63Sn/37Pb	Yes	NiAu	Pass 1050x No Failure		
SOT-23 Footprint Compatible LLP [3]									
6	2.92 × 3.29 × 0.8	1.92 × 1.2	1.45 × 1.14	63Sn/37Pb	Yes	NiAu	Pass 1050x No Failure		
					No	NiAu	Pass 1050x No Failure		
LLP - No Pullback [4]									
40	5 × 5 × 0.8	3.6 × 3.6	3.6 × 3.6	SAC305	Yes	NiAu	Pass 1050x No Failure		
48	6 × 6 × 0.8	4.6 × 4.6	4.3 × 4.3	SAC305	Yes	NiAu	950	2730	3.3
48	7 × 7 × 0.8	5.1 × 5.1	2.4 × 2.2	63Sn/37Pb	Yes	NiAu	Pass 1500x No Failure		
48	7 × 7 × 0.6	5.1 × 5.1	4.7 × 4.7	63Sn/37Pb	No	NiAu	Pass 1500x No Failure		
48	7 × 7 × 0.4	5.2 × 5.2	4.4 × 4.1	SAC305	No	NiAu	Pass 1600x No Failure		
48	7 × 7 × 0.4	5.2 × 5.2	2.2 × 2.2	SAC305	No	NiAu	Pass 1600x No Failure		

(1) Terminal Pad Size: 0.5 × 0.25 mm; Terminal Pad Pitch: 0.5 mm; Die Thickness: 0.216 mm; PCB Thickness: 1.6 mm
(2) Terminal Pad Size: 0.5 × 0.4 mm, Terminal Pad Pitch: 0.8 mm, Die Thickness: 0.216 mm, PCB Thickness: 1.6 mm
(3) Terminal Pad Size: 0.5 × 0.35 mm, Terminal Pad Pitch: 0.96 mm, Die Thickness: 0.216 mm, PCB Thickness: 1.6 mm
(4) Terminal Pad Size: 0.4 × 0.25 mm, Terminal Pad Pitch: 0.5 mm, Die Thickness: 0.216 mm, PCB Thickness: 1.6 mm

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I/O Count	Body Size (mm)	Exposed DAP Size (mm)	Die Size (mm)	Solder	DAP Soldered	PCB Surface Finish	15/15/15/15		
							Failure Cycle		Beta
							First	63.2%	
LLP - No Pullback [5]									
48	7 × 7 × 0.4	5.2 × 5.2	4.4 × 4.1	SAC305	No	NiAu	Pass 1700x No Failure		
LLP — No Pullback, Single Row [6]									
80	12 × 12 × 0.75	10.65 × 10.65	10.5 × 10.5	SAC305	Yes	OSP	552	1066	6.1

(5) Cycle Duration: 34 minutes (3 minute ramp/14 minute Dwell)

(6) Terminal Pad Size: 0.4 × 0.25mm, Terminal Pad Pitch: 0.5mm, Die Thickness: 0.203mm, PCB Thickness: 0.694mm, Temperature Range: 0 to 100°C as per JEDEC Standard (JESD22-A104), Cycle Duration: 15min (5min dwell / 10min Ramp)

A.2 Board Drop Test

Test Conditions:

- Test Board Dimension: 142.5 mm × 142.5 mm × 1.6 mm
- Printed Circuit Board Finish: Ni-Au0.05 µm - 0.2 µm gold thickness
- Dummy die in package
- Package is bonded with a Daisy Chain Circuit
- Cumulative Dead weight of the board: 150 Grams
- Drop Height: 1.5 meters
- Drop Surface: Non cushioning vinyl tile
- Number of Drops: 30 total
  - 7 drops: along the length of the PCB
  - 7 drops: along the width of the PCB
  - 8 Drops: Along the diagonal of the board
  - 8 Drops: With the components on the top of the board

Failure Determination: Change of 10% in Net Resistance

Results:

Package Type	Drop Test Results
24L 4 mm × 5 mm LLP (DAP soldered to PCB)	0/20
24L 4 mm × 5 mm LLP (DAP NOT soldered to PCB)	0/20
44L 7 mm × 7 mm LLP (DAP soldered to PCB)	0/20
44L 7 mm × 7 mm LLP (DAP NOT soldered to PCB)	0/20
56L 9 mm × 9 mm LLP (DAP soldered, Power/Ground Rings soldered to PCB)	0/25
14L Power LLP	0/32
48L 7 mm × 7 mm LLP [1] (DAP solder to PCB)	0/15
Single Row 80L 12mm × 12mm LLP [2] (DAP soldered to PCB)	0/68

(1) Per Jedec Standard JESD22-B111, 1500G's 0.5mS Half-Sine Pulse

(2) Per Nokia Standard for PWB level Mechanical Shock Test

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A.3 Vibration Test

Test Conditions:

- Test Board Dimension: 142.5 mm × 142.5 mm × 1.6 mm
- Printed Circuit Board Finish: Ni-Au 0.05 µm - 0.2 µm gold thickness
- Dummy die in package
- Package is bonded with a Daisy Chain Circuit
- Die attach pad soldered to PCB
- Vibration test conditions:
  - Sinusoidal excitation performed for 1 hour at 20G force followed by 3 hours at 40G force
  - Random Vibration with variable frequencies ranging from 20Hz to 2,000Hz for 3 hours with a force of 2G RMS

Results: DAP Soldered to PCB

Package Type	Test Results
24L 4 mm × 5 mm LLP	0/24
44L 7 mm × 7 mm LLP	0/20
56L 9 mm × 9 mm LLP	0/25
14L 6 mm × 5 mm Power LLP	0/32

A.4 Flex Test

Test Conditions:

- PCB Size: 75 × 55 × 0.8 mm
- Surface Finish: Electroless Nickel Immersion Gold
- Solder Paste: 63Sn/37Pb
- Stencil: 0.127 mm
- Deflection: 1 mm with 12.7 mm puncher offset
- Span: 50 mm
- Frequency: 1Hz

Results:

Package	16L	60L
Body Size (mm)	4 × 4	9 × 9
1mm @ 1Hz with 0.5 inch offset	+5000 cycles	+5000 cycles

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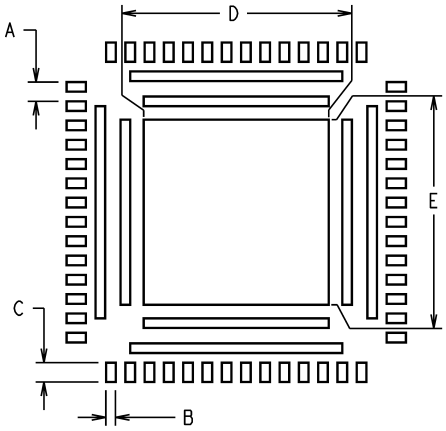
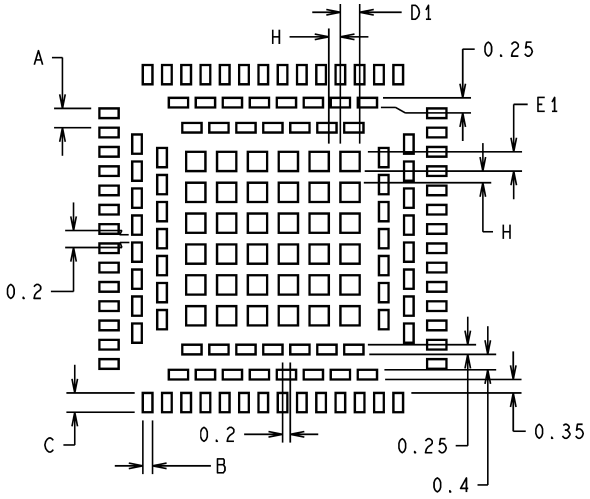
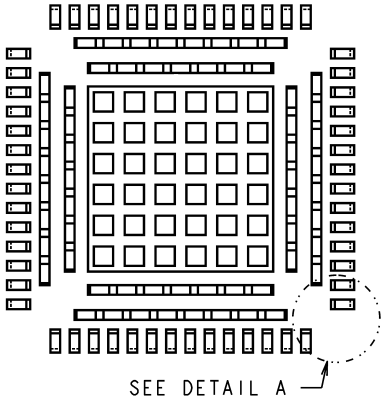
Appendix B Custom Package Design



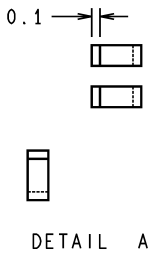
Recommended Pad



Recommended Stencil Aperture



Stencil Over



	Number of pins	56
A	LLP, PCB, Stencil Terminal Pitch (mm)	0.5
B	LLP, PCB, Stencil Terminal Width (mm)	0.25
C	LLP, PCB, Stencil Terminal Length (mm)	0.5
D	LLP, PCB Exposed DAP Width (mm)	4.8
D1	Exposed DAP Aperture Width (mm)	0.5
H	Aperture split width, centered (mm)	0.3
E	LLP, PCB Exposed DAP Length (mm)	4.8
E1	Exposed DAP Aperture Length (mm)	0.5
F	Stencil Aperture opening offset (mm)	0.1

Figure 29. Typical Recommended Stencil Openings for 56 Pin LLP with Exposed DAP, Ground and Power Bars

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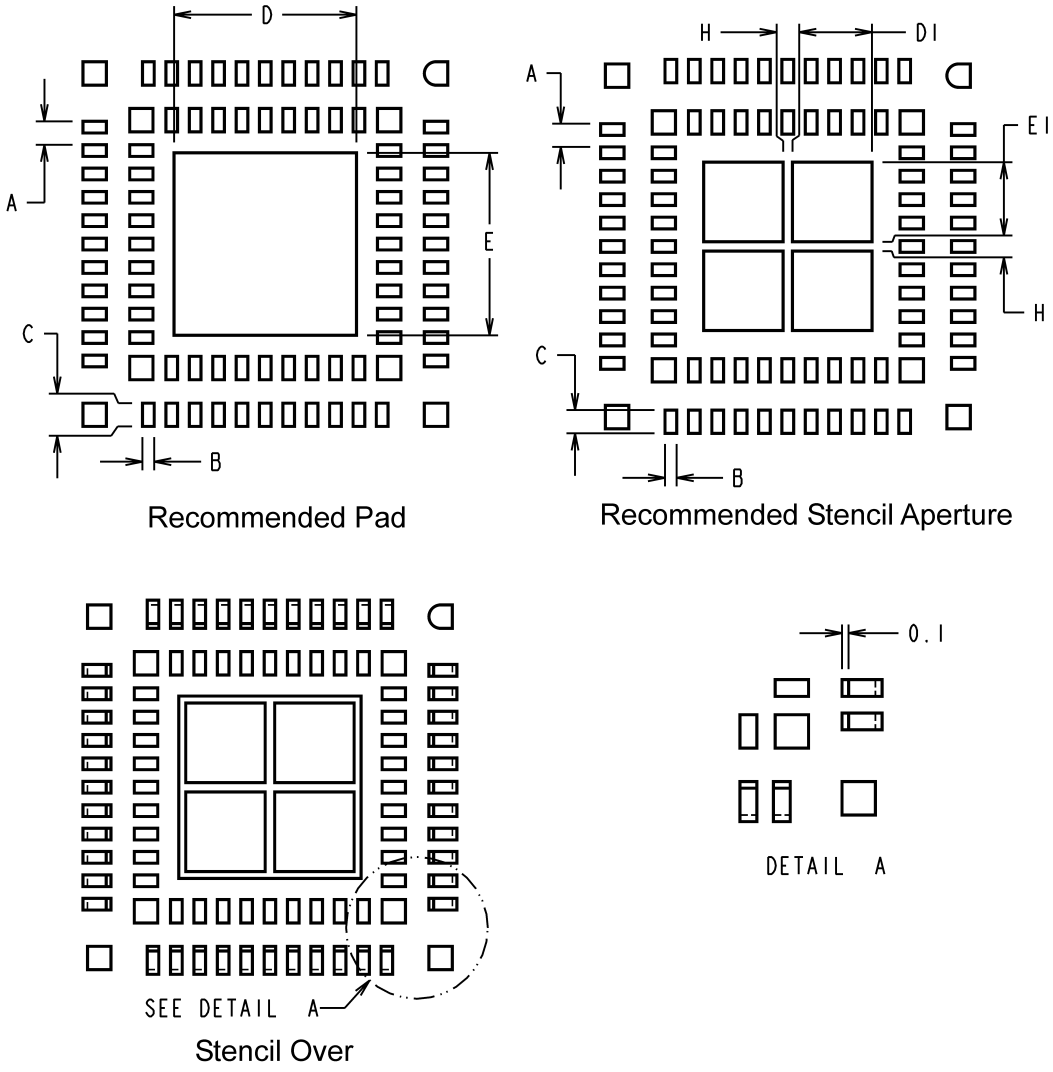

	Number of pins	80
A	LLP, PCB, Stencil Terminal Pitch (mm)	0.5
B	LLP, PCB, Stencil Terminal Width (mm)	0.25
C	LLP, PCB Terminal Length (mm)	0.5
D	LLP, PCB Exposed DAP Width (mm)	3.9
D1	Exposed DAP Aperture Width (mm)	1.7
H	Aperture split width, centered (mm)	0.2
E	LLP, PCB Exposed DAP Length (mm)	3.9
E1	Exposed DAP Aperture Length (mm)	1.7
F	Stencil Aperture opening offset (mm)	0.1

Figure 30. Typical Recommended Stencil Openings for 80 Pin LLP with Exposed DAP and Dual Row

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B.1 Stencil Openings for SOT23 5/6L Footprint Compatible LLP

For the SOT23 5/6L footprint compatible LLP for which the PCB has been designed for the SOT23 package, refer to Figure 31 for solder stencil openings.

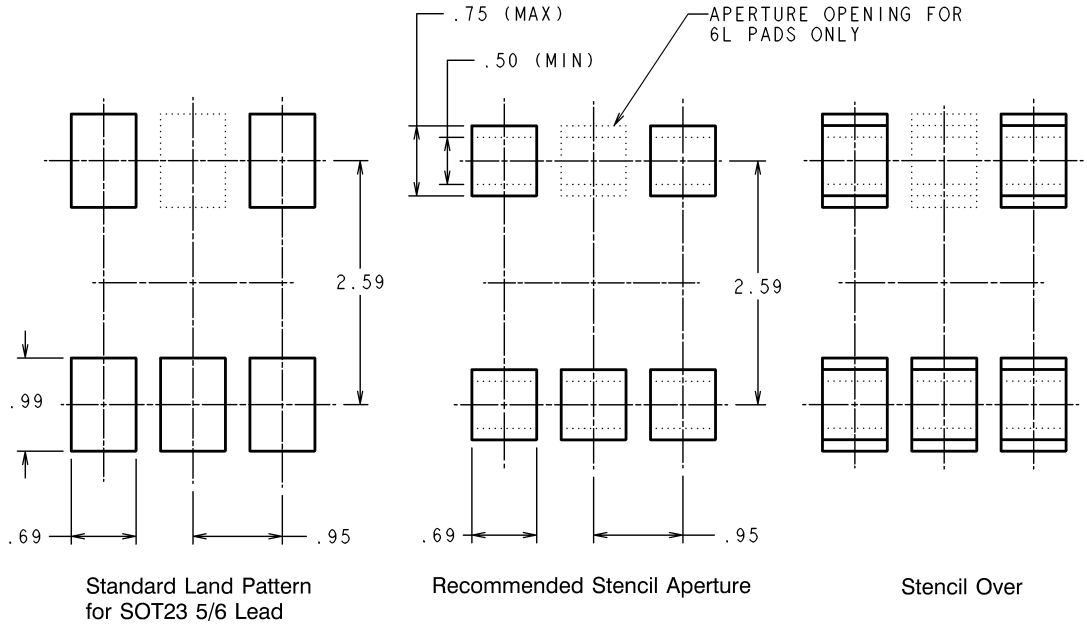

Figure 31. Recommended Stencil Apertures for SOT23 5/6 Lead Footprint Compatible LLP

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Appendix C Package on Substrate (POS) Package Placement

The POS package has a LLP footprint with a micro SMD die mounted on the top of the package. The following are suggestions of how to avoid damage to the package during board assembly process:

- Select a pick and place nozzle with no more than half of the dimension of the device
- Reduce the pick and place nozzle vacuum pressure
- Add 0.05 mm to the component thickness during placement programming or apply minimum force to avoid putting too much pressure on the device during board mounting

Appendix D Revision Log

Revision Date	Description
September 2005	Added 0.4 mm LLP information.
February 2006	Updated the section on Thermal Design Considerations
August 2010	Added solder bump package offering. Updated Stencil Aperture table. Added 80 lead reliability data.
September 2011	Add POS package appendix and reference.

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