OA-15 Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers

ABSTRACT

As op amp operating speeds have moved to ever higher frequencies, a whole new set of design concerns have come into play for linear op amp applications. With the development of the current feedback topology, design concerns unique to that topology must also be considered if optimal performance is to be achieved from devices offering over 200 MHz −3 dB bandwidths. This application report reviews some of the considerations common to all wideband linear op amp applications as well as topics unique to the current feedback topology pioneered by Comlinear Corporation. These design guidelines are intended to help the designer get the full potential out of Comlinear's high performance, current feedback, operational amplifiers.

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1   Introduction

Since there are quite disparate areas to consider here, the approximate order of discussion will follow a perceived frequency of occurrence ranking. Those considered first seem to impact every designer, with more particular concerns dealt with later.

2   Parasitic Capacitance Effects and What to do About Ground and Power Planes in a PC Board Layout.

The sensitivity of the Comlinear amplifiers to parasitic capacitance arises solely from their wide bandwidth characteristics and not from the current feedback aspect of their design. With parts showing a loop gain that does not drop to unity until the 100 MHz region, a few picofarad capacitance to ground in the loop can have a profound effect on the phase margin at the unity gain crossover frequency. Figure 1 shows a typical non-inverting gain op amp, including the internal structure for the current feedback topology, along with the two most critical external parasitic capacitances. See *OA-13 Current Feedback Loop Gain Analysis and Performance Enhancement Application Report* (SNOA366) or *OA-31 Current Feedback Amplifiers Application Report* (SNOA364) for a development of the current feedback transfer function.

$$\text{ideal } A_V \equiv \frac{V_o}{V_i} = 1 + \frac{R_f}{R_g}$$

Most critical parasitic capacitances
$C_{Po} \longrightarrow$ output capacitance
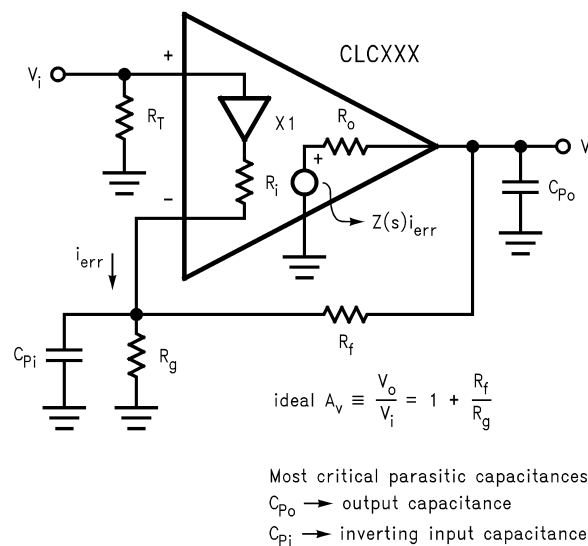$C_{Pi} \longrightarrow$ inverting input capacitance

Figure 1. Non-inverting Gain with Internal Current Feedback Topology

Parasitic, or loading, capacitance directly on the output is particularly effective at transforming amplifiers into oscillators. Closed loop stability for any negative feedback amplifier is determined by the open loop phase margin. In tracing the signal around the loop it is always desirable to have significantly less than 180 degrees phase shift around the loop at the unity gain crossover frequency. Adding a capacitor directly on the output will cause additional signal phase shift due to the additional pole introduced by the open loop output impedance, R_o, driving the output pin capacitance, C_{po}. Even small capacitances and low R_o's can cause significant phase shifts with unity gain crossovers in the 100 MHz region (a typical unity gain crossover frequency for Comlinear amplifiers).

Several design and test guidelines can be suggested to keep this sensitivity to C_{po} under control.

1. Always clear ground and power planes away from the output pin net. This includes opening up a little wider than standard clearance to ground and power inner planes to any through hole or trace carrying the output signal.

2. Never probe directly with a high impedance probe or a DVM on the output pin (passive divider probes are okay). If probing, always probe through a series resistor > = 100Ω since this will decouple the effect of the probe capacitance from the output pin. This also holds for adding PC board test points. If needed, connect the test points through a series resistor located as close as possible to the device pin being brought out.

3. If a capacitive load must be driven, such as flash ADC's most of the Comlinear amplifier data sheets include a plot of a recommended series resistor to put at the output prior to the load capacitance. Adding a resistor prior to the load (or parasitic) capacitance, changes the load's effect from a pole to a pole-zero pair. This causes a phase dip in the loop phase response that has recovered prior to unity gain crossover.

4. Driving into another amplifier stage, or actually almost any other high input impedance active device, can also present enough capacitance to cause problems. Again, a small series resistor right at the output prior to going off to this device will defuse the situation.

Figure 2 and Figure 3 show the effect of an output capacitance on the small signal frequency response of the CLC205, a hybrid current feedback op amp intended for higher gains. The plot shows the SPICE simulated gain, in dB, vs. linear frequency under several loading conditions. Similar plots may be generated using the small signal macromodels. Initially, a 200Ω load is driven, then just a 20 pF load, and finally, the 20 pF load with a series 30Ω resistor (R_s in Figure 2). Clearly, getting into a series resistor prior to the capacitive load can dramatically improve the frequency response flatness, and hence pulse response capabilities for the amplifier simulated here. Recall that this approach is applicable for both current and voltage feedback amplifiers.

Generally, it is suggested to get the output voltage through a resistor as soon as possible before running it over any significant length of trace or cable. If a matched impedance load is to be driven, source match right at the output pin with a discrete resistor equal to the transmission line's characteristic impedance, and terminate the line similarly. Although short trace runs do not need to be impedance matched, using just the series resistor will isolate the trace capacitance when no terminating resistor is used.
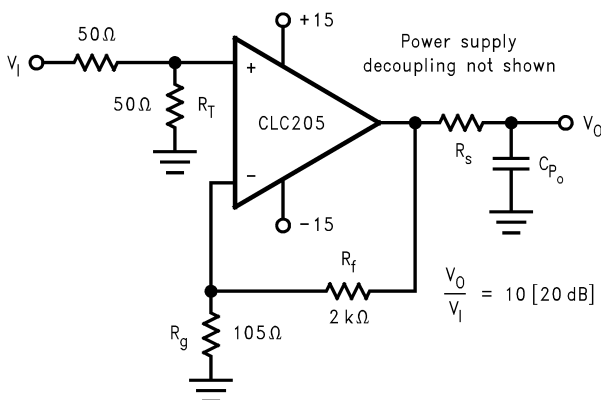

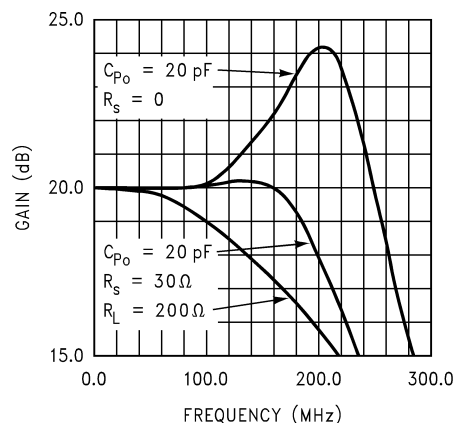**Figure 2. Simulation Circuit for Capacitive Loading Test**

Figure 3. Frequency Response for Various Loadings

Parasitic capacitance on the inverting node is a considerably more complex, but not nearly as troublesome, phenomena. Capacitance on this input affects both the non-inverting signal gain, by appearing in shunt with the gain setting resistor, and the loop gain phase margin in a 2nd order sense. Two types of pulse response characteristics can be observed due to this parasitic. If the dominant effect is simply shunting R_g in the ideal gain expression, neglecting loop gain effects for now, a single overshoot with a decay will be observed. If this capacitance is large enough to effect the phase margin, considerable ringing in the pulse response will also be observed.

Again, minimize ground and power planes around the inverting node net. The single overshoot and decay will most often be observed when a current feedback part intended for higher gains, and hence designed to use a relatively high feedback resistor value, is used at low non-inverting gains. The relatively high R_g required to get a low non-inverting gain will bring the impact of whatever parasitic is present down in frequency into the passband of the amplifier. The solution here, beyond simply limiting C_{pi}, is to run inverting mode if possible, or switch to a part intended for lower gain operation, and hence designed to use lower resistor values. Given a fixed C_{pi}, operating with lower R_f and R_g will move the zero frequency out beyond the amplifier passband. For more detail on the gain range considerations for current feedback amplifiers, see *OA-14 Improving Amplifier Noise for High 3rd Intercept Amplifiers Application Report* (SNOA389).

Figure 4, Figure 5, and Figure 6 shows a test circuit and simulation results demonstrating the effect of inverting node capacitance for the CLC205 operated at relatively low non-inverting gain.

The effect of increasing C_{pi} from 0.5 pF to 5 pF in the circuit of Figure 4 can be seen as a considerable peaking in the frequency response of Figure 5. This is not, in this case, a loss of phase margin peaking, but simply a zero coming into the non-inverting transfer function due to C_{pi} shunting R_g. This zero frequency is at $(C_{pi} \times (R_g||R_f) / (2 \times pi))$ Hz. Note in the pulse response of Figure 6 that C_{pi} causes a single overshoot with negligible ringing.
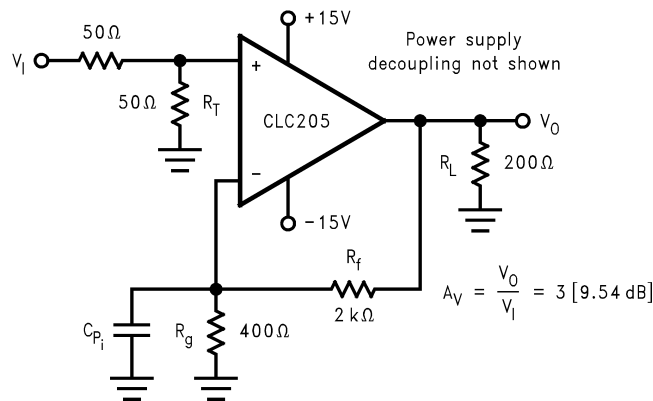

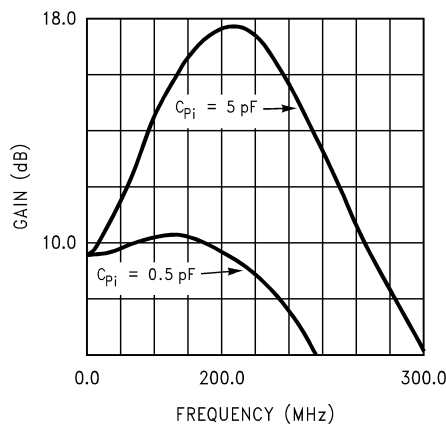**Figure 4. Simulation Circuit for Inverting Input Capacitive Test**

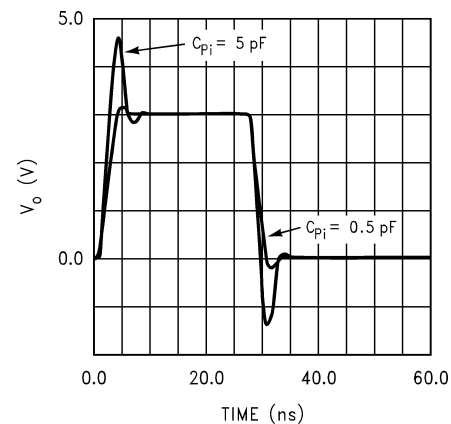**Figure 5. Frequency Response vs. C_{pi}**

Figure 6. Pulse Response vs. C_{pi}

If ringing is observed in the pulse response, this is more likely due to capacitance on the output pin. However, larger parasitic capacitances on the inverting node (>10 pF) can also cause loop gain phase margin problems, particularly for parts intended for high gains. Again, the discussion about avoiding parasitic capacitances on the output pin applies equally well here. Figure 7 shows the difference in pulse response behavior between C_{po} and C_{pi} effects. The upper trace, which was plotted with a 1V offset for clarity, shows the ringing pulse response for the most peaked response of Figure 3. This is typical of output pin capacitance effects. The lower trace is a repeat of the C_{pi} = 5 pF pulse response of Figure 6.

Parasitic capacitance to an AC ground on the non-inverting input, including the capacitance of the high impedance non-inverting input itself, will generally only introduce an additional response pole, depending on the source impedance driving the input capacitance. For low source impedances, this pole comes in well beyond the passband of the amplifier. However, when the parasitic capacitance on the non-inverting and inverting nodes are approximately equal, intentionally adding non-inverting source impedance equal to $R_g||R_f$ can be very effective at cancelling the response zero coming in through C_{pi} shunting R_g.
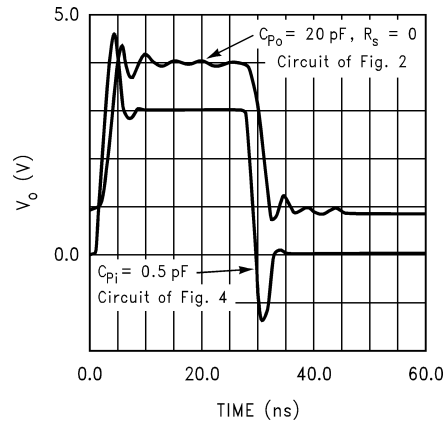
Figure 7. Contrasting Pulse Responses for C_{po} and C_{pi}

Figure 8 shows this approach with the C_{pi} = 5 pF case considered earlier in Figure 4. Note that we have intentionally matched the capacitance at the non-inverting input and added R_{ni} = 300 to bring the frequency response back to flatness. The signal gain is not changed by the addition of R_p. This approach simply cancels the zero apparent in the upper trace of Figure 9, significantly decreasing the pulse overshoot as shown in Figure 10.

Although it is critical to remove ground plane from the signal input and output nodes, a good, low inductance, ground return path must be provided for the AC load current. This is typically provided by putting small-valued ceramic capacitors directly on the power supplies, connected to a good adjacent ground plane. These conflicting goals of good power supply grounding with no parasitic capacitance on the I/O pins can be achieved by opening a window around the part for the ground and power planes with the high frequency decoupling capacitors connecting into this ground plane. The layout drawing of the 730013 evaluation board (in the product accessories section of the catalog), shows a good high frequency layout for the 8-pin DIP monolithic amplifier products offered by Comlinear.
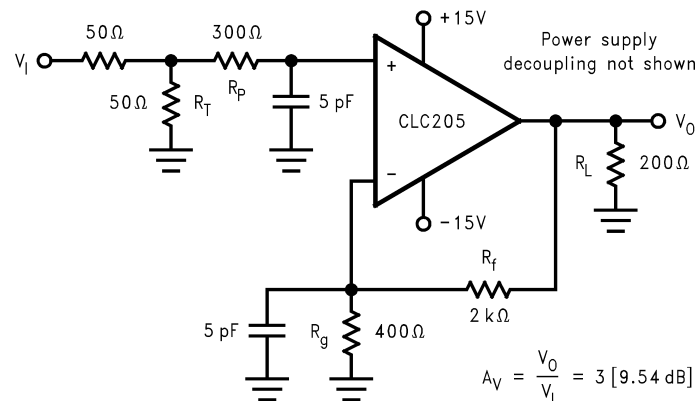

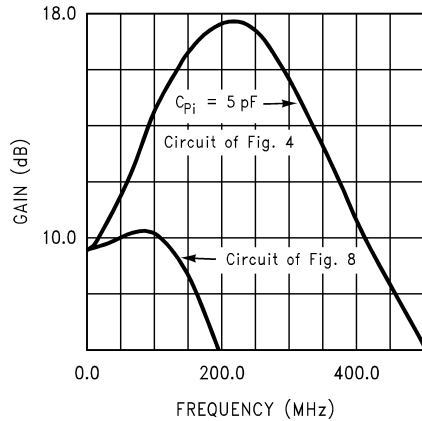**Figure 8. Simulation Circuit of C_{pi} Peaking Cancellation**

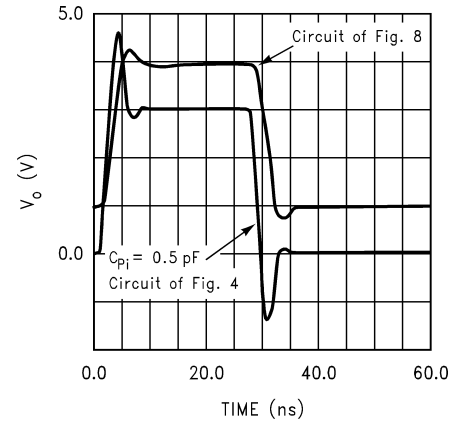**Figure 9. Frequency Response Demonstrating Zero Cancellation**

Figure 10. Pulse Response with Zero Cancellation

Figure 11 shows the same amplifier as Figure 1 with the suggestions for handling parasitic capacitances incorporated.

The circuit of Figure 11 includes every fix for the possible problems arising from parasitic capacitance discussed thus far. Very rarely would all of these be required for the same application. If test points are to be brought out, always come out through at least 100Ω resistors with the body of those resistors as close as possible to the amplifier pins. Probing at these test points can still radically alter the signal path frequency response. The amplifier should, however, remain stable with at least 100Ω isolating resistors. If inverting node parasitic capacitance seems to be a problem, R_p can be very effective at cancelling it out (except when C_{pi} is so large as to cause phase margin problems). If a parasitic or load capacitance must be driven, R_s may be used very effectively to improve the frequency response flatness. And, always get the high frequency capacitors on the power supplies as close to the part as possible into a good ground plane.
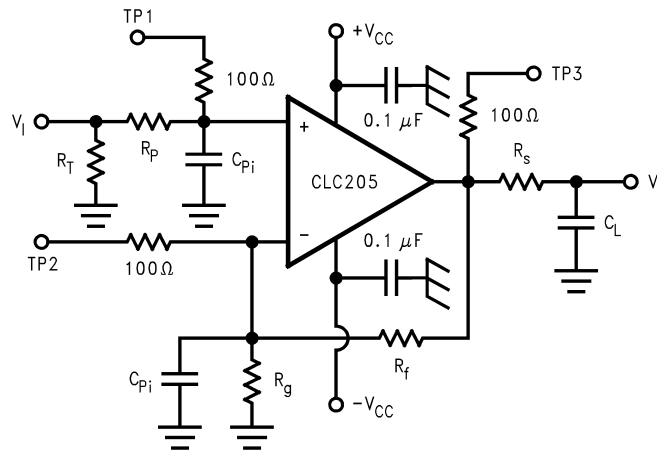

Figure 11. Non-Inverting Amplifier Featuring Several Suggested Protections from Parasitic Capacitance Effects

3   The Importance of the Feedback Resistor

The feedback resistor value becomes of paramount importance in the current feedback topology used by most of the Comlinear amplifiers. The feedback resistor is the single most important element in setting the overall frequency response for the current feedback amplifier topology, as discussed in *OA-14 Improving Amplifier Noise for High 3rd Intercept Amplifiers Application Report* (SNOA389). Briefly, since we are looking for a feedback current from the output voltage to the inverting input, the feedback impedance plays the dominant role in determining what this will be. This, in turn, will determine the amplifier's loop gain and phase margin. Achieving adequate phase margin is critical to the success of any operational amplifier application.

Every current feedback amplifier is optimized for a particular value of feedback resistor. This value is typically noted at the heading of the specifications listing. Always select a value near this as the starting point for any design. Lower values may be used at the risk of lower phase margin and greater frequency response peaking. Higher values may be used at the expense of lower amplifier bandwidth. In fact, increasing the feedback resistor value is a very effective means of overcompensating the amplifier. Unlike voltage feedback amplifiers, a unity gain follower application requires the recommended feedback resistor to be in place from the output to the inverting input. Although having no influence on the low frequency signal gain in the unity follower application, the feedback element is still needed to determine the loop gain for the current feedback topology.

Using reactive elements in the feedback path, either intentionally or unintentionally, can play havoc with the loop gain phase margin. Generally, this should be avoided unless done with extreme care. The small signal macromodels are very useful for predicting what will happen with different feedback configurations. Using direct capacitive feedback, to implement an integrator, will generally cause oscillations with a current feedback amplifier. Integrators can be implemented, however, using the alternative topologies shown in *OA-07 Current Feedback Op Amp Applications Circuit Guide* (SNOA365). Also, the CLC420, a wideband voltage feedback op amp, can be used to implement classical integrator topologies.

Returning to the feedback resistor itself, never use a wirewound type for this, or any other, resistor in a broadband application. Also, trying to compensate the amplifier by using shunt capacitance across R_f will typically yield oscillations with the current feedback topology. It is much more fruitful to compensate by increasing the value of the feedback resistor, although a pot in the feedback path is not recommended.

4   Non-Inverting Source Impedance Considerations

The impedance seen looking out of the non-inverting input can play a strong role in determining an amplifier's overall performance. For very broadband applications, significant resistive source impedance, in conjunction with the part's input capacitance, can become the bandlimiting point in the system. This is normally not a problem for 50Ω terminations driven from a 50Ω source.

When running the amplifier in inverting mode, the non-inverting input would typically be grounded, either directly, or through an approximately 25Ω resistor. No attempt at source impedance matching on the two inputs for bias current cancellation should be made since the two bias currents for a current feedback amplifier are totally unrelated in both magnitude and polarity. Hence, unlike a voltage feedback op amp, there is no meaning to an offset current specification.

Generally, taking the non-inverting input to ground through a 25Ω resistor (for inverting amplifier applications) will eliminate any oscillations that might be seen due to negative input impedance effects at very high frequencies for the non-inverting input. It is oftentimes sufficient to simply ground the non-inverting input. But a careful check for low level oscillations above 500 MHz should be made, particularly for the faster amplifiers, if direct grounding is desired. If oscillations are observed, going to a 25Ω, or higher, resistor to ground will kill this self oscillation in the non-inverting input transistors.

When it is desired to AC couple the non-inverting input signal, as shown in Figure 12, particular attention must be paid to the effect the terminating resistor has on the DC operating point of the amplifier. Oftentimes, in an effort to achieve very low pole frequencies for the AC coupling (without an inordinately large coupling capacitor, C_t), R_t is made very large or, in some cases, not included.

R_t, however, provides the DC current path for the non-inverting input bias current. Wideband amplifiers with a purely bipolar construction, as Comlinear's amplifiers typically are, have an input bias current ranging into the 10's of µA's. It is critical, therefore, to consider the effect a large R_t has on the input offset voltage (as shown in Figure 12). It is very easy, with large R_t, for this bias current requirement to have driven the input and output into saturation precluding proper high frequency operation. The effect of high R_t on the non-inverting noise current gain should also be considered. This noise current will add as an input noise voltage term dependent on the frequency dependent source impedance looking back out the non-inverting input.
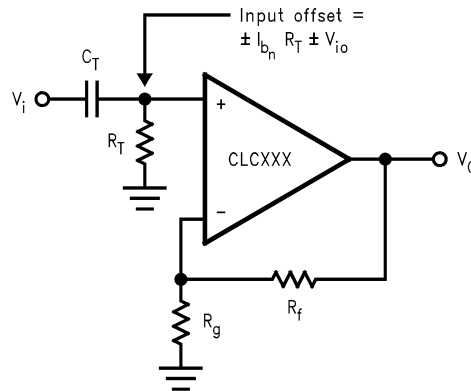

Figure 12. Effect of R_t on DC Input Offset Voltage

5   Input and Output Voltage Range Considerations

The common mode input voltage range specification (CMIR) shown in the Comlinear data sheets indicates how near the specified supply voltages the non-inverting input voltage may be for proper operation. When operating properly, the inverting node voltage simply follows the non-inverting even for differential amp applications. For current feedback, this is due to the unity gain buffer from V^+ to V^-, while for voltage feedback, this is due the feedback loop.

Since all of the amplifiers are specified with balanced bipolar supply voltages, the CMIR and output voltage ranges are given as an allowed bipolar swing around ground. Both specifications are, however, indicating the required voltage headroom to the supplies on the non-inverting input and output pins respectively. Recasting these specifications as a required voltage headroom would allow input and output voltage ranges to be set for non-standard supply voltages.

In almost all cases, the maximum output voltage swing will be the limiting factor. Only at very low non-inverting gains, or for single amplifier differential operation, will the CMIR limit operation. The crossover non-inverting gain where the limiting point will change from input to output can be found by dividing the output voltage range by the input voltage range.

Operation that can cause the amplifier to exceed its output voltage range should be handled with special caution. Except for devices including an output limiting or clamping function (CLC500, CLC501, CLC502), exceeding the output voltage range will result in saturation internal to the amplifier. In all cases, this will result in very slow recovery time from overdrive. Since the error signal, for current feedback, is a current back to the inverting input, saturating the output voltage so that it no longer fully supplies the current being set up in the gain setting resistor will cause a current to build up in the inverting input. This is analogous to a voltage developing across the inputs of a voltage feedback amplifier when overdriven. This inverting input current can also limit recovery time from saturation effects internal to the amplifier.

All of the monolithic amplifiers from Comlinear can handle this saturation without damage. Extreme overdrives at the inputs can, however, exceed the current handling capability of the inverting node at which point a voltage will start to build across the inputs. This can, if large enough, break down some internal junctions leading to an increase in noise and possibly a shift in the DC characteristics of the amplifier.

Unless specifically indicated as overdrive protected (CLC205, CLC206, CLC207, CLC560, CLC561), special care should be taken not to drive any of the hybrid amplifiers into output saturation. Intended for the widest band, high power operation, these parts have enough internal drive capability to potentially damage themselves under a saturated output condition. Although not noted in the data sheets, the CLC231 and CLC232 low gain hybrid amplifiers can also be output stage saturated without damage. Even with an output saturable capability, all of the hybrid amplifiers need a careful analysis of junction temperatures to ensure that they do not exceed the rated maximum of 175°C.

From these considerations, it is not recommended that these unprotected hybrid amps be used as comparators—with the output intentionally forced from supply rail to supply rail. (The fast recovery clamping of the CLC501 does, however, offer an excellent opportunity for a very flexible high speed comparator function.) It is also not recommended to increase the value of the output stage collector resistors, for those parts bringing the output transistor collectors out separately, to act as a current limit since this will only saturate the output stage sooner. Generally, these resistors are intended only to de-couple high speed load current transients from the rest of the amplifier to enhance high speed settling times. It is possible, however, to use these resistors as an output short ckt current limit for those parts indicated as being overdrive protected. And finally, when using adjustable gain circuits, particularly with switching FETs, take care to keep the amplifiers out of an open loop situation during gain adjust.

For situations requiring a robust output overdrive capability, the clamping amplifiers are by far the best choice.

6   Cascaded Amplifier Considerations

High gain, cascaded amplifier applications require particular attention to a number of parasitic and operational effects. Figure 13 shows an example circuit of 3-CLC401's configured for an overall gain of 1000 (60 dB) that will be used to demonstrate the suggestions developed here.

Several opportunities exist to develop an oscillator with very high gain, wideband circuits. The most common is direct output to input parasitic coupling. The output signal path should be physically isolated and, if necessary, shielded from the input signal path. When the final output is driving a relatively heavy AC load, either capacitive or, in this case, resistive (100Ω), high frequency load currents through the supplies can couple back into early stages completing an oscillatory feedback loop. High frequency de-coupling directly on the supply pins of each stage are required at a minimum.

Interstage ferrite beads on the supply rails, as shown in Figure 13, can also be used to attenuate this feedback path. The power supply connections of Figure 13 bring in the supplies at the final gain stage with LC PI filter stages used as it connects into earlier amplifier stages.

This provides increasing high frequency attenuation as we go to amplifier stages earlier on in the gain path. This is very desirable from both a PSRR standpoint and in breaking any feedback path through the power supplies from the output to input.

For close physically coupled amplifier stages, interstage matched impedances are probably not necessary. The two interstage 40Ω resistors of Figure 13 are intended to isolate the input capacitance of the next stage from the output of the previous stage as suggested earlier in the discussion of parasitic load capacitance effects.

One key concern in a very high gain path is the build-up of DC errors. The circuit of Figure 13 AC couples the gain setting resistors which reduces the DC gain to 1 for each amplifier stage. With only 1 mV input offset voltage at the first stage, the final amplifier output, (prior to the 6 dB matching loss), would be at 2V for this gain of 2000 if the 1 µF capacitors had not been used in the gain setting networks. If DC coupling at high gains is desired, some sort of composite correction loop should be considered, see *OA-07 Current Feedback Op Amp Applications Circuit Guide* (SNOA365).

As a general rule, the highest gain stage should be used as the first stage to limit the impact on the overall input noise of the noise contribution of succeeding stages. Here, the equivalent input noise of the 2nd two stages would be divided by the gain of +20 in the first stage in adding to overall equivalent input noise. The total equivalent input noise for the circuit of Figure 13 is 3 nV/$\sqrt{\text{Hz}}$. For a noise calculation discussion, see *OA-12 Noise Analysis for Comlinear Amplifiers Application Report* (SNOA375); for reducing the input noise for AC coupled applications, see *OA-14 Improving Amplifier Noise for High 3rd Intercept Amplifiers Application Report* (SNOA389).

Figure 14 shows the measured broadband gain and phase response for the circuit of Figure 13. Note that the measured −3 dB bandwidth, extending from 3 kHz to 200 MHz, achieves an equivalent 200 GHz Gain-Bandwidth product.
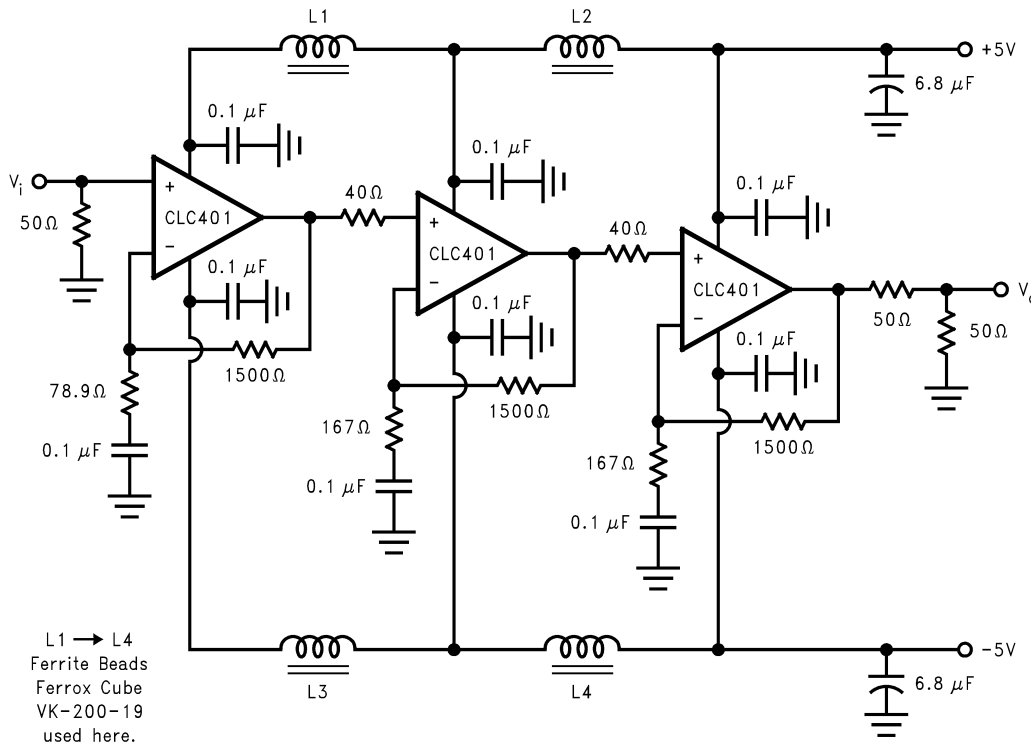
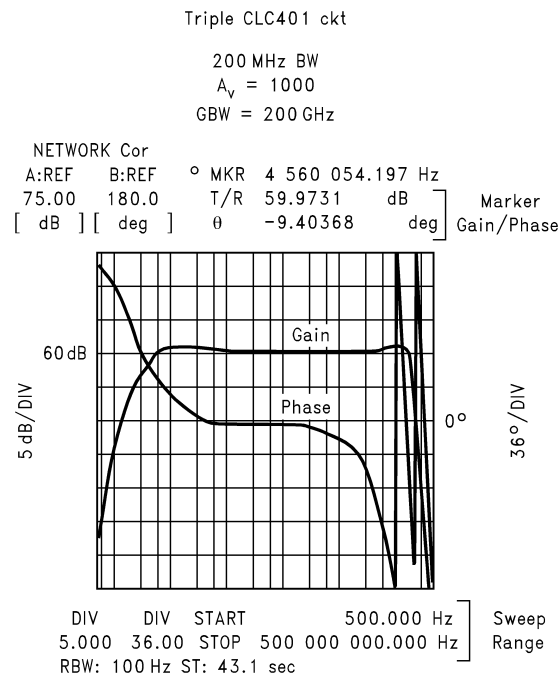**Figure 13. Wideband, High Gain, Cascaded Amplifiers**

Figure 14. Measured Gain and Phase for High Gain Cascaded Circuit

7 Conclusion

The circuits included in this application report have been tested with Texas Instruments parts that may have been obsoleted and/or replaced with newer products. Please refer to the CLC to LMH conversion table to find the appropriate replacement part for the obsolete device.

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