User's Guide

Ethernet PHY IBIS Models and Simulation User's Guide

ABSTRACT

This Users Guide demonstrates how to utilize TI's Ethernet PHY IBIS models to perform system level simulations of MAC interface timing. This guide will use the DP83TG720 IBIS model as an example, but the information applies to all other TI Ethernet PHY IBIS models.

Table of Contents

Trademarks

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1 Getting Started

IBIS models can be downloaded from their respective product page on ti.com, under the "Design tools & simulation" section. The following instructions will be utilizing the DP83TG720 IBIS model, found here.

Transient simulations can be performed in either HyperLynx or Keysight ADS, both of which will be demonstrated in the following sections.

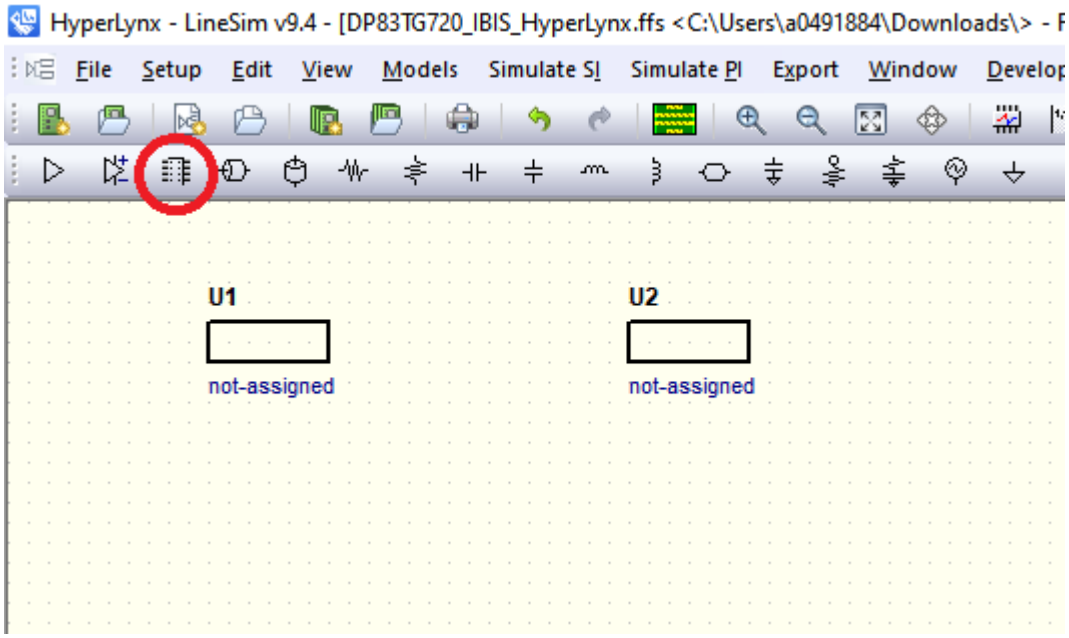
2 HyperLynx

2.1 Transient Simulations of RGMII

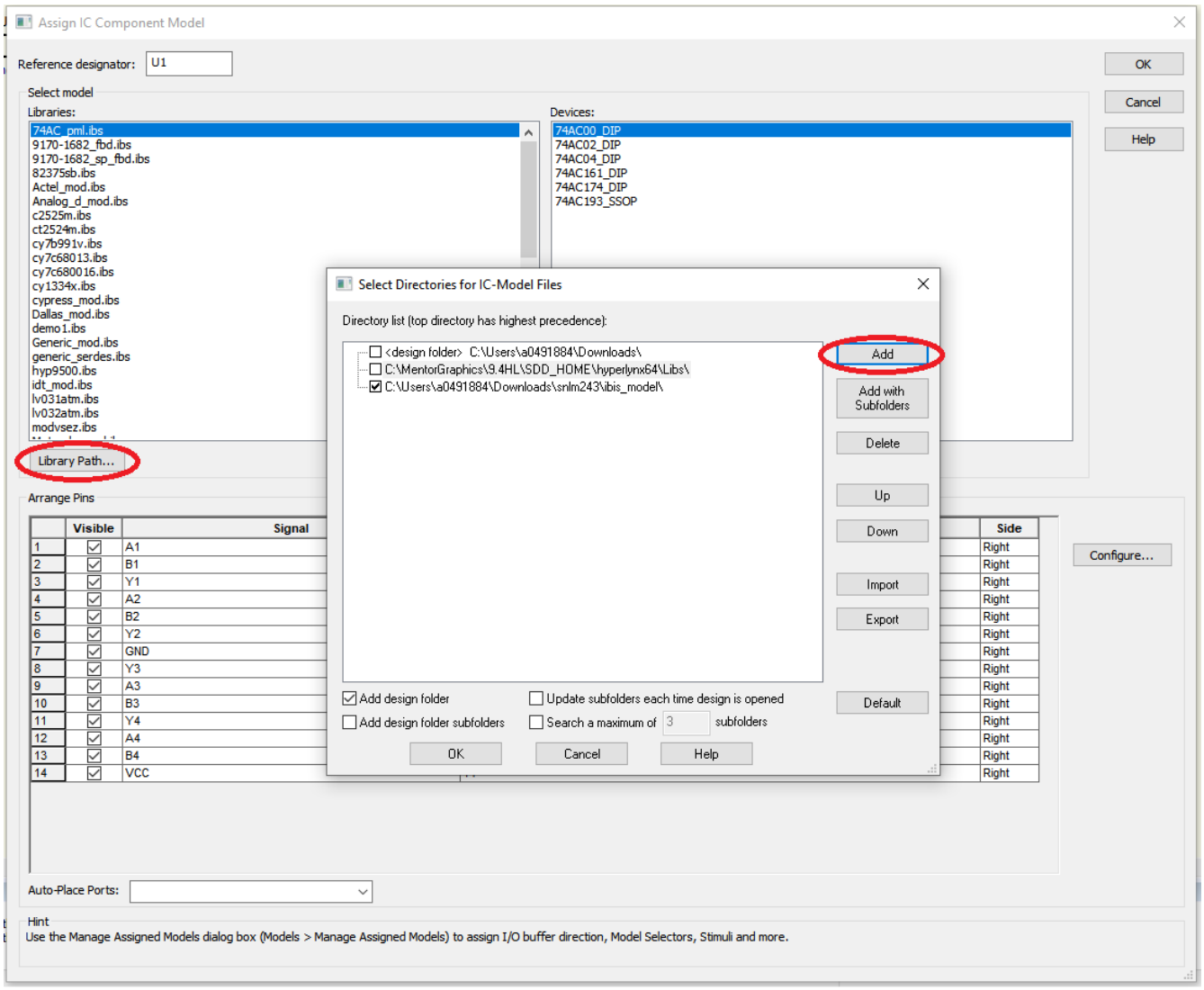
This section will demonstrate how to create simulations of RGMII signaling to verify timing specifications of any MAC interface.

2.1.1 Setup

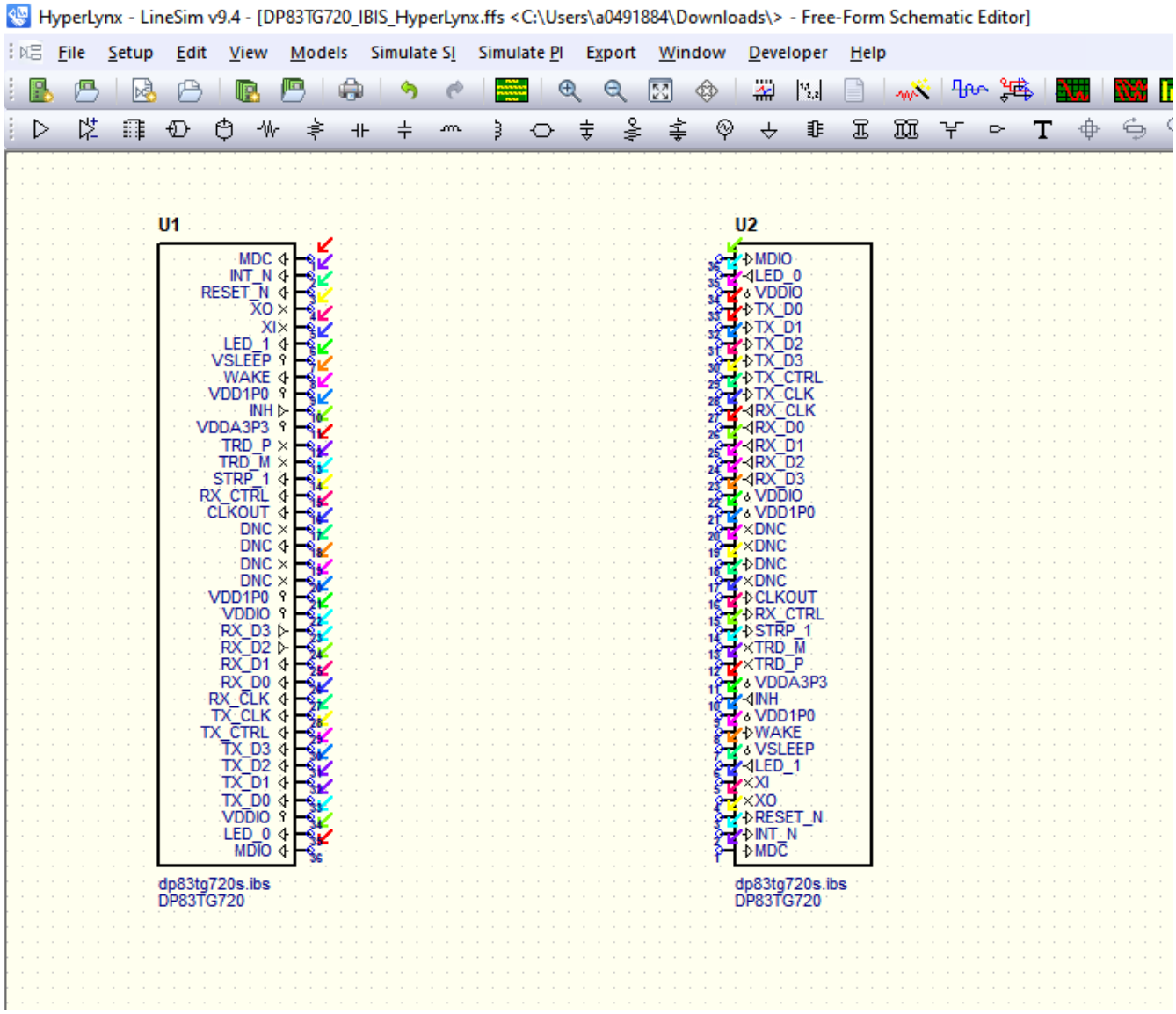
1. Open HyperLynx and create a new SI or SI/PI schematic.
2. Place two IC components from the toolbar.



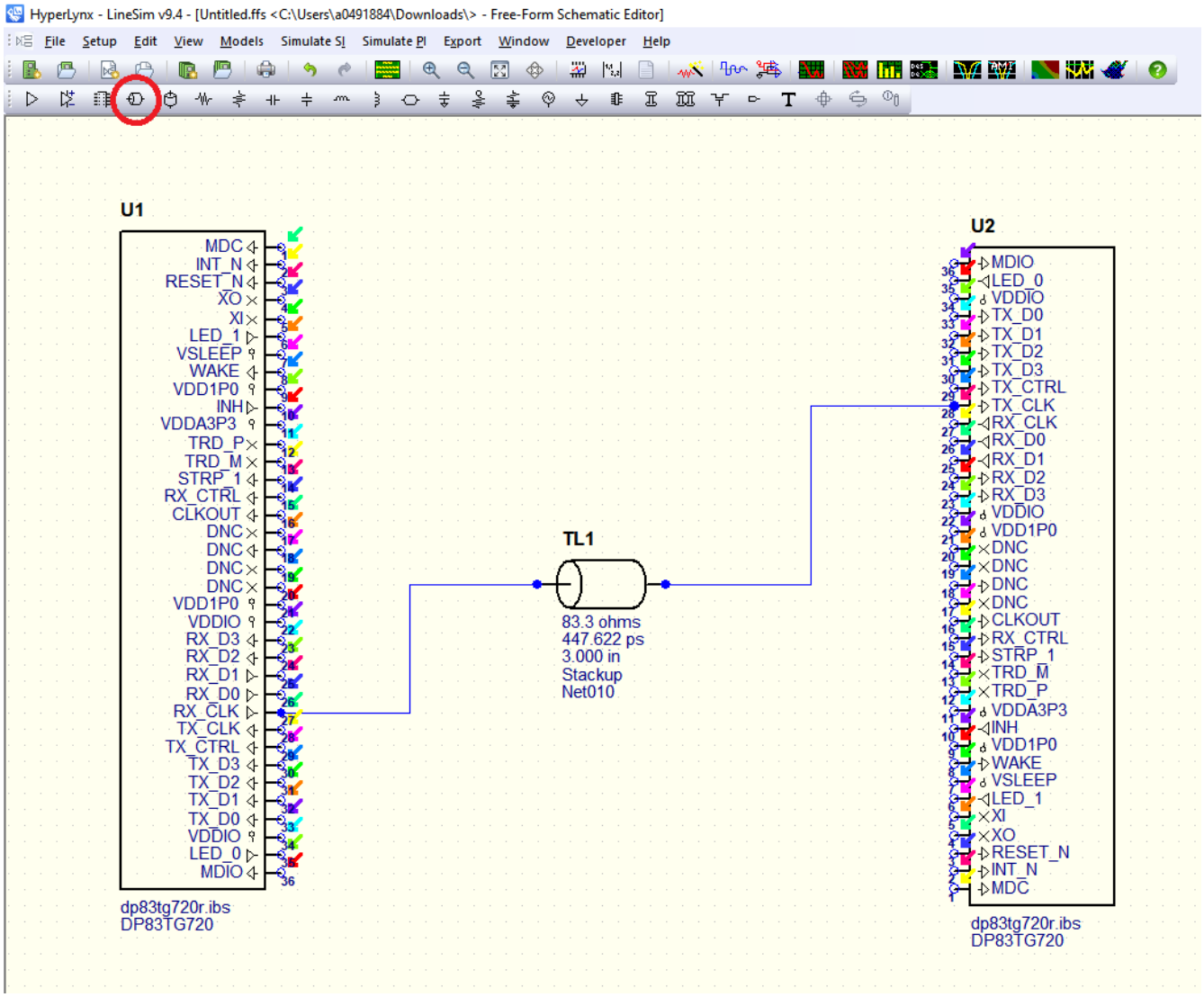
3. Double click each component. Click "Library Path..." then "Add" to specify the location of the dp83tg720r.ibs file. Click "OK".



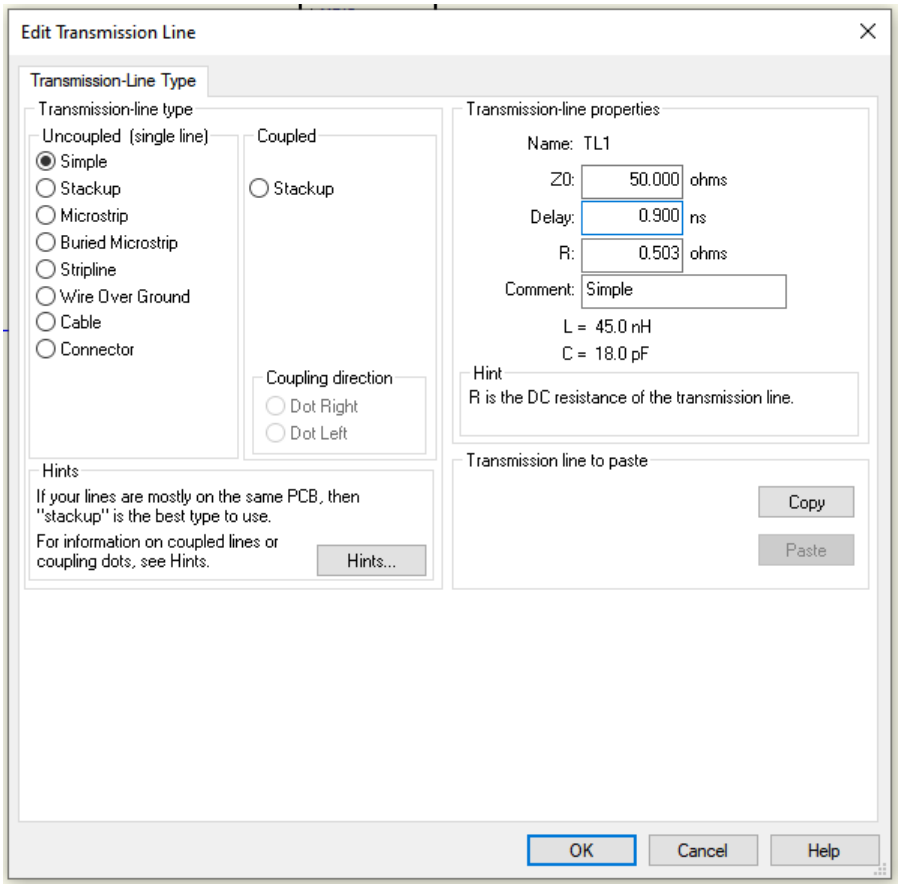
4. Select the dp83tg720r.ibs file and click Ok. Do the same for the other IC component. Right click on U2 and rotate twice.



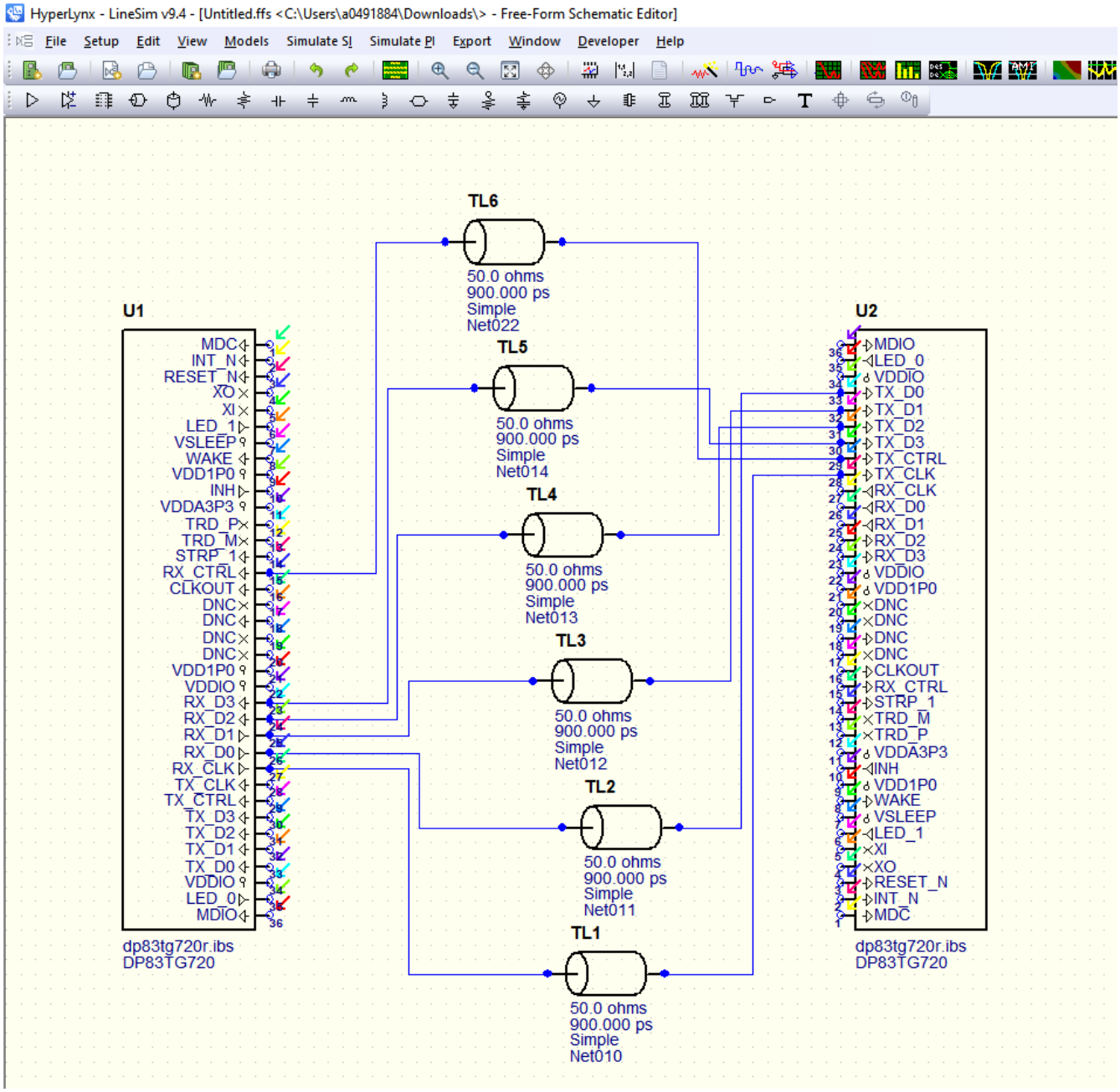
5. In this example, the RGMII connections will be made using an ideal transmission line as the channel. A following section will show how to upload custom S parameter files to simulation actual PCB designs. For now, place a transmission line component from the toolbar and use it to connect RX_CLK and TX_CLK as shown below.



6. Double click TL1 and change the type to Simple. Set the transmission line parameters as desired. Click "OK."



7. Copy and Paste TL1 five more times and make the following connections.



8. Right click U1 and select "Manage Model selectors, Buffer directions and Stimuli..." Specify the Model selector, I/O buffer direction, and Pin stimulus.

   Each pin in the IBIS file has several different selectable models, based on the operating levels of the power supplies and adjustable termination values. The DP83TG720 has adjustable impedance control for RGMII signaling pads and CLKOUT pin, to allow for slew rate control. Reference the readme_ibis_dp83tg720r.xlsx file to select which one to use. Slow and slowest modes will decrease the rise and fall times of each signal. The different models correspond to the cfg_mac_rx_impedance bits in register 0x0456, and cfg_other_impedance bits in register 0x455 in the data sheet.

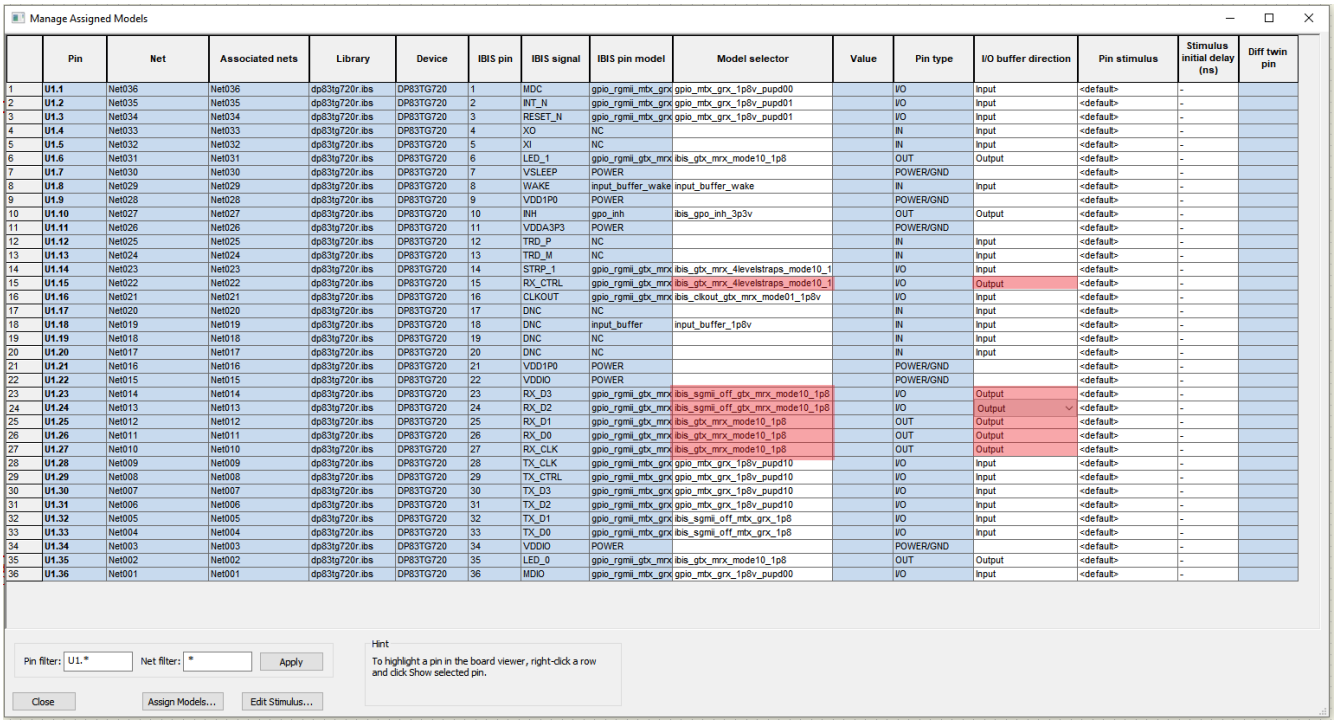
Table 7-69. IO_CONTROL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-5	cfg_mac_rx_impedance	R/W	8h	Slew Rate Control for RGMII pads - 01010b = Medium Slew (OA tr/tf compliant, max tr/tf = 1ns) 01011b = Slowest Slew (For low emissions, max tr/tf = 1.2ns) 01000b = Default mode (rgmii tr/tf compliant, max tr/tf=750ps)

Table 7-68. IO_CONTROL_2 Register Field Descriptions

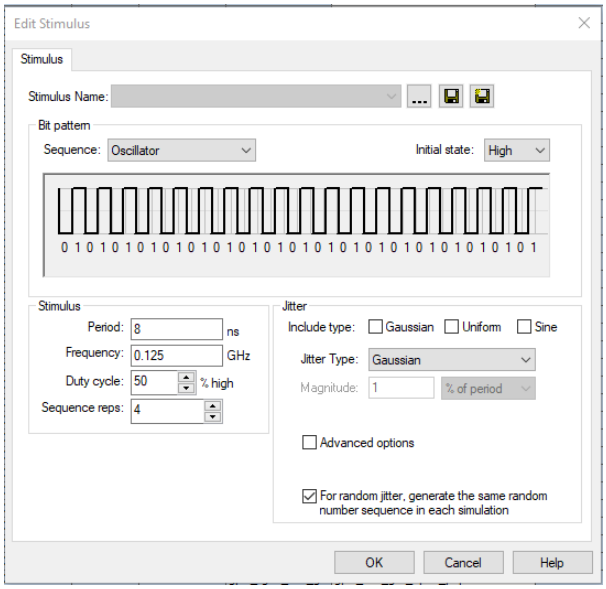
Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	
13-9	cfg_other_impedance	R/W	0h	Slew Rate Control for CLKOUT - 00000b = Default rise/fall time 00001b = Slower rise/fall time 00010b = Faster rise/fall time

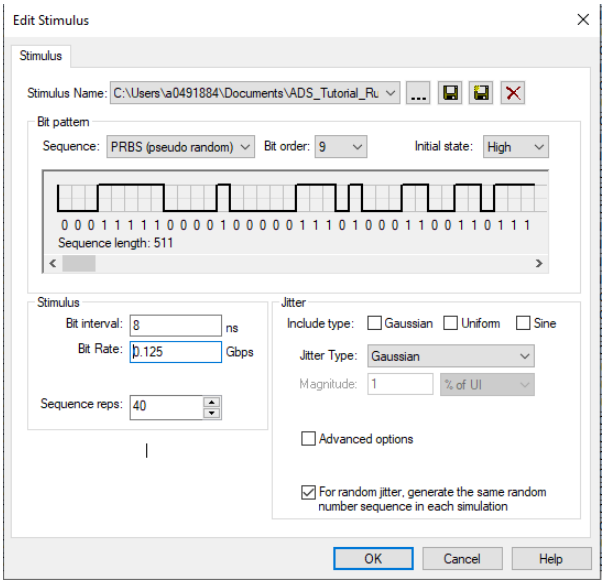
9. This case will use a Vddio level of 1.8V and default termination, so leave the default model selectors for each pin.
   Under the I/O buffer drop-down, select Output for all six of the relevant pins.

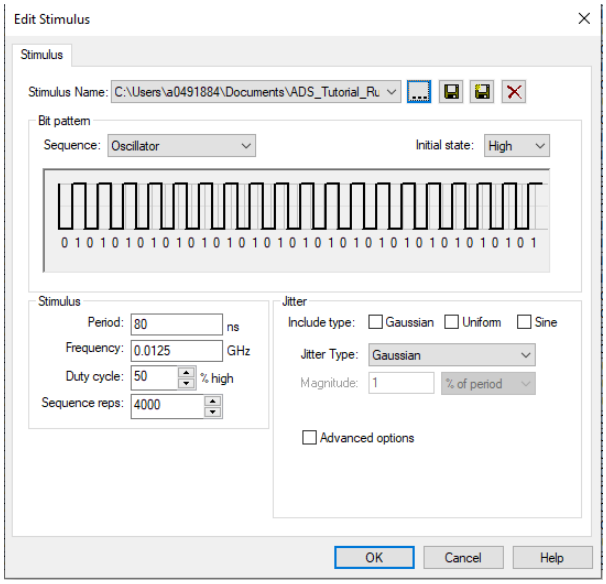


	Pin	Net	Associated nets	Library	Device	IBIS pin	IBIS signal	IBIS pin model	Model selector	Value	Pin type	I/O buffer direction	Pin stimulus	Stimulus initial delay (ns)	Diff twin pin
1	U1.1	Net036	Net036	dp83tg720r.ibs	DP83TG720	1	MDC	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd00		I/O	Input	<default>	-	
2	U1.2	Net035	Net035	dp83tg720r.ibs	DP83TG720	2	INT_N	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd01		I/O	Input	<default>	-	
3	U1.3	Net034	Net034	dp83tg720r.ibs	DP83TG720	3	RESET_N	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd01		I/O	Input	<default>	-	
4	U1.4	Net033	Net033	dp83tg720r.ibs	DP83TG720	4	XO	NC			IN	Input	<default>	-	
5	U1.5	Net032	Net032	dp83tg720r.ibs	DP83TG720	5	XI	NC			IN	Input	<default>	-	
6	U1.6	Net031	Net031	dp83tg720r.ibs	DP83TG720	6	LED_1	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_mode10_1p8		OUT	Output	<default>	-	
7	U1.7	Net030	Net030	dp83tg720r.ibs	DP83TG720	7	VSLEEP	POWER			POWER/GND		<default>	-	
8	U1.8	Net029	Net029	dp83tg720r.ibs	DP83TG720	8	WAKE	input_buffer_wake	input_buffer_wake		IN	Input	<default>	-	
9	U1.9	Net028	Net028	dp83tg720r.ibs	DP83TG720	9	VDD1P0	POWER			POWER/GND		<default>	-	
10	U1.10	Net027	Net027	dp83tg720r.ibs	DP83TG720	10	INH	gpo_inh	ibis_gpo_inh_3p3v		OUT	Output	<default>	-	
11	U1.11	Net026	Net026	dp83tg720r.ibs	DP83TG720	11	VDDA3P3	POWER			POWER/GND		<default>	-	
12	U1.12	Net025	Net025	dp83tg720r.ibs	DP83TG720	12	TRD_P	NC			IN	Input	<default>	-	
13	U1.13	Net024	Net024	dp83tg720r.ibs	DP83TG720	13	TRD_M	NC			IN	Input	<default>	-	
14	U1.14	Net023	Net023	dp83tg720r.ibs	DP83TG720	14	STRP_1	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_4levelstraps_mode10_1		I/O	Input	<default>	-	
15	U1.15	Net022	Net022	dp83tg720r.ibs	DP83TG720	15	RX_CTRL	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_4levelstraps_mode10_1		I/O	Output	<default>	-	
16	U1.16	Net021	Net021	dp83tg720r.ibs	DP83TG720	16	CLKOUT	gpio_rgmii_gtx_mrx	ibis_clkout_gtx_mrx_mode01_1p8v		I/O	Input	<default>	-	
17	U1.17	Net020	Net020	dp83tg720r.ibs	DP83TG720	17	DNC	NC			IN	Input	<default>	-	
18	U1.18	Net019	Net019	dp83tg720r.ibs	DP83TG720	18	DNC	input_buffer	input_buffer_1p8v		IN	Input	<default>	-	
19	U1.19	Net018	Net018	dp83tg720r.ibs	DP83TG720	19	DNC	NC			IN	Input	<default>	-	
20	U1.20	Net017	Net017	dp83tg720r.ibs	DP83TG720	20	DNC	NC			IN	Input	<default>	-	
21	U1.21	Net016	Net016	dp83tg720r.ibs	DP83TG720	21	VDD1P0	POWER			POWER/GND		<default>	-	
22	U1.22	Net015	Net015	dp83tg720r.ibs	DP83TG720	22	VDDIO	POWER			POWER/GND		<default>	-	
23	U1.23	Net014	Net014	dp83tg720r.ibs	DP83TG720	23	RX_D3	gpio_rgmii_gtx_mrx	ibis_sgmii_off_gtx_mrx_mode10_1p8		I/O	Output	<default>	-	
24	U1.24	Net013	Net013	dp83tg720r.ibs	DP83TG720	24	RX_D2	gpio_rgmii_gtx_mrx	ibis_sgmii_off_gtx_mrx_mode10_1p8		I/O	Output	<default>	-	
25	U1.25	Net012	Net012	dp83tg720r.ibs	DP83TG720	25	RX_D1	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_mode10_1p8		OUT	Output	<default>	-	
26	U1.26	Net011	Net011	dp83tg720r.ibs	DP83TG720	26	RX_D0	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_mode10_1p8		OUT	Output	<default>	-	
27	U1.27	Net010	Net010	dp83tg720r.ibs	DP83TG720	27	RX_CLK	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_mode10_1p8		OUT	Output	<default>	-	
28	U1.28	Net009	Net009	dp83tg720r.ibs	DP83TG720	28	TX_CLK	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd10		I/O	Input	<default>	-	
29	U1.29	Net008	Net008	dp83tg720r.ibs	DP83TG720	29	TX_CTRL	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd10		I/O	Input	<default>	-	
30	U1.30	Net007	Net007	dp83tg720r.ibs	DP83TG720	30	TX_D3	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd10		I/O	Input	<default>	-	
31	U1.31	Net006	Net006	dp83tg720r.ibs	DP83TG720	31	TX_D2	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd10		I/O	Input	<default>	-	
32	U1.32	Net005	Net005	dp83tg720r.ibs	DP83TG720	32	TX_D1	gpio_rgmii_mtx_grx	ibis_sgmii_off_mtx_grx_1p8		I/O	Input	<default>	-	
33	U1.33	Net004	Net004	dp83tg720r.ibs	DP83TG720	33	TX_D0	gpio_rgmii_mtx_grx	ibis_sgmii_off_mtx_grx_1p8		I/O	Input	<default>	-	
34	U1.34	Net003	Net003	dp83tg720r.ibs	DP83TG720	34	VDDIO	POWER			POWER/GND		<default>	-	
35	U1.35	Net002	Net002	dp83tg720r.ibs	DP83TG720	35	LED_0	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_mode10_1p8		OUT	Output	<default>	-	
36	U1.36	Net001	Net001	dp83tg720r.ibs	DP83TG720	36	MDIO	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd00		I/O	Input	<default>	-	

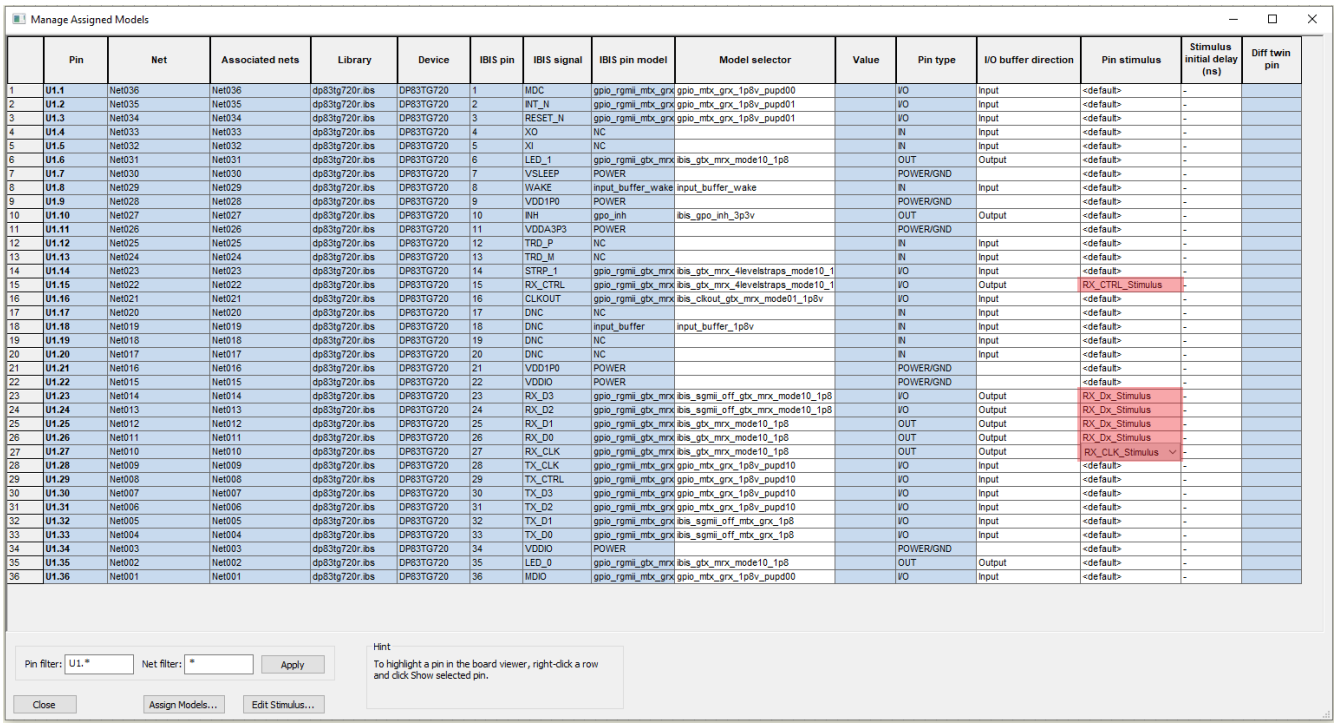
10. Click the "Edit Stimulus..." button in the lower left corner. Create an oscillator stimulus for the RX_CLK output, and PRBS stimulus for the RX_Dx outputs to emulate actual RGMII data transmission.
11. To emulate the RX_CLK signal, select “Oscillator” from the drop down menu, and enter a frequency of 0.125GHz, and increase the sequence reps to 4000. Click the Save button and save this as “RX_CLK _Stimulus.eds”
    Change the sequence dropdown to PRBS. Select bit order 9. Save this file as “RX_Dx_Stimulus.eds”
    Finally, create a 12.5MHz oscillator for the RX_CTRL output and name it.
    “RX_CTRL_Stimulus.eds”







12. Click "OK" to return to the previous screen, and assign the new stimuli to their respective pins. Click the close button.

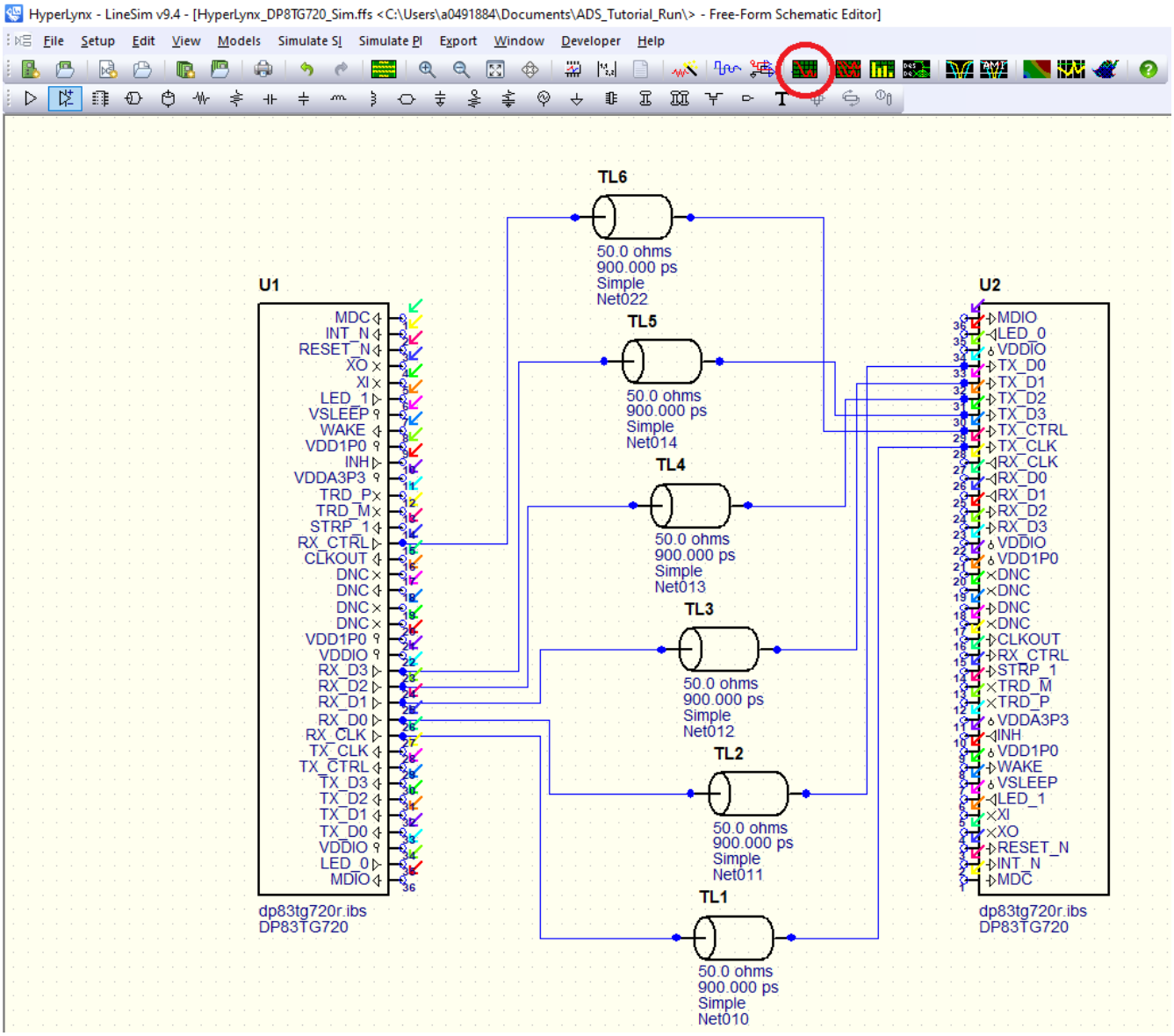


	Pin	Net	Associated nets	Library	Device	IBIS pin	IBIS signal	IBIS pin model	Model selector	Value	Pin type	I/O buffer direction	Pin stimulus	Stimulus initial delay (ns)	Diff twin pin
1	U1.1	Net036	Net036	dp83tg720r.ibs	DP83TG720	1	MDC	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd00		I/O	Input	<default>	-	
2	U1.2	Net035	Net035	dp83tg720r.ibs	DP83TG720	2	INT_N	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd01		I/O	Input	<default>	-	
3	U1.3	Net034	Net034	dp83tg720r.ibs	DP83TG720	3	RESET_N	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd01		I/O	Input	<default>	-	
4	U1.4	Net033	Net033	dp83tg720r.ibs	DP83TG720	4	XO	NC			IN	Input	<default>	-	
5	U1.5	Net032	Net032	dp83tg720r.ibs	DP83TG720	5	XI	NC			IN	Input	<default>	-	
6	U1.6	Net031	Net031	dp83tg720r.ibs	DP83TG720	6	LED_1	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_mode10_1p8		OUT	Output	<default>	-	
7	U1.7	Net030	Net030	dp83tg720r.ibs	DP83TG720	7	VSLEEP	POWER			POWER/GND		<default>	-	
8	U1.8	Net029	Net029	dp83tg720r.ibs	DP83TG720	8	WAKE	input_buffer_wake	input_buffer_wake		IN	Input	<default>	-	
9	U1.9	Net028	Net028	dp83tg720r.ibs	DP83TG720	9	VDD1P0	POWER			POWER/GND		<default>	-	
10	U1.10	Net027	Net027	dp83tg720r.ibs	DP83TG720	10	INH	gpo_inh	ibis_gpo_inh_3p3v		OUT	Output	<default>	-	
11	U1.11	Net026	Net026	dp83tg720r.ibs	DP83TG720	11	VDDA3P3	POWER			POWER/GND		<default>	-	
12	U1.12	Net025	Net025	dp83tg720r.ibs	DP83TG720	12	TRD_P	NC			IN	Input	<default>	-	
13	U1.13	Net024	Net024	dp83tg720r.ibs	DP83TG720	13	TRD_M	NC			IN	Input	<default>	-	
14	U1.14	Net023	Net023	dp83tg720r.ibs	DP83TG720	14	STRP_1	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_4levelstraps_mode10_1		I/O	Input	<default>	-	
15	U1.15	Net022	Net022	dp83tg720r.ibs	DP83TG720	15	RX_CTRL	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_4levelstraps_mode10_1		I/O	Output	RX_CTRL_Stimulus	-	
16	U1.16	Net021	Net021	dp83tg720r.ibs	DP83TG720	16	CLKOUT	gpio_rgmii_gtx_mrx	ibis_clkout_gtx_mrx_mode01_1p8v		I/O	Input	<default>	-	
17	U1.17	Net020	Net020	dp83tg720r.ibs	DP83TG720	17	DNC	NC			IN	Input	<default>	-	
18	U1.18	Net019	Net019	dp83tg720r.ibs	DP83TG720	18	DNC	input_buffer	input_buffer_1p8v		IN	Input	<default>	-	
19	U1.19	Net018	Net018	dp83tg720r.ibs	DP83TG720	19	DNC	NC			IN	Input	<default>	-	
20	U1.20	Net017	Net017	dp83tg720r.ibs	DP83TG720	20	DNC	NC			IN	Input	<default>	-	
21	U1.21	Net016	Net016	dp83tg720r.ibs	DP83TG720	21	VDD1P0	POWER			POWER/GND		<default>	-	
22	U1.22	Net015	Net015	dp83tg720r.ibs	DP83TG720	22	VDDIO	POWER			POWER/GND		<default>	-	
23	U1.23	Net014	Net014	dp83tg720r.ibs	DP83TG720	23	RX_D3	gpio_rgmii_gtx_mrx	ibis_sgmii_off_gtx_mrx_mode10_1p8		I/O	Output	RX_Dx_Stimulus	-	
24	U1.24	Net013	Net013	dp83tg720r.ibs	DP83TG720	24	RX_D2	gpio_rgmii_gtx_mrx	ibis_sgmii_off_gtx_mrx_mode10_1p8		I/O	Output	RX_Dx_Stimulus	-	
25	U1.25	Net012	Net012	dp83tg720r.ibs	DP83TG720	25	RX_D1	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_mode10_1p8		OUT	Output	RX_Dx_Stimulus	-	
26	U1.26	Net011	Net011	dp83tg720r.ibs	DP83TG720	26	RX_D0	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_mode10_1p8		OUT	Output	RX_Dx_Stimulus	-	
27	U1.27	Net010	Net010	dp83tg720r.ibs	DP83TG720	27	RX_CLK	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_mode10_1p8		OUT	Output	RX_CLK_Stimulus	-	
28	U1.28	Net009	Net009	dp83tg720r.ibs	DP83TG720	28	TX_CLK	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd10		I/O	Input	<default>	-	
29	U1.29	Net008	Net008	dp83tg720r.ibs	DP83TG720	29	TX_CTRL	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd10		I/O	Input	<default>	-	
30	U1.30	Net007	Net007	dp83tg720r.ibs	DP83TG720	30	TX_D3	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd10		I/O	Input	<default>	-	
31	U1.31	Net006	Net006	dp83tg720r.ibs	DP83TG720	31	TX_D2	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd10		I/O	Input	<default>	-	
32	U1.32	Net005	Net005	dp83tg720r.ibs	DP83TG720	32	TX_D1	gpio_rgmii_mtx_grx	ibis_sgmii_off_mtx_grx_1p8		I/O	Input	<default>	-	
33	U1.33	Net004	Net004	dp83tg720r.ibs	DP83TG720	33	TX_D0	gpio_rgmii_mtx_grx	ibis_sgmii_off_mtx_grx_1p8		I/O	Input	<default>	-	
34	U1.34	Net003	Net003	dp83tg720r.ibs	DP83TG720	34	VDDIO	POWER			POWER/GND		<default>	-	
35	U1.35	Net002	Net002	dp83tg720r.ibs	DP83TG720	35	LED_0	gpio_rgmii_gtx_mrx	ibis_gtx_mrx_mode10_1p8		OUT	Output	<default>	-	
36	U1.36	Net001	Net001	dp83tg720r.ibs	DP83TG720	36	MDIO	gpio_rgmii_mtx_grx	gpio_mtx_grx_1p8v_pupd00		I/O	Input	<default>	-	

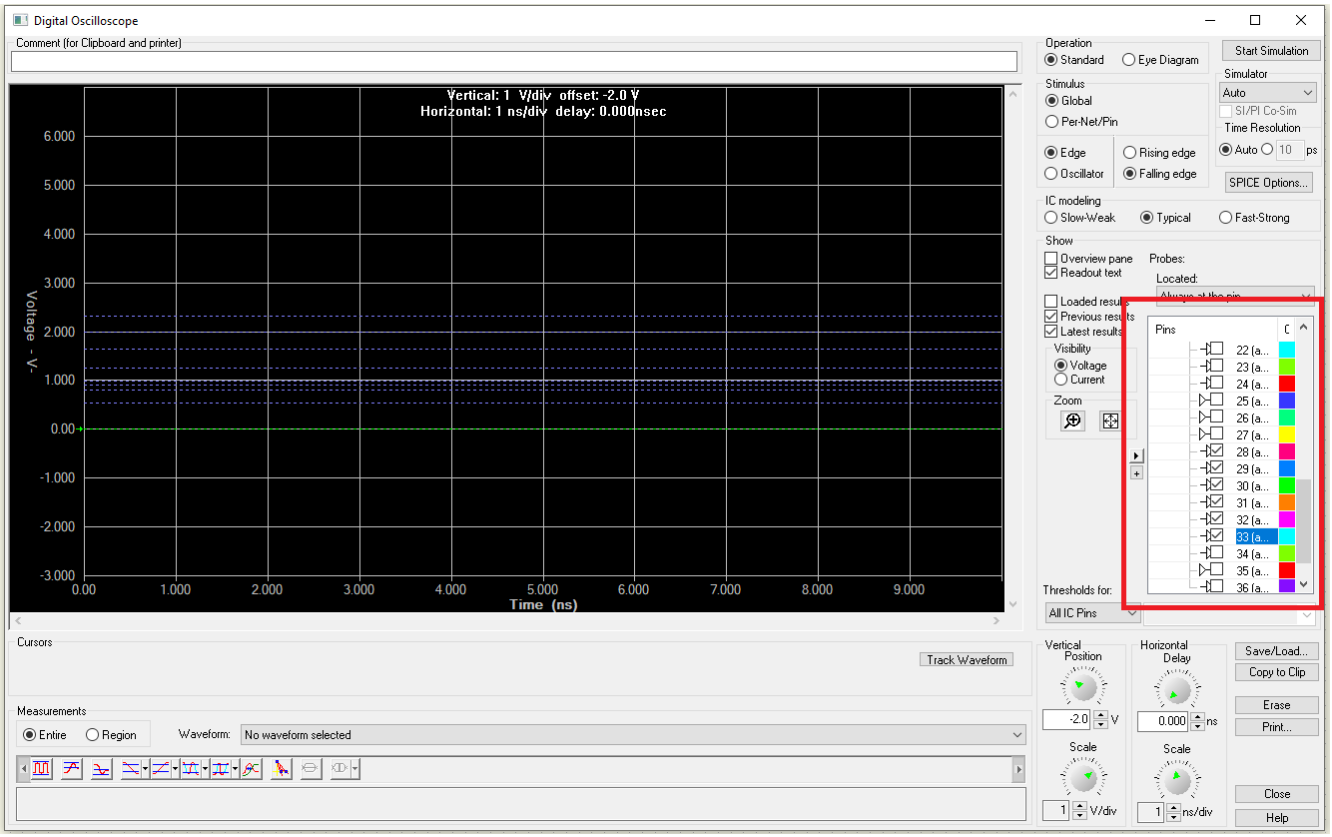
13. No additional configuration is required on U2, but confirm that the connected pins are selected as inputs. The model is now ready to simulate.

2.1.2 Measurements

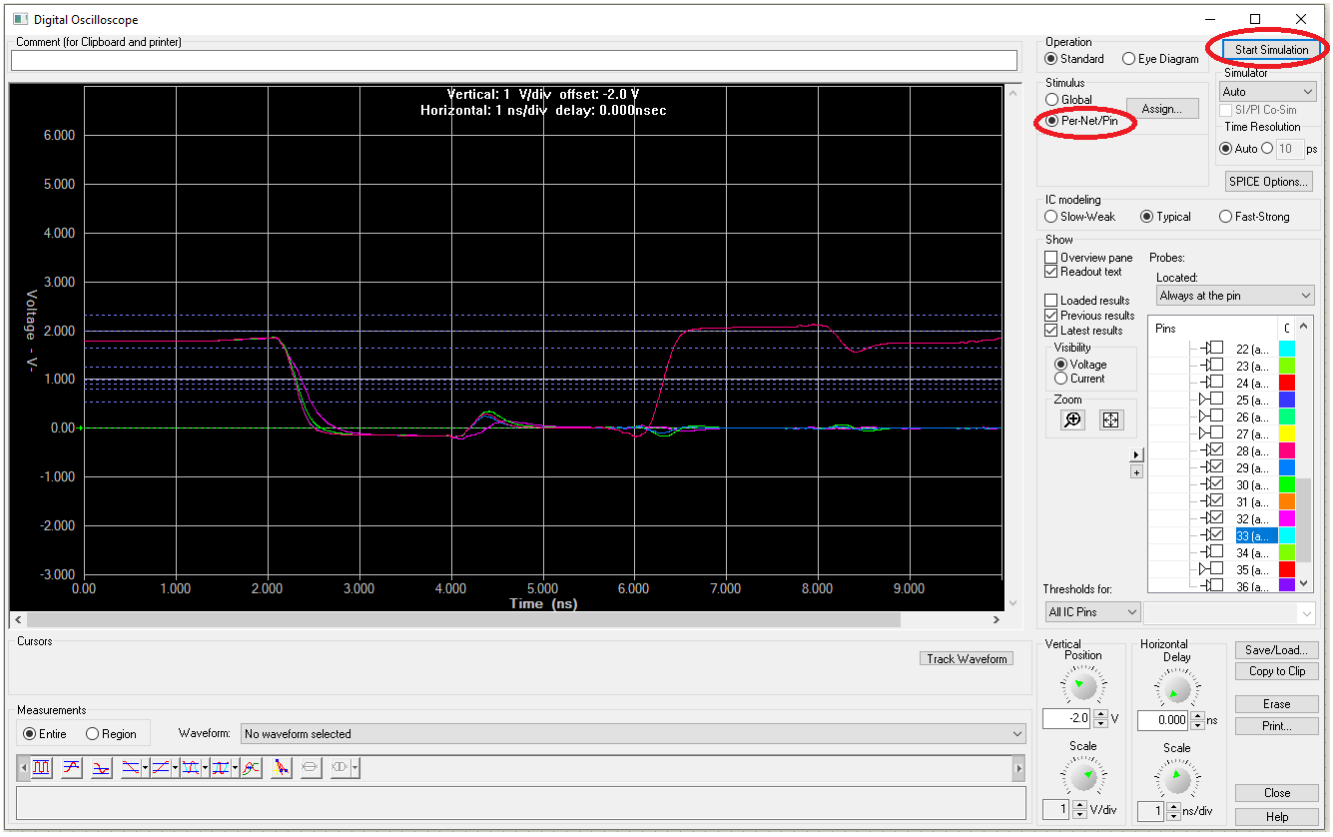
1. Click the button in the toolbar to open the waveform window.



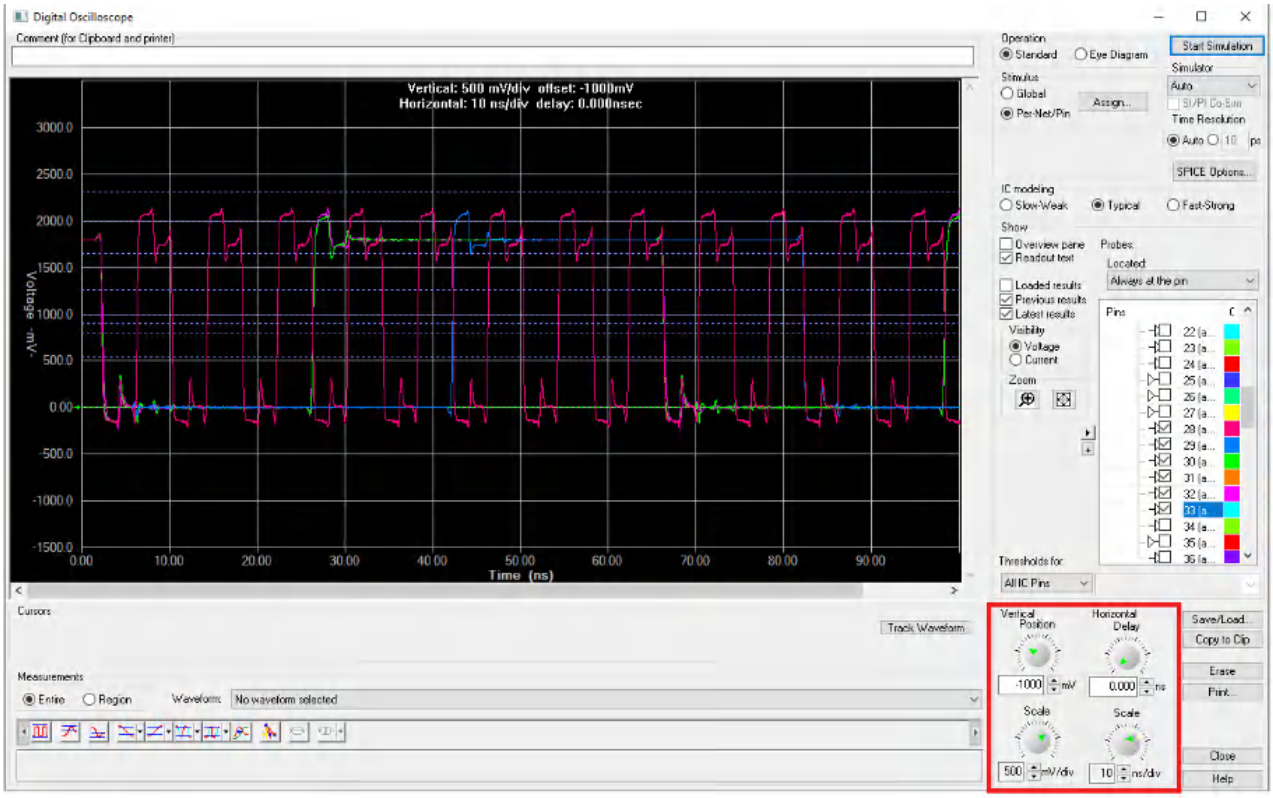
2. Select which pins to view waveforms of. Click the triangle to the left of the pins box and click "Disable all probes." Select pins 28-33 on U2.



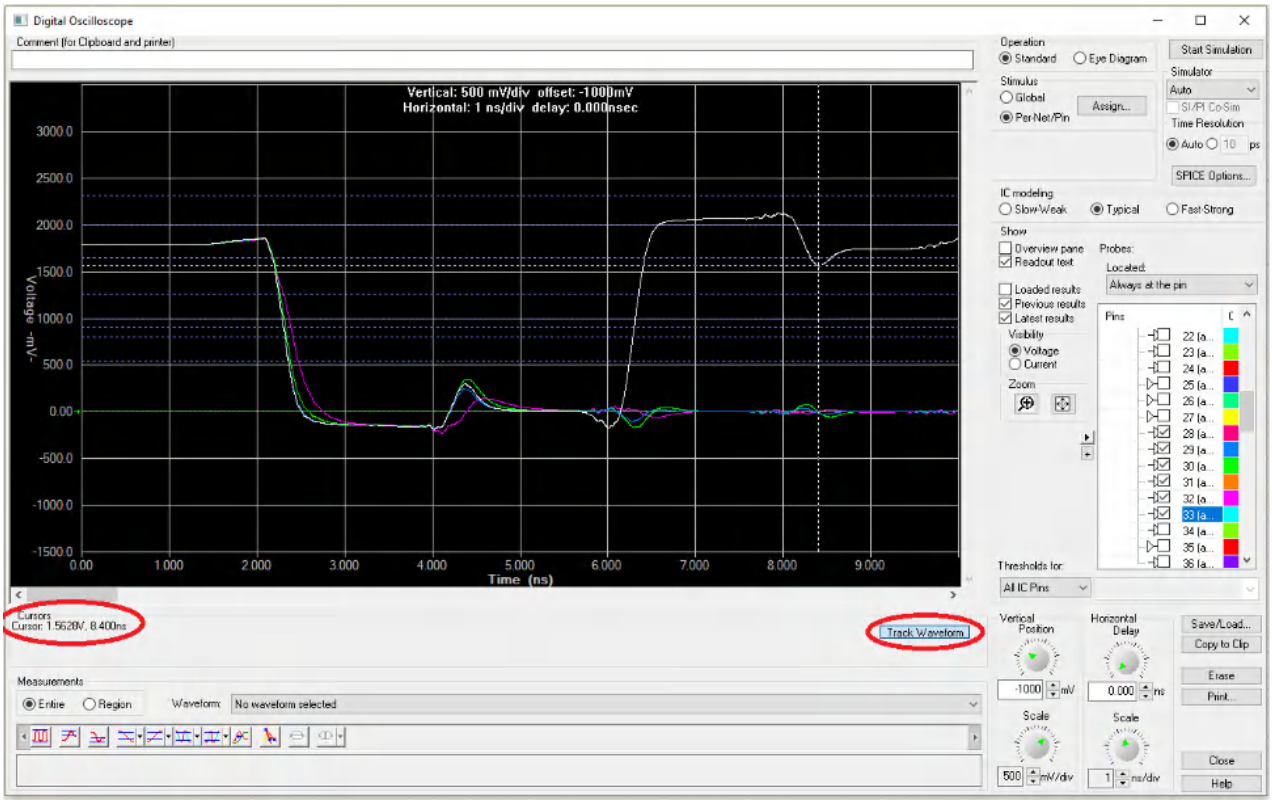
3. Under the stimulus selector, choose "Per-Net/Pin" to allow the individual stimuli selected earlier. Click the Start Simulation button. The following waveforms will appear.



4. Use the up and down arrows under the dials to adjust the view of the waveform.



5. Any time or voltage value can be gathered from this plot manually. Click the Track Waveform button and click on a waveform. The cursor information will be shown here.



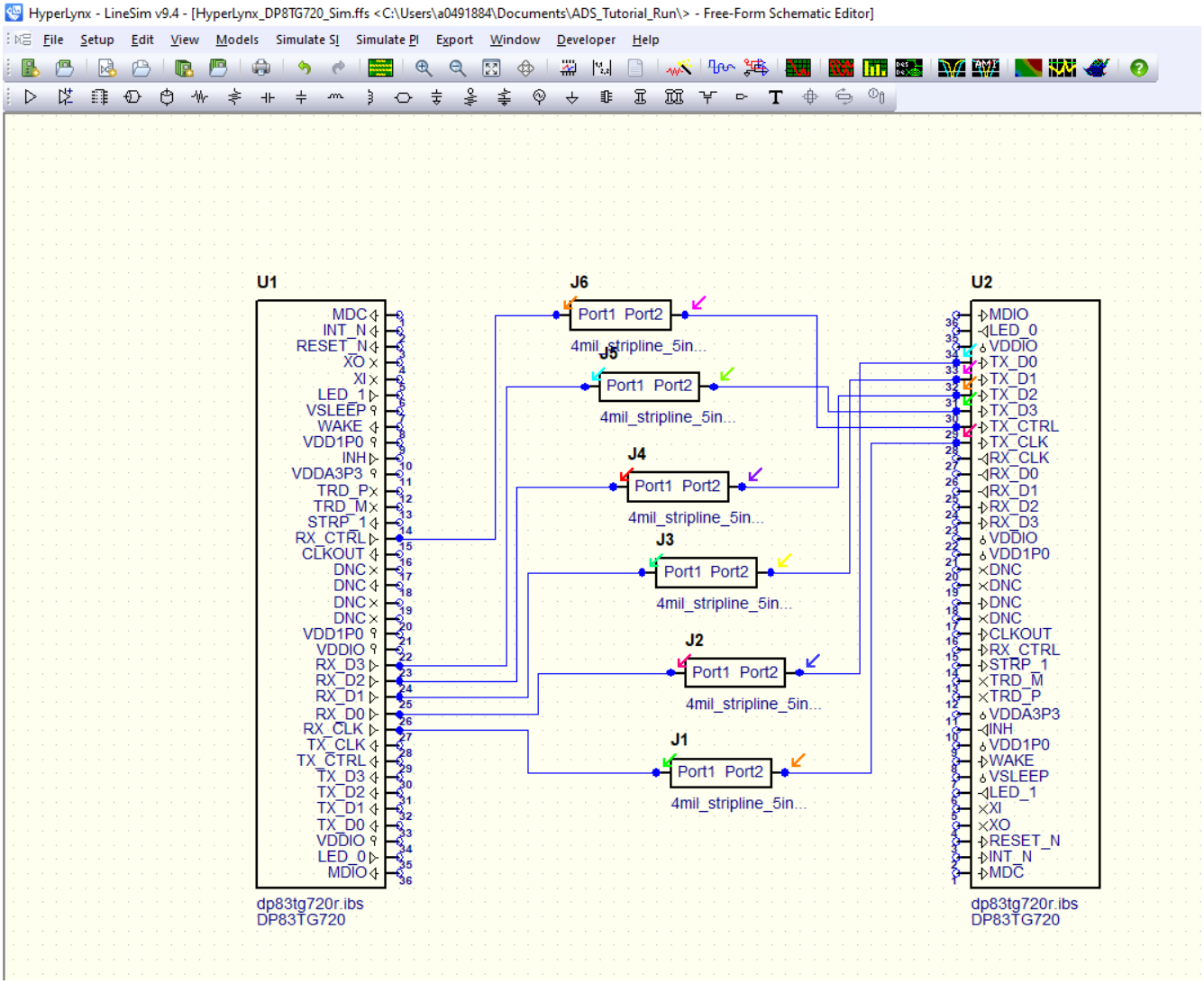
6. To acquire automatic measurements, select a waveform and measurement option in the bottom left. Options include peak-to-peak voltage, rise/fall times, positive/negative overshoot, etc.

2.1.3 Further Configuration

The previous sections cover the basics of HyperLynx simulations. Additional configuration options follow. By default, the previous waveforms are shown to allow an easy comparison of any changes made.

1. Change the IC modeling option to Slow-Weak or Fast-Strong. Notice the rise/fall times increase and decrease respectively, and there is less and more overshoot respectively. This setting is used to simulate all process corners of silicon manufacturing.
2. Set the location at the pin or at the die. This will choose whether to include the package characteristics or not.
3. Go back to the main window and change the model selector or stimuli for the desired pins.
4. Change the transmission line characteristics

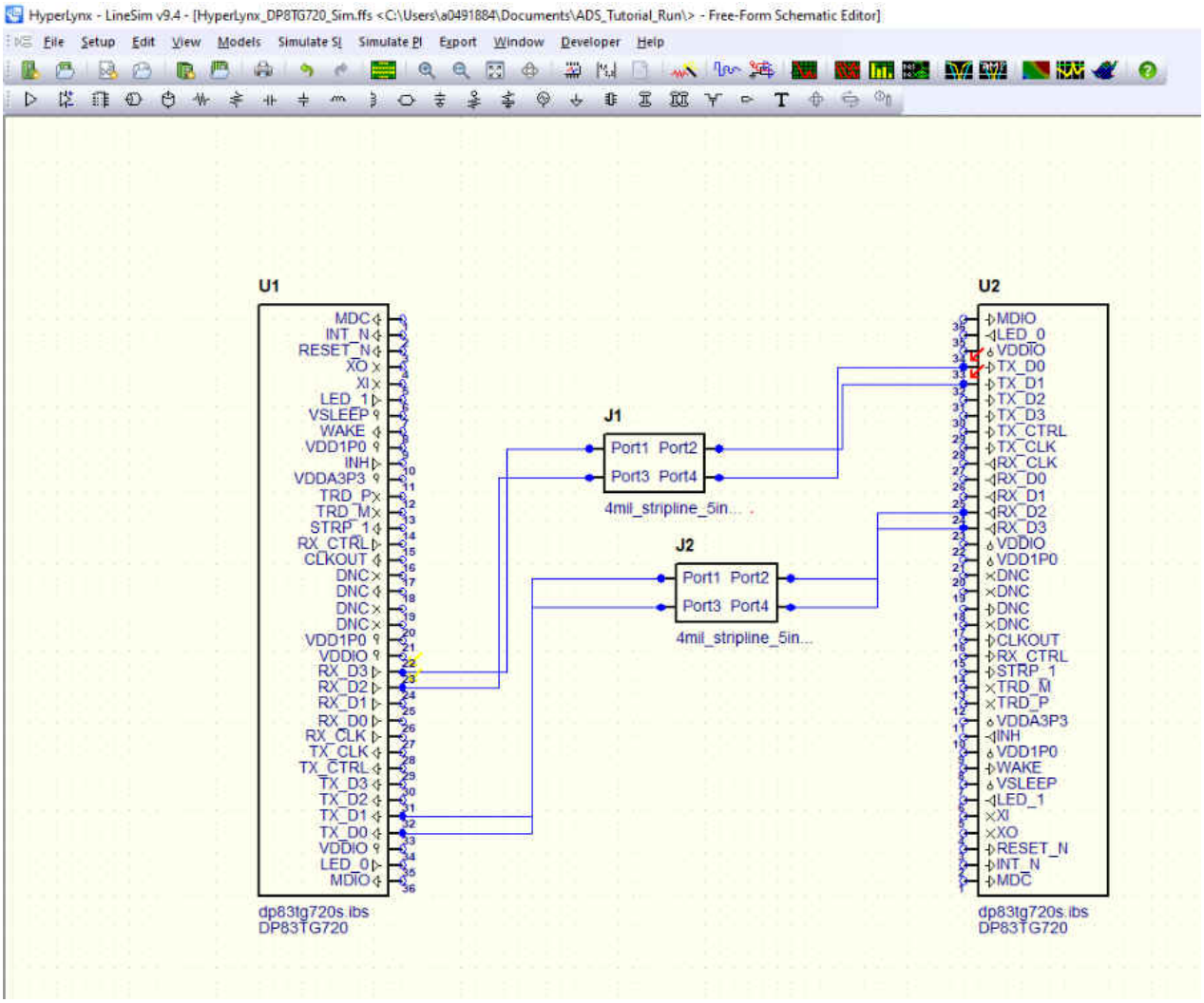
In most cases, it will be beneficial to use actual S-Parameters of PCB traces instead of ideal transmission lines. Select the S-Parameter option from the toolbar and replace each transmission line with this. Double click the J1 item and select your desired S-Parameter file. This example is using a 5 inch, 4 mil FR4 trace file. Return to the simulation window and re-simulate.



2.2 SGMII Differential Simulation

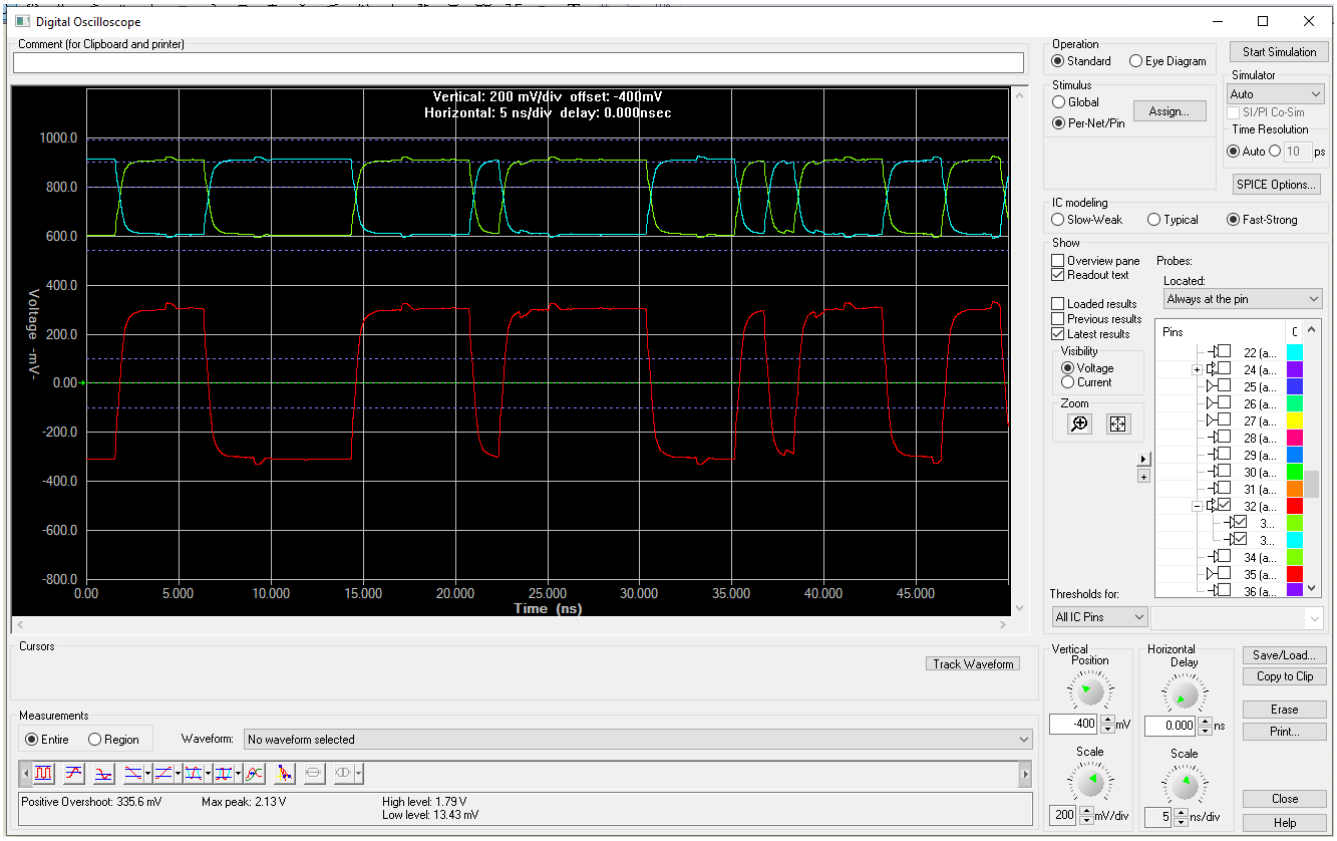
This example will show how to simulate the SGMII differential interface. Most of the configuration will be the same as the above example, so refer to the previous section for more detailed direction.

1. Create a schematic in this fashion, using an S4P model of a differential FR4 trace for the transmission line.



2. Double click U1 and U2 and select the dp83tg720s.ibs model.
3. Open the Manage model selector window for U1. Notice pins 23 and 24 have the ibis_sgmii_tx model selected, and are notated as a diff twin pair.
4. Create a 625MHz PRBS-9 stimuli for the SGMII pins and assign them to pins 23 and 24.

5. Open the simulation window and select the box next to pin 32. The Blue and Green traces show the individual trace waveforms, while the red shows math (pin 32 – pin 33).



6. Take measurements and change the configuration as desired.

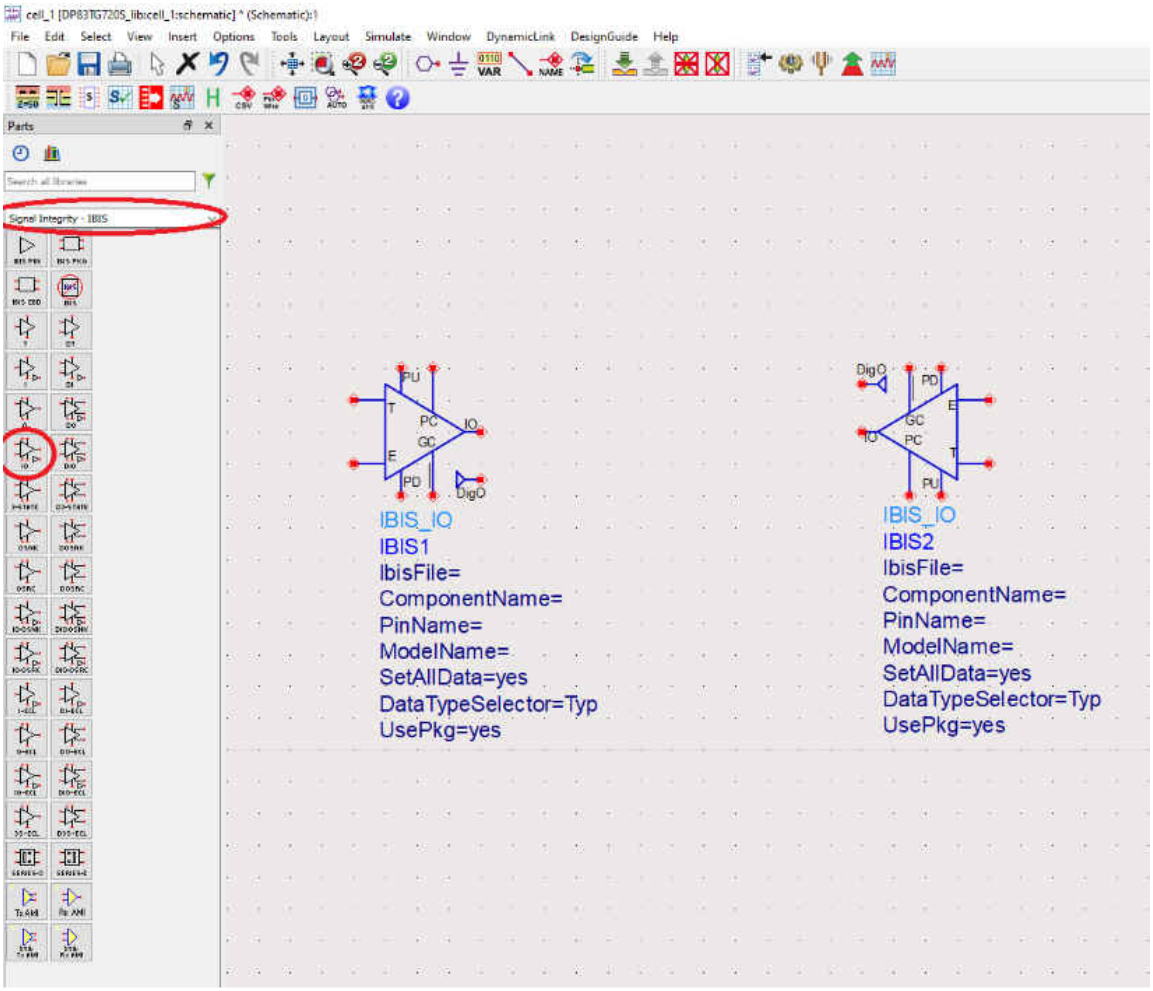
3 Keysight ADS

3.1 Transient Simulations of RGMII

This section will demonstrate how to create simulations of RGMII signaling in ADS to verify timing specifications of any MAC interface.

3.1.1 Setup

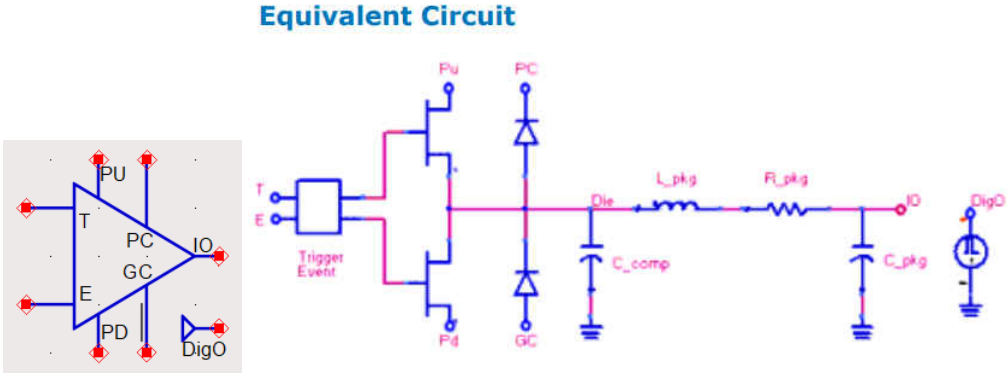
1. Create a new schematic and navigate to the Signal Integrity – IBIS palette in the drop-down. Select the IO component and place two. This example will demonstrate the RX_CLK to TX_CLK connection.



2. Double click the IO component and select the dp83tg720r.ibs file for both components.
3. This component functions as either the IBIS_O (Output) buffer or the IBIS_I (Input) buffer depending on the enable state. When the buffer is enabled, it functions as an IBIS_O (Output) buffer. When disabled, it behaves as an IBIS_I (Input) buffer.

   In the Input mode, the DigIO pin assumes the value 0 or 1 depending on the voltage at the IO pin compared to the model's Vinl and Vinh parameters.

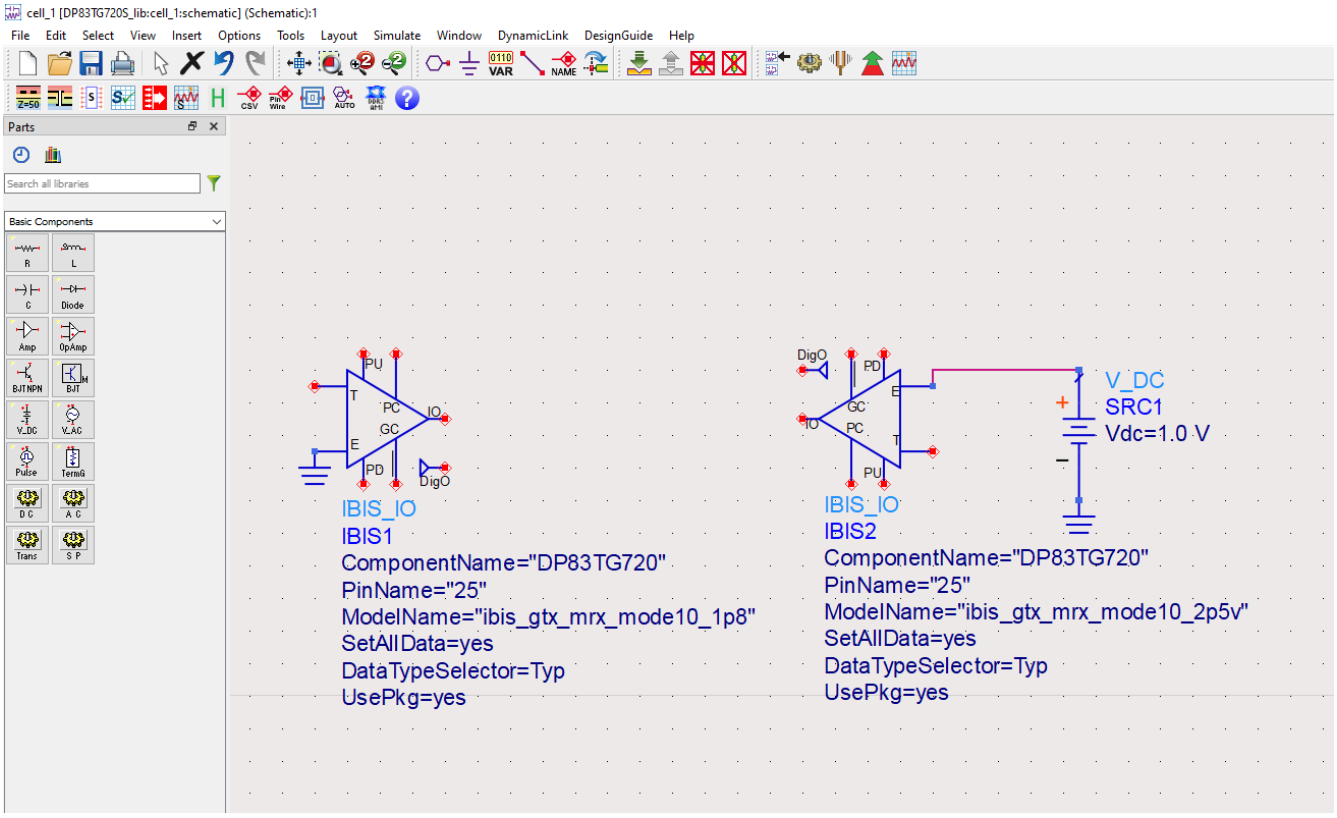
   Further description of all the IBIS components available in ADS can be found here:



4. Next, wire each one of the pins starting with the enable pin.

   Double click on the left component, and click on the Model tab. You will see this model is active-low. This means pulling this pin low will make this part an Output, while providing a voltage source greater than or equal to 1 V will make it an Input. An Active-High model would be the inverse.

   To make the left IO an Output and the Right IO an Input, make the connections as follows. The DC source can be found in the Basic Components palette.



5. Make the rest of the connections as follows

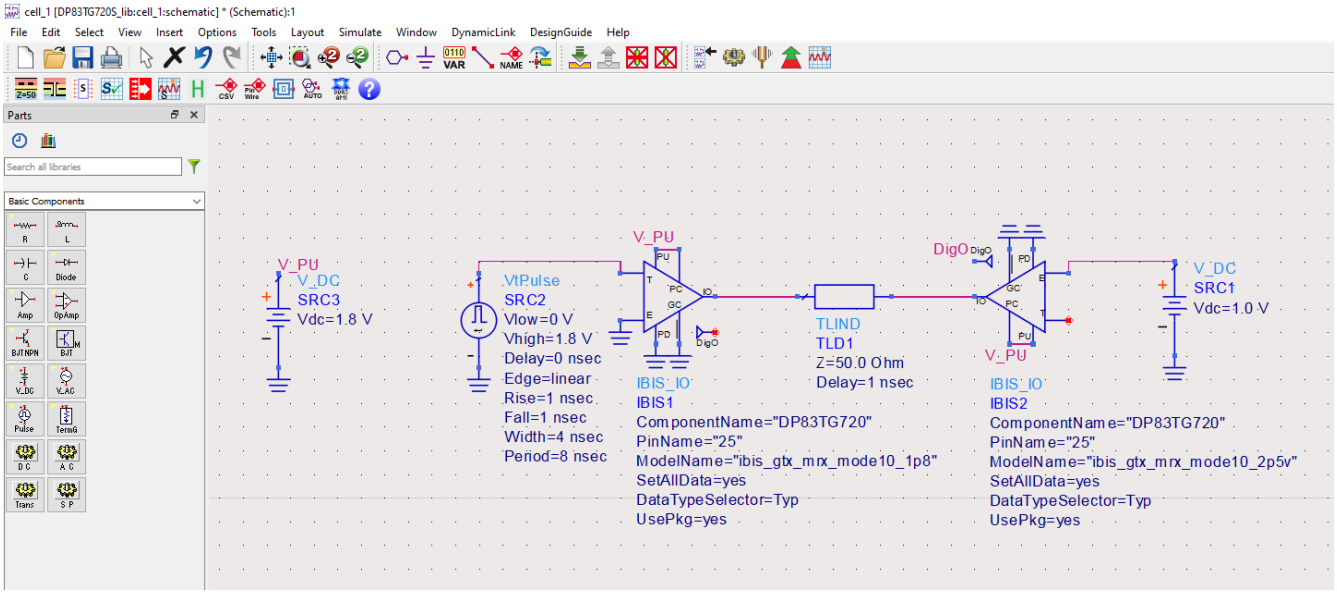
   Trigger Pin – For the Output component, this is the input to the buffer. Place a Pulse source from the Source-Time Domain palette, and configure it to [0,1.8] V and 125 Mhz. For the Input component, this pin is unused.

   IO – Connecting these two pins together will form the channel. In between, add a transmission line of your choosing. Ideal T-Lines are found in the Tlines-Ideal Palette.

   PU(Pullup), PC (Power clamp) – Connect these to the desired logic level of operation.

   PD (Pulldown), GC (Ground clamp) - Connect to ground.

   DigO – Digital output pin for the input device. Insert a pin name here to monitor this later.



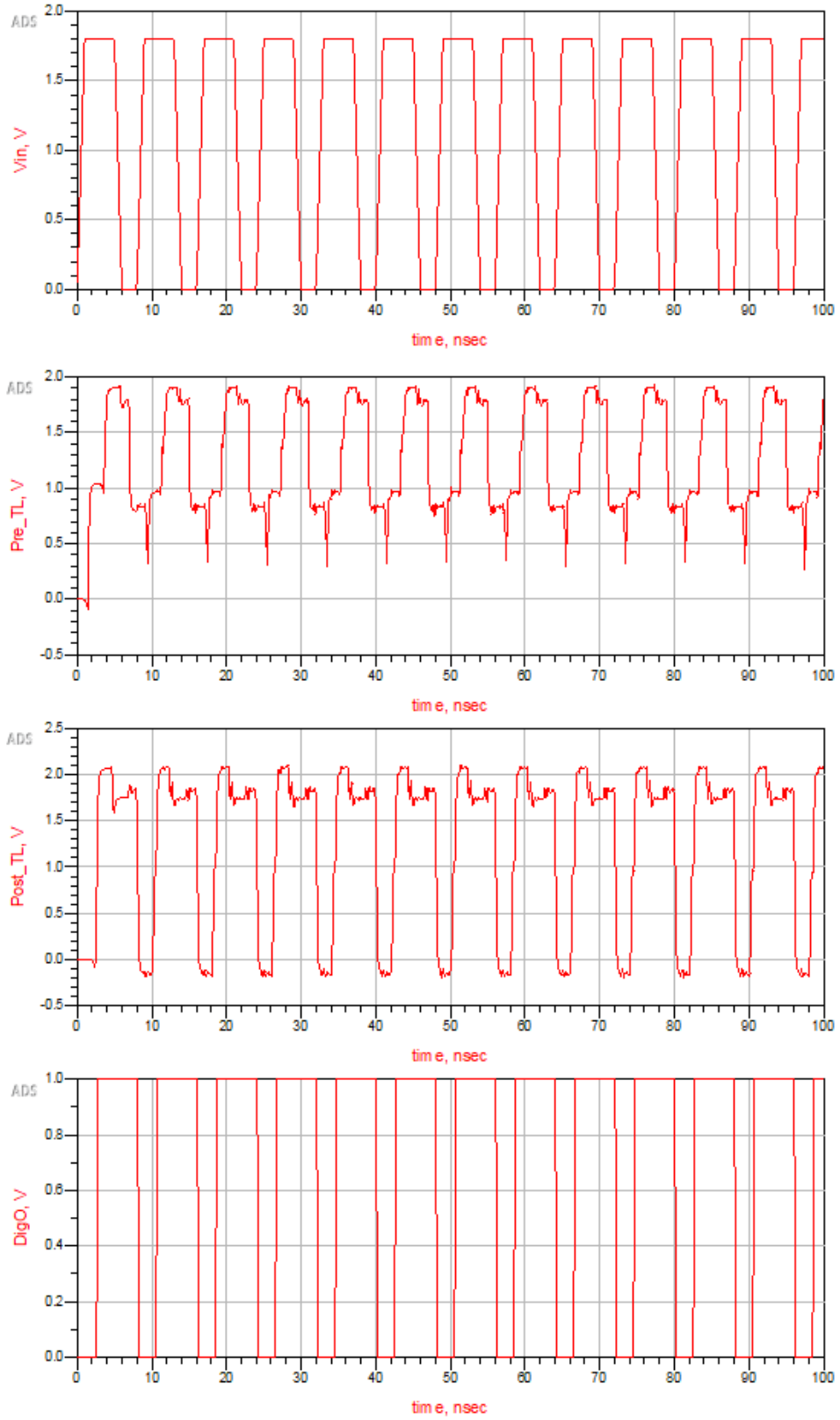
6. Now that the necessary connections are made, double click on the left IBIS component, and navigate to the Pin tab. Here, select the pin and available models. Select the RX_CLK pin and use the default Model. Click Apply.

   Do the same on the right IBIS component, but select the TX_CLK pin.

3.1.2 Simulation

1. Place a transient simulation controller from the Simulation-Transient Palette. Configure it to last 100 nsec with 100 psec step size.
2. Add names to the nets which will be monitored in the simulation. Click the gear icon to start the simulation.

3. Place rectangular charts for each of the signals, or place multiple signals on one chart.

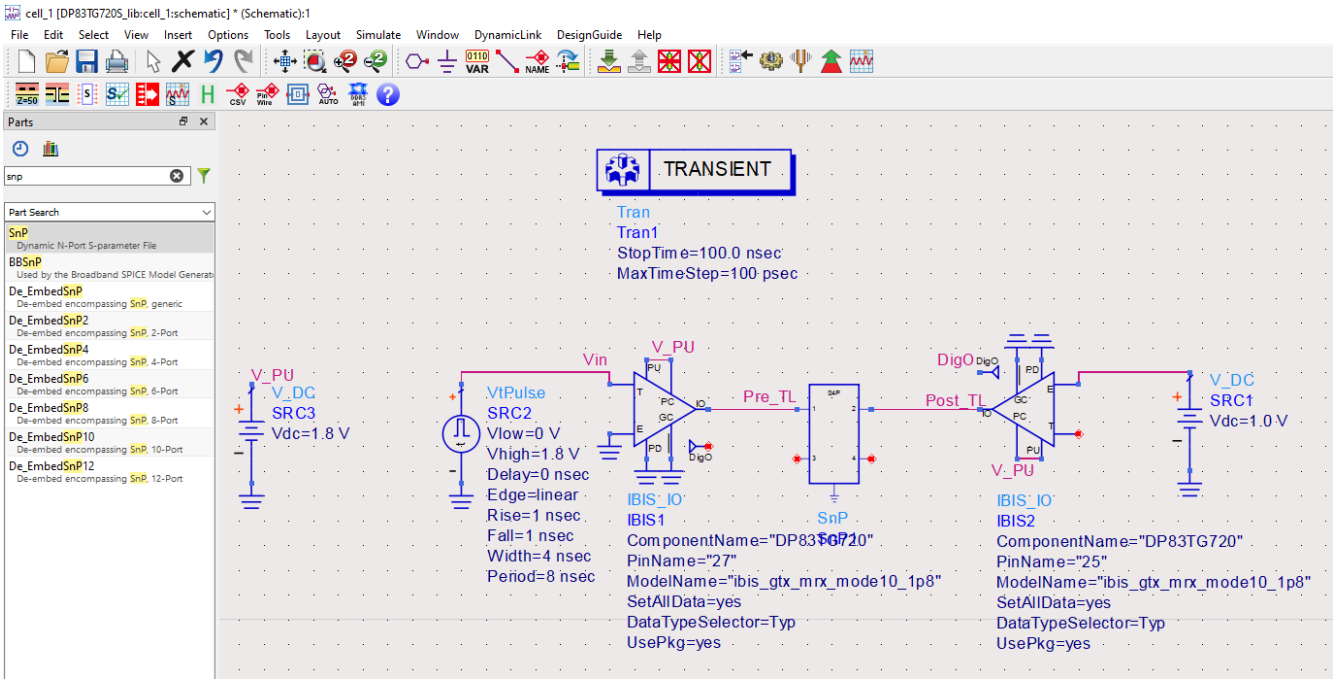


3.1.3 Further Configuration

Further configuration options include:

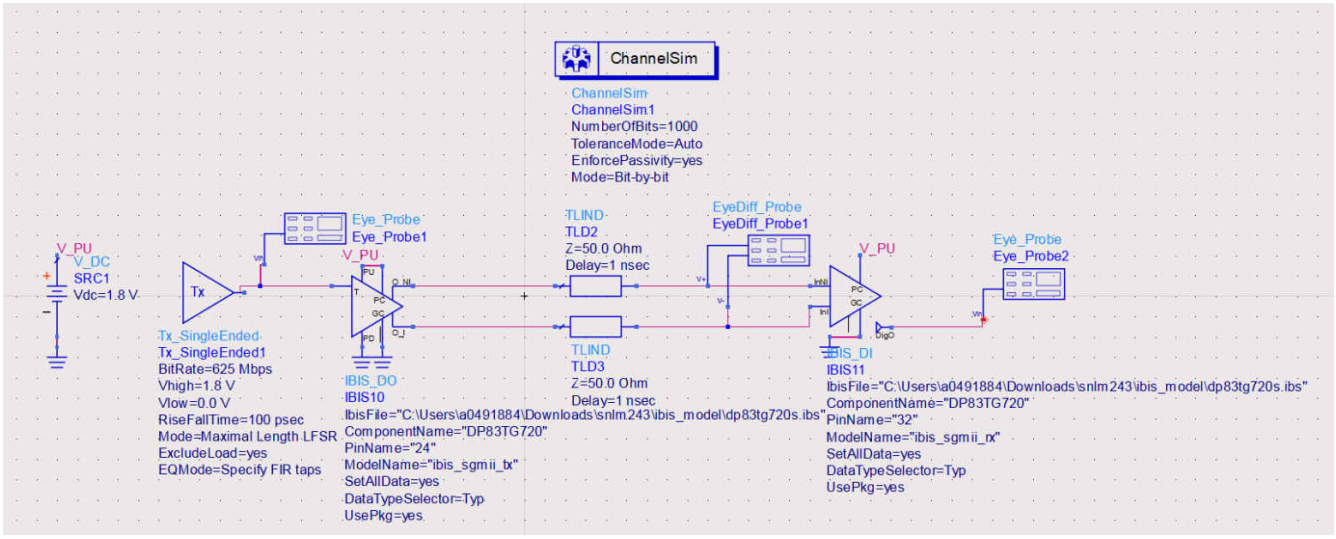
1. Change IC model to Fast/Slow
2. Use package or not.
3. Change the Model selector to a different pin or voltage level. When you increase the model logic level here, increase the Pullup value to the same.
4. Change V_IN. For the RX_D pins, use a PRBS source, found in the Sources-Time Domain palette.

To replace the transmission line with custom S-Parameter models, search for the SnP component in the search bar and connect it in place of the ideal transmission line.

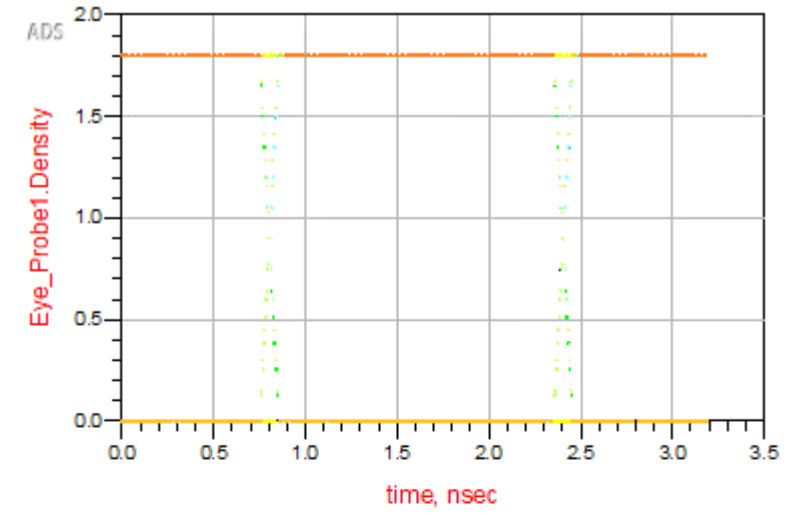


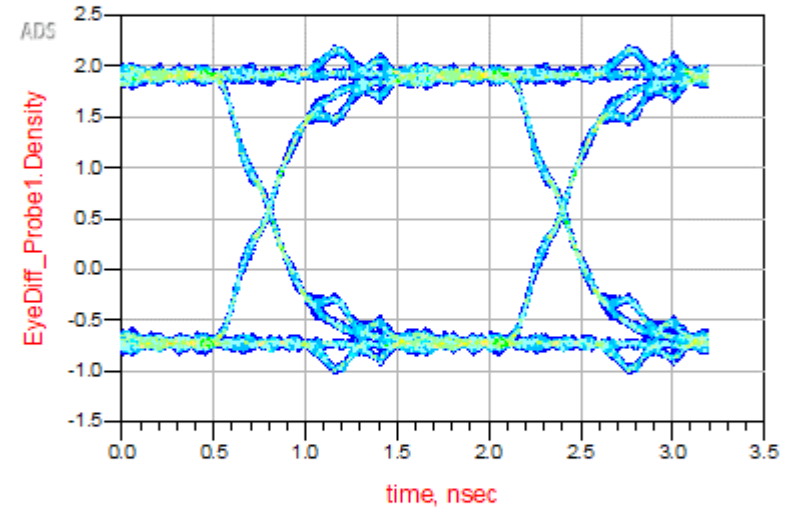
3.2 SGMII Channel Simulation with Eye Diagram

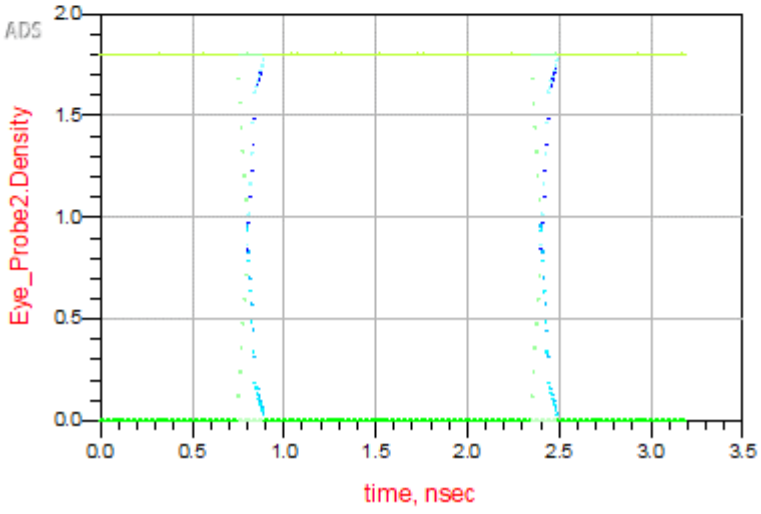
1. Place an IBIS_DI and IBIS_DO component and select the dp83tg720s.ibs files for each. Select pin 23 or 24 for the output and 31 or 32 for the input. It will not matter since the pins are designated as a differential pair.
2. Recreate the rest of the setup as shown below, and simulate.



3. Create rectangular plots and add each eye density plot as shown.







4. Add a list block and select eye_probe1.summary, eyediff_probe1.summary, etc. to see a list of the eye heights and widths.

measurement	Eye_Probe1.Summary	EyeDiff_Probe1.Summary	Eye_Probe2.Summary
Level1	1.800	1.899	1.800
Level0	0.000	-0.715	0.000
Height	1.800	2.283	1.800
Width	1.592E-9	1.592E-9	0.000

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