User's Guide

DS160PT801X16EVM Riser Card Evaluation Module

ABSTRACT

The DS160PT801X16EVM is a 16-lane PCIe riser card board intended to be used for evaluation of the Texas Instruments DS160PT801 PCIe Gen4 retimer. The EVM uses the 1x16 Card Electromechanical (CEM) connector to enable quick system testing in a standard x16 socket and a standard PCIe endpoint. The evaluation board may be used with the SigCon Architect software program to provide register control and status information from the DS160PT801 devices. Contact a local Texas Instruments representative to obtain the SigCon Architect.

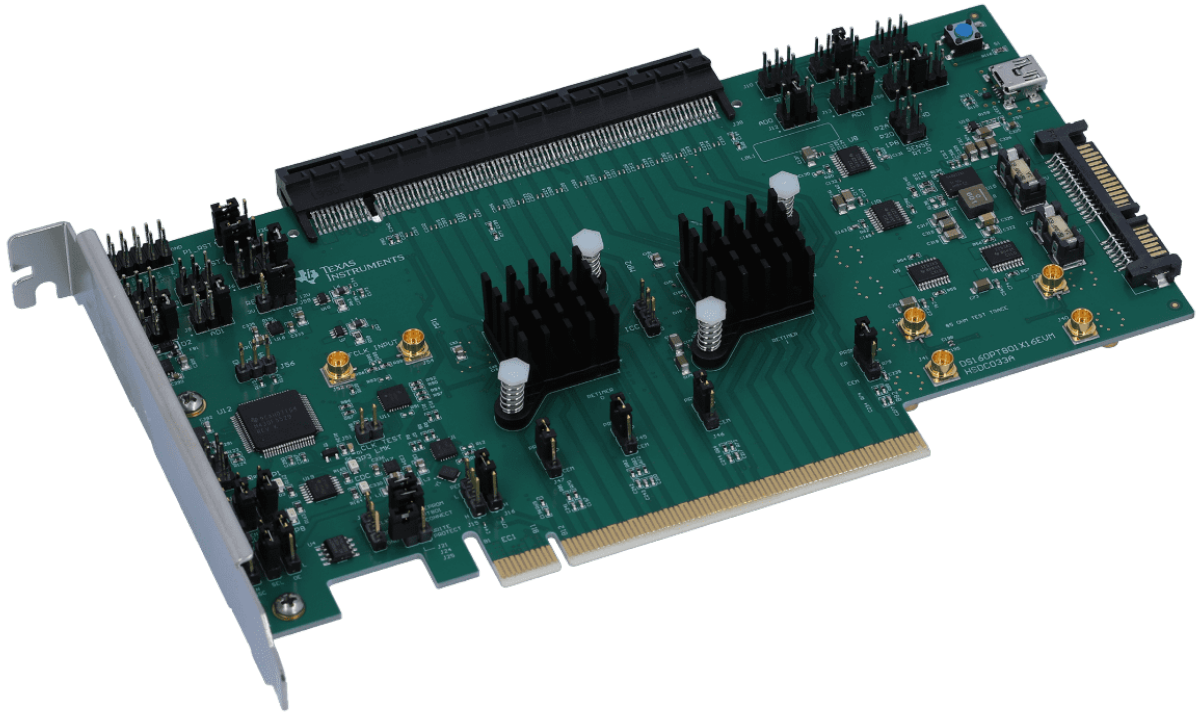


Figure 1-1. DS160PT801 EVM

Table of Contents

List of Figures

List of Tables

Trademarks

Windows® is a registered trademark of Microsoft Corporation.
All trademarks are the property of their respective owners.

1 EVM Control and Configuration Information

The DS160PT801X16 EVM uses an AT24C16 EEPROM to store retimer configuration settings. This EEPROM is pre-loaded with an EEPROM image with various settings to enable quick system bring-up for common-clock PCIe topologies.

Custom EEPROM images for compliance or separate reference independent spread (SRIS) clock topologies may be created and written to the EEPROM using the SigCon Architect software or by using the DS160PT801 I2C interface. For additional information on EEPROM programming through the I2C interface of the DS160PT801, please refer to the DS160PT801 EEPROM Programming Guide.[1]

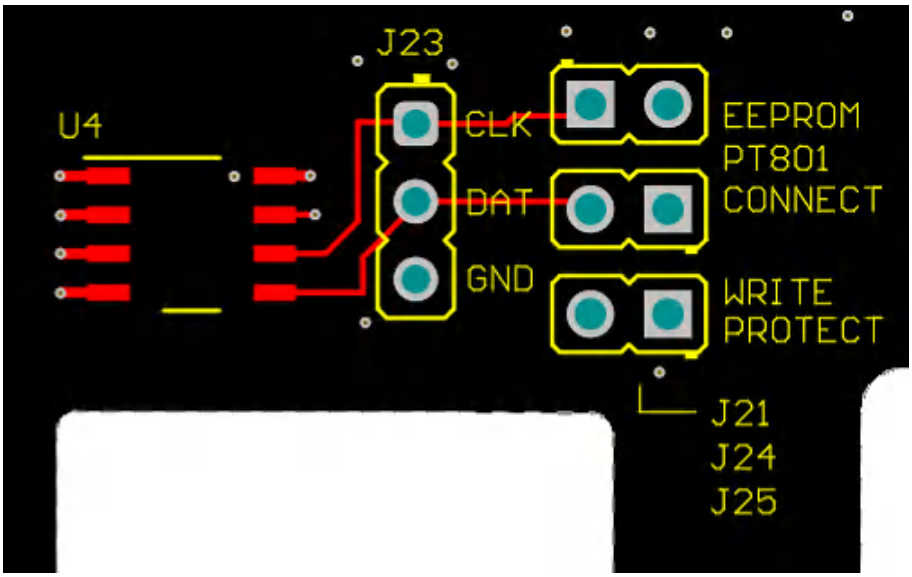


Figure 1-1. DS160PT801X16EVM EEPROM Control and Connection

The EE-PT801 connect headers (J21 and J24) allow for quick connection or disconnection of the EEPROM serial interface. Additional test access points are provided at header J23 to allow the user to monitor EEPROM activity. The J25 header may be used to Write Protect the EEPROM and prevent any changes to the current EEPROM image. When the EEPROM is disconnected, the retimer will completely rely on the pin-strap settings for configuration, which may be modified using the shunt jumpers included with the EVM.

1.1 Retimer Pin Controls

The DS160PT801X16EVM is pre-configured on power-up to use the retimer configuration stored in the onboard EEPROM. These settings may be adjusted by using the pin controls through the onboard headers and jumpers. There are 3 types of headers on the EVM for pin-controls: 2-level, 4-level, and 5-level headers. This section highlights the pin controls and how to adjust them. Additional information about pin settings is provided in the DS160PT801 data sheet.

Jumper options for 2-Level, 3-pin headers are as follows:

- No jumper on header pins – Input floating
- Shunt jumper at pins 1-2 – Input to 1.8 V or 3.3V
- Shunt jumper at pins 2-3 – Input to GND

Jumper options for 4-Level, 6-pin headers are as follows:

- No jumper on header pins – Input floating
- Shunt jumper at pins 1-2 – Inputs to 1.8 V
- Shunt jumper at pins 3-4 – Inputs 10 kΩ to GND
- Shunt jumper at pins 5-6 – Inputs to GND

[1] The DS160PT801 EEPROM Programming Guide is available upon request.

Jumper options for 5-Level, 8-pin headers are as follows:

- No jumper on header pins – Input floating
- Shunt jumper at pins 1-2 – Inputs to 1.8 V
- Shunt jumper at pins 3-4 – Inputs 10 kΩ to 1.8 V
- Shunt jumper at pins 5-6 – Inputs 10 kΩ to GND
- Shunt jumper at pins 7-8 – Inputs to GND

The EVM will have many of the headers pre-populated with jumpers out of the box. The default jumper positions represent the most common positions for the jumpers used during evaluation and testing. Table 1-1 lists the default position for the jumpers.

Table 1-1. Default EVM Jumper Positions

Header Designator	Jumper Position	Description
J1	1-2	Disable CDCE6214 SSC clocking
J2	1-2	Disable CDCE6214 clock output
J4	2-3	Disable CDCE6214 EE_SEL
J6	7-8	Set retimer U2 mode to dual-chip link-width manager
J7	5-6	Set retimer U2 SMBus address to 0x20
J8	5-6	Set retimer U2 SMBus address to 0x20
J11	5-6	Set retimer U3 mode to dual-chip link-width follower
J12	3-4	Set retimer U3 SMBus address to 0x22
J13	5-6	Set retimer U3 SMBus address to 0x22
J16	2-3	Assert CLKREQ#, 1 K pulldown to GND
J18	1-2	Deassert Port 0 PRTRST#, 1 K pullup to 1.8 V
J20	1-2	Deassert Port 1 PRTRST#, 1 K pullup to 1.8 V
J21	1-2	Connect EE_CLK to retimer, enable EEPROM
J24	1-2	Connect EE_DAT to retimer, enable EEPROM
J45	1-2	Endpoint control of PRSNT#2 PCIe signal
J46	1-2	Endpoint control of PRSNT#3 PCIe signal
J47	1-2	Endpoint control of PRSNT#1 PCIe signal
J48	1-2	Endpoint control of PRSNT#4 PCIe signal
J49	2-3	Use clock source from CEM connector for REFCLK
J50	2-3	Disable clock output from LMK00334
J58	3-4	Set voltage regulator to output 1.15 V
J59	1-2	Enable U16 voltage regulator with 12 V supply

1.2 USB-to-SMBus Interface

The DS160PT801X16EVM uses an onboard MSP430 microcontroller to create USB-to-SMBus interface. The USB-to-SMBus interface is intended to be used with Texas Instruments software like SigCon Architect to communicate to the DS160PT801 retimers.

When using the default jumper configuration listed in Table 1-1, the DS160PT801 at location U2 is setup for SMBus address 0x20 (8-bit address). The DS160PT801 at location U3 is setup for SMBus address 0x22. The retimers can also be configured to other SMBus address combinations.

Figure 1-2 shows the locations of the SMBus address headers used to modify the default SMBus addresses for the retimers. For more information on valid SMBus addresses, please refer to the DS160PT801 data sheet.

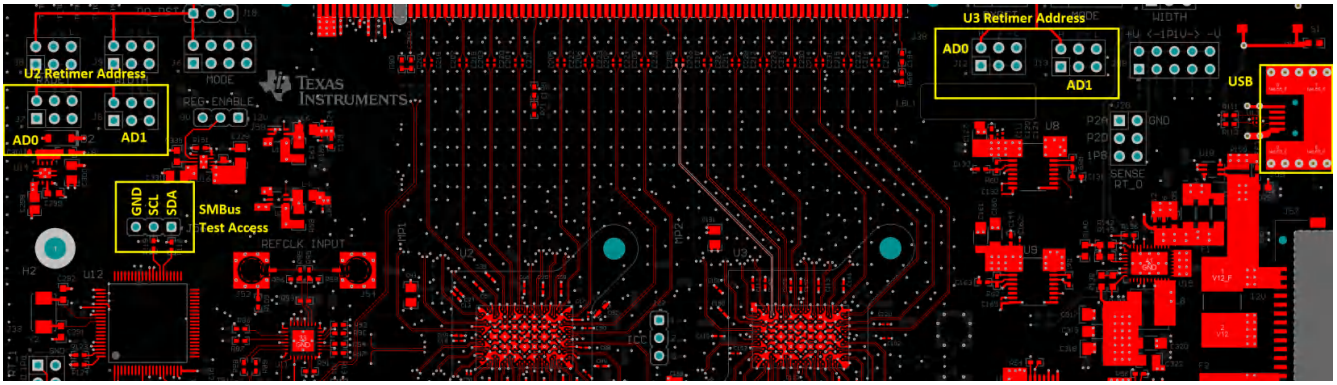


Figure 1-2. DS160PT801X16EVM SMBus Interface Connections

To access the DS160PT801 devices through this interface, power must be applied through the SATA or *Gold Finger* connectors.

1.3 PCIe PRSNT# Signal Control and Configuration

The riser card allows users to alter the hot-plug presence detect signal (PRSNT#) returned to the PCIe host sytem. This is done by using the headers shown in Figure 1-3. By modifying the jumpers it is possible to have the PRSNT# signal represent a x1, x4, x8, or x16 mechanical link width. When using the default jumper configuration listed in Table 1-1, the DS160PT801 riser card allows the PRSNT# lines to be dynamically determined by the connected endpoint, which is useful for hot-plug detection.

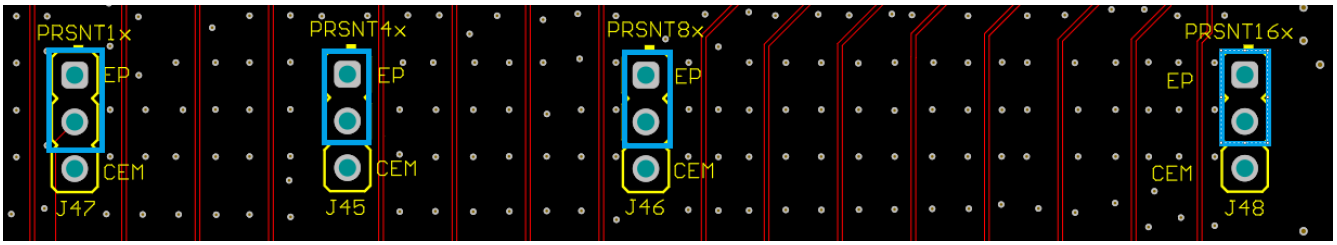


Figure 1-3. DS160PT801X16EVM PCIe PRSNT# Controls

Removing the four shunt jumpers on J45–J48 and placing a single shunt across the lower two pins in one of the connectors allows the riser card to override PRSNT#. This is useful if a certain width is desirable. For example, by inserting a shunt jumper in position 2-3 on header J45 will force the PRSNT# status to represent a 1x4 mechanical link width.

1.4 PCIe Reference Clock Control and Configuration

The riser card was designed to accommodate common and independent 100-MHz reference clock architectures. The default configuration is for a common clock distribution. The incoming system clock is buffered with a clock fanout device (LMK00334) and sent to each retimer and to the endpoint. The following graphics highlight EVM and BOM changes which are available to modify the PCIe clock configuration.

1. Set J49 = L for CEM Clock distribution (Common Clock – default setting)
2. Set J49 = H for CDCI6214 Clock distribution (Independent Clock)

Regardless of the clock configuration, there are SMP test points available for clock measurement or triggering. Refer to Figure 1-4 and Figure 1-5 for more details.

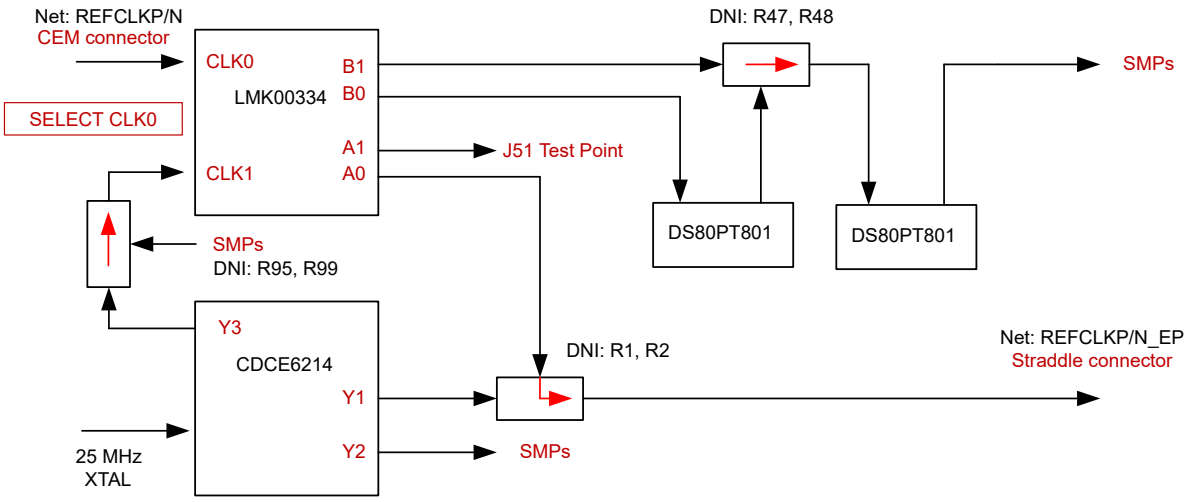


Figure 1-4. Common Clock Topology Example

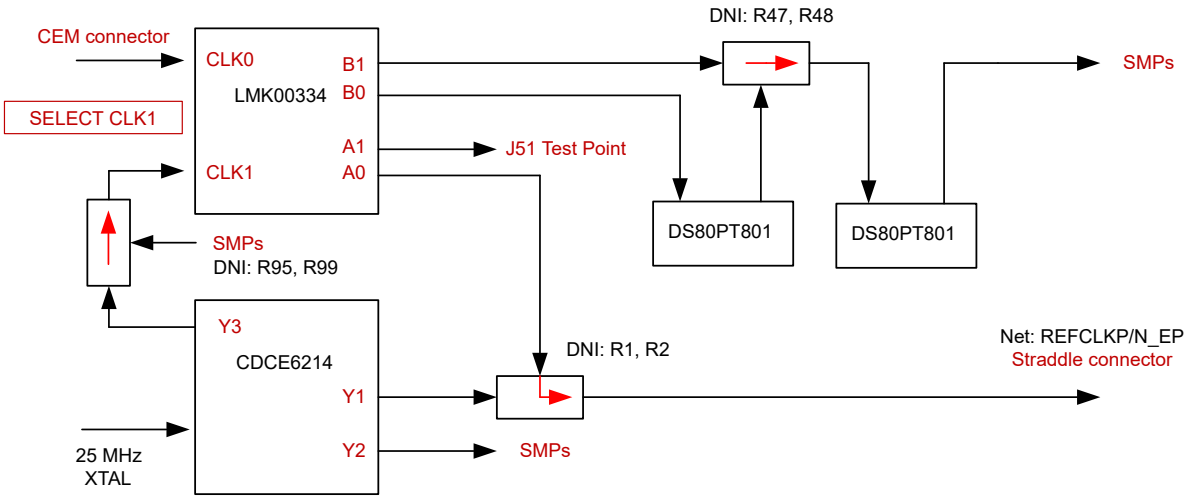


Figure 1-5. Independent Clock Topology Example

2 EVM Power

Onboard regulation is used to step down the input 12-V and 3.3-V supplies to power both DS160PT801 retimers and other devices on the riser card EVM. There are LEDs to indicate *power good* for the 1.17-V, 1.8-V and 3.3-V power supplies. The 1.17-V power supply level can be adjusted in 50-mV increments between 1.0 V and 1.2 V. Connector J58 is used to make these adjustments. By default, the jumper for J58 is set to the 3-4 position, which is 1.15 V. The center of the header is a 1.1 V supply level, increasing supply levels to the left and decreasing supply levels to the right. The EVM must be powered off completely 15 seconds to change voltage level.

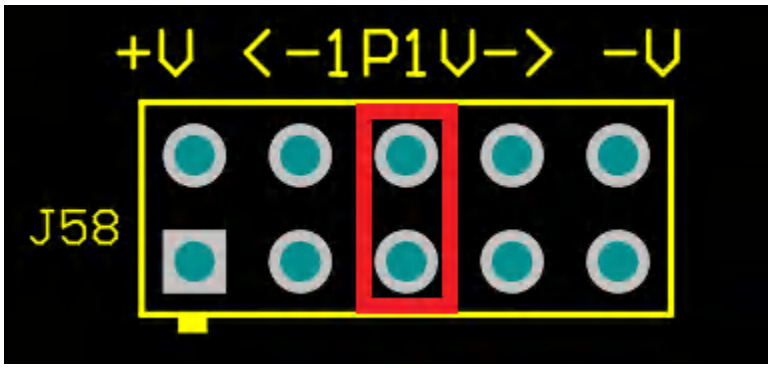


Figure 2-1. 1.17-V Power Supply Pin Controls

To facilitate debug and prototype system bring up, the DS160PT801X16 EVM can be powered in two different ways. One method is through the Gold Finger connector. The other is with the SATA connector at the right side of the riser card design. The SATA connector can be used to power the EVM separately from the system power supply. This can be used to help diagnose power supply issues and allow for pre-configuration of the DS160PT801 through the SMBus interface before system power-up.

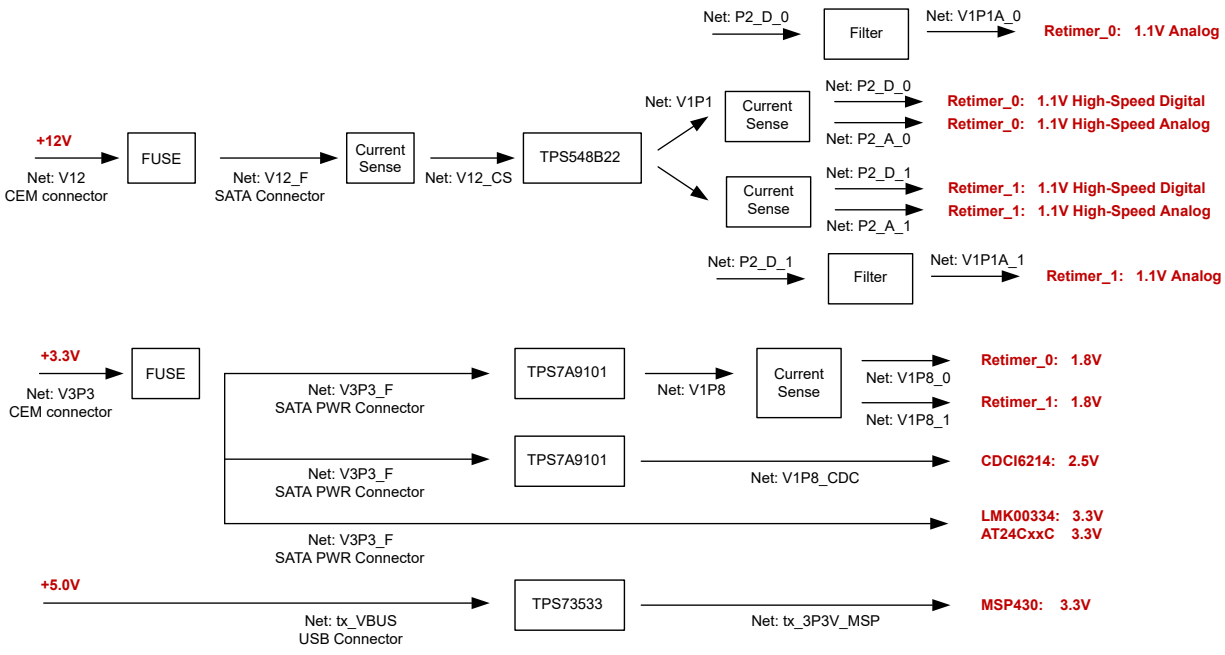


Figure 2-2. DS160PT801X16EVM Power Network

2.1 EVM Current Sensing

Onboard current sense devices are incorporated into the EVM design and layout to monitor voltage regulator power delivery and assist with thermal analysis. The voltages measured at this connector can be used to calculate the efficiency of the voltage regulator and the current delivered to each DS160PT801 device.

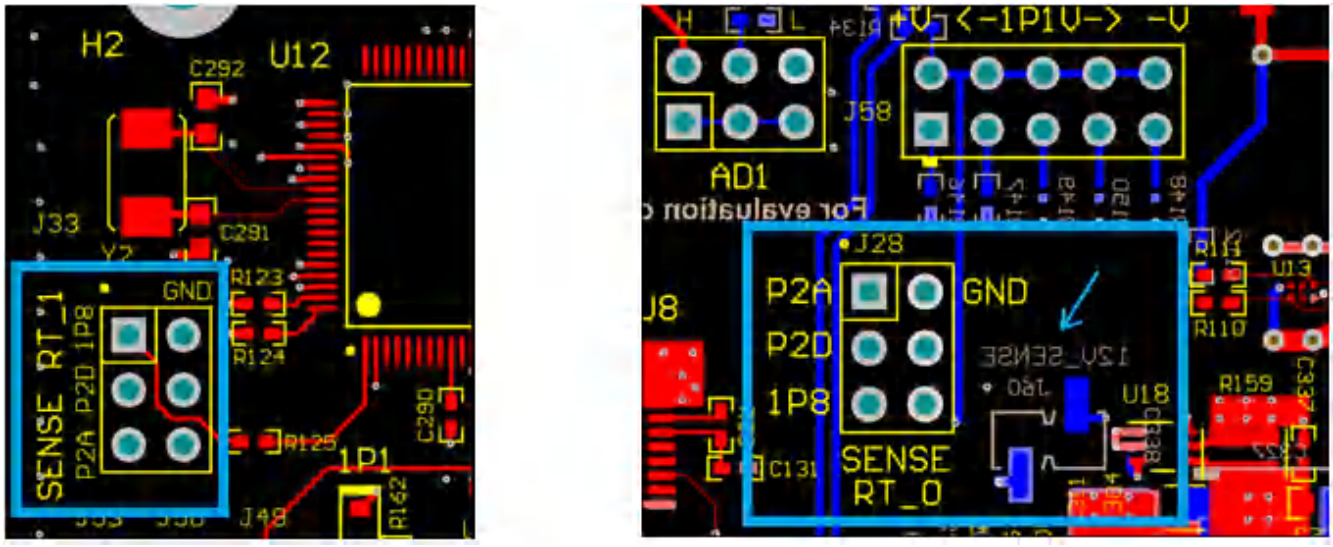


Figure 2-3. DS160PT801X16EVM Current Sense Measurement Locations

Equation 1 through Equation 4 describe the relationship between the voltage measured from the current sense devices and the current delivered.

12V_SENSE (J60): Input 12-V supply to TPS548B22 VR

$$V_{MEASURED} / 20 = \text{Input VR Current (Amps)} \quad (1)$$

1P8: 1.8-V supply to retimer 0 (U2).

$$V_{MEASURED} / 20 = \text{Retimer, 1.8 V current consumption in Amps} \quad (2)$$

P2A: 1.17-V supply to retimer (PWR_2A)

$$V_{MEASURED} / 20 = \text{Retimer, 1.17 V current consumption (PWR\_2A) in Amps.} \quad (3)$$

P2D: 1.17-V supply to retimer (PWR_2B). Also includes PWR_2C.

$$V_{MEASURED} / 0.2 = \text{Retimer, 1.17 V current consumption (PWR\_2B + PWR\_2C) in Amps.} \quad (4)$$

Notes:

1. Retimer 0 (U2) sense connections are in J28
2. Retimer 1 (U3) sense connections are in J33
3. 12V_SENSE (J60) is on the *bottom layer*

3 SigCon Architect GUI

The SigCon Architect GUI is designed to be used in conjunction with the DS160PT801X16EVM. By communicating to the two onboard retimers through the included USB cable, the status of the retimers and PCIe link can be assessed using a graphical interface.

The SigCon Architect framework is also designed to work with other Texas Instruments products. For this reason, the installation of the software is split into two parts: The SigCon Architect Framework and the product profile plug-in. Adding the DS160PT801 product profile to the SigCon Architect framework will enable its evaluation features. At the time of this document's release, the latest version of the SigCon Architect framework is version 3.1.0.1, and the latest DS160PT801 profile is version 1.4.0.1.

Together this software enables users to evaluate the DS160PT801 PCIe Gen4 retimer in a system environment. SigCon Architect is available by request. Please contact a local TI sales representative for more information.

3.1 Setup and Installation

The SigCon Architect framework and DS160PT801 product profile are designed to work with a Windows® operating system. The installation of the software takes place in two parts. First the installation of the SigCon Architect v3 framework. After installing the framework, the DS160PT801 product profile may be added.

The step-by-step setup instructions below show be followed to complete the installation of the software and prepare the DS160PT801X16EVM for evaluation using SigCon Architect.

1. Download and install SigCon Architect Version 3.
2. Download and install the DS160PT801 profile.
3. Connect the included micro-USB cable to the EVM and to the Windows PC.
4. Connect the EVM to the host system by plugging the EVM into a PCIe x16 CEM slot.
5. Install a PCIe end point card, such as a network interface card or GPU, into the opposing top mount straddle connector.
6. Provide power to the EVM by turning on the host system.
7. Start the SigCon Architect application to begin evaluation.
8. Confirm that the DS160PT801 Configuration page is selected in the navigation panel on the left side of the window.

The EVM and software should now be ready for evaluation. The DS160PT801 SigCon Architect profile contains 6 pages that group similar functions of the retimer together. These pages are: configuration, low-level, EEPROM, high-level, diagnostic, and eye monitor. The navigation panel on the left side of the window provides navigation to all pages; however, pages will be inaccessible until an SMBus connection is established by using the Configuration page.

3.2 Configuration Page

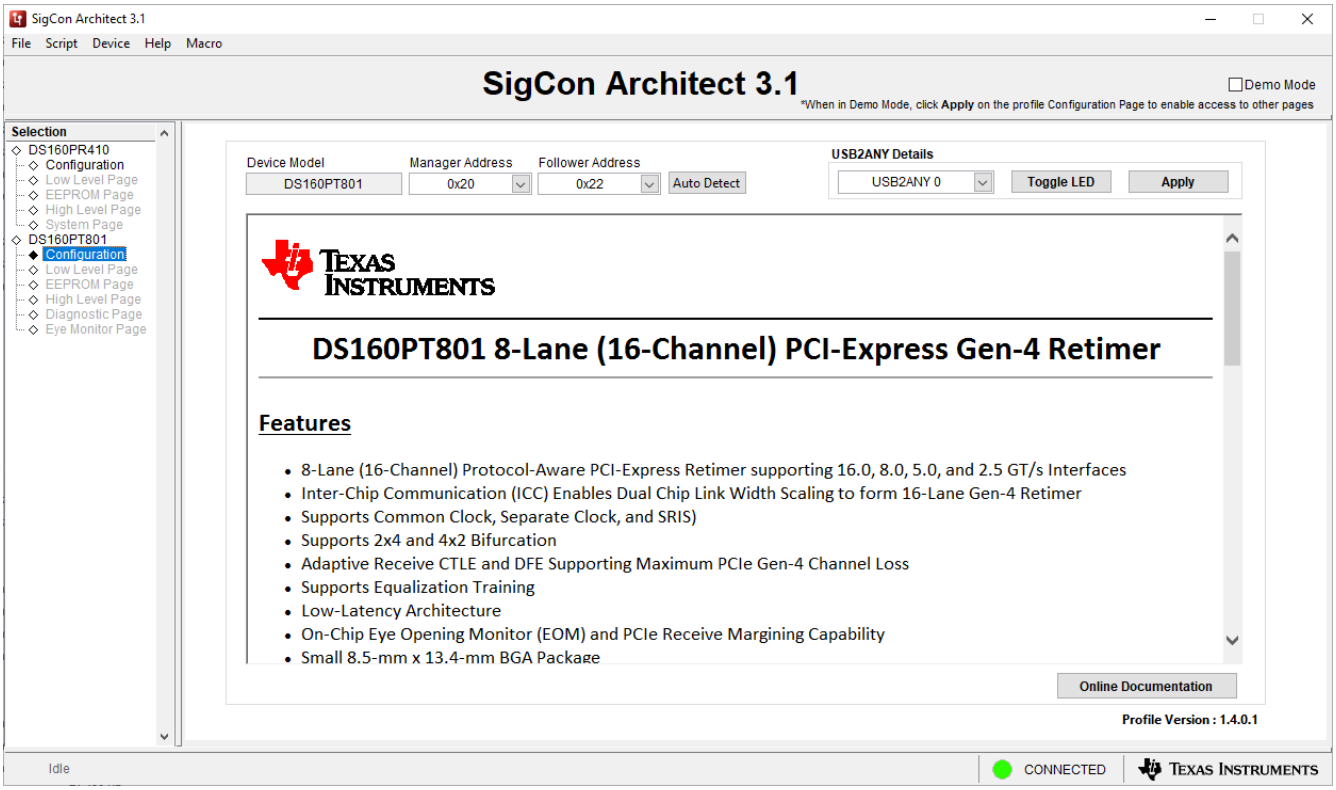


Figure 3-1. Configuration Page Screenshot

The Configuration page of the DS160PT801 profile in the SigCon Architect GUI is the only page enabled after starting the software. This page is intended to be used to configure a connection to the EVM's onboard retimers through the USB2ANY interface for full access to the retimer functions. To establish a connection, the SMBus address for the link-width manager and link-width follower should be specified in the provided dropdowns. After the valid SMBus addresses are specified, the *Apply* button is used to establish the connection. The following are descriptions of the various input fields of the Configuration page:

- **Manager Address Dropdown** specifies the SMBus address of the link-width manager.
- **Follower Address Dropdown** specifies the SMBus address of the link-follower.
- **Toggle LED Button** can toggle an onboard LED and can be used to confirm a successful connection.
- **Apply Button** attempts to establish an SMBus connection to the onboard retimers. If a connection is successfully established, the other pages of the DS160PT801 GUI will be enabled.
- **Online Documentation Button** connects to online documentation for the DS160PT801 on ti.com.
- **Demo Mode Checkbox** may be used to enable GUI demo mode. In this mode, all features of the GUI are enabled to demonstrate the features of the GUI without an active retimer connection. This may be used to create EEPROM images, view the register map, or evaluate other portions of the DS160PT801 GUI.

3.3 Low-Level Page

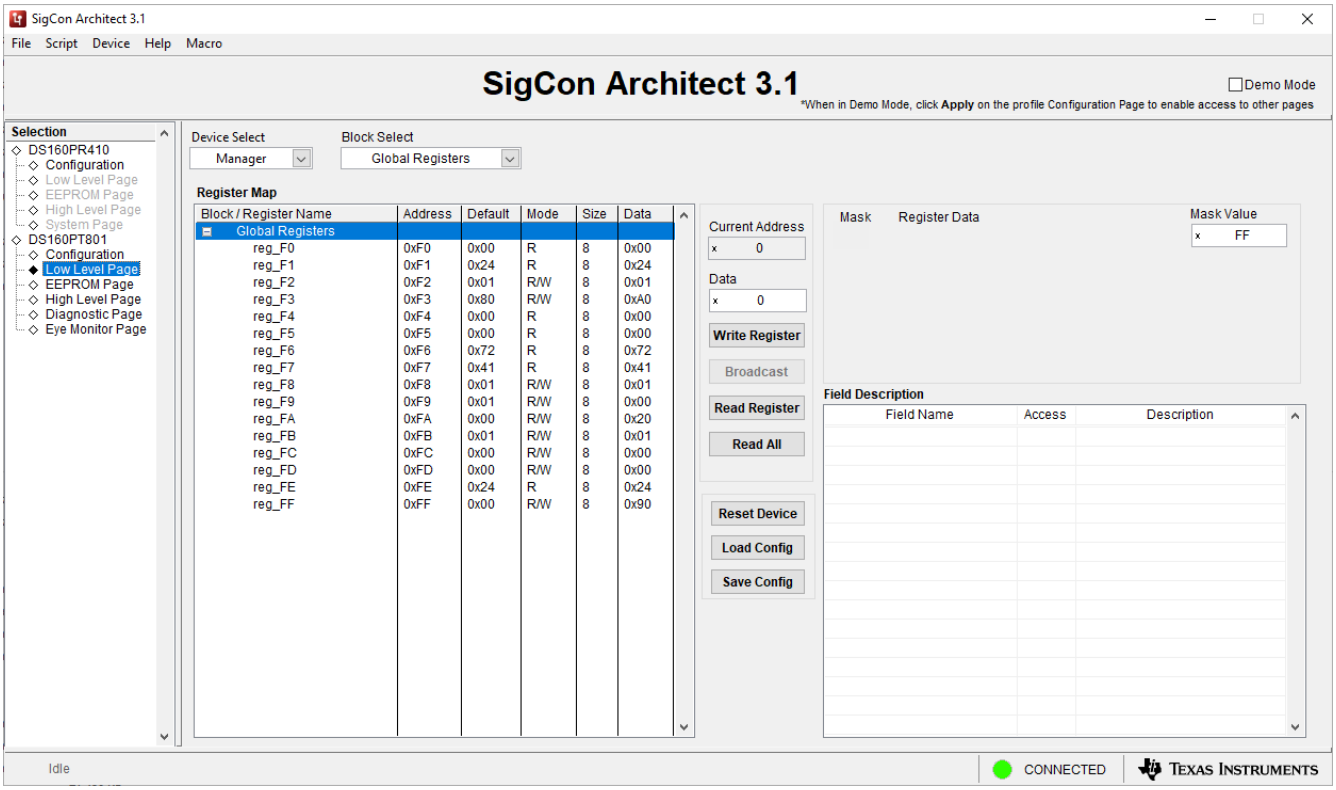


Figure 3-2. Low-Level Page Screenshot

The Low-Level page of the GUI is used for basic register access to the register map of the DS160PT801 retimer by providing SMBus read and write functions. The ability to save a specific retimer configuration for use later is also provided and can be used performing system evaluation. The description of the input fields of the Low-Level page are as follows.

- **Device Select Dropdown** allows a user to change the active register map from either the link-width manager or link-width follower SMBus address.
- **Block Select Dropdown** allows a user to change the active register block between Global, Shared, Channel, or PLL registers.
- **Current Address Field** displays the currently selected register address.
- **Data Field** displays the data currently stored at the selected register address.
- **Mask Value Field** displays the mask value that will be used for write operations at this register. Only the bits that are set to a "1" in this field will be written to.
- **Write Register Button** issues an SMBus write of the data listed in the data field at the current address using the bit mask indicated in the Mask Value field.
- **Broadcast Button** becomes active when one of the channel register blocks are selected. Clicking this button performs a write operation similar to the *Write Register* button, but it will broadcast the write to all channels in the currently selected device.
- **Read Register Button** issues an SMBus read of the data listed in the current address field.
- **Read All Button** issues a SMBus read of all registers for the currently selected register block.
- **Reset Device Button** resets all register values back to their default values. This will cause an active PCIe link to fail.
- **Load Config Button** can be used to load a previously saved set of SMBus register values.
- **Save Config Button** saves a file that stores the current values for all SBMus registers. This file can later be loaded using the *Load Config* button.

3.4 EEPROM Page

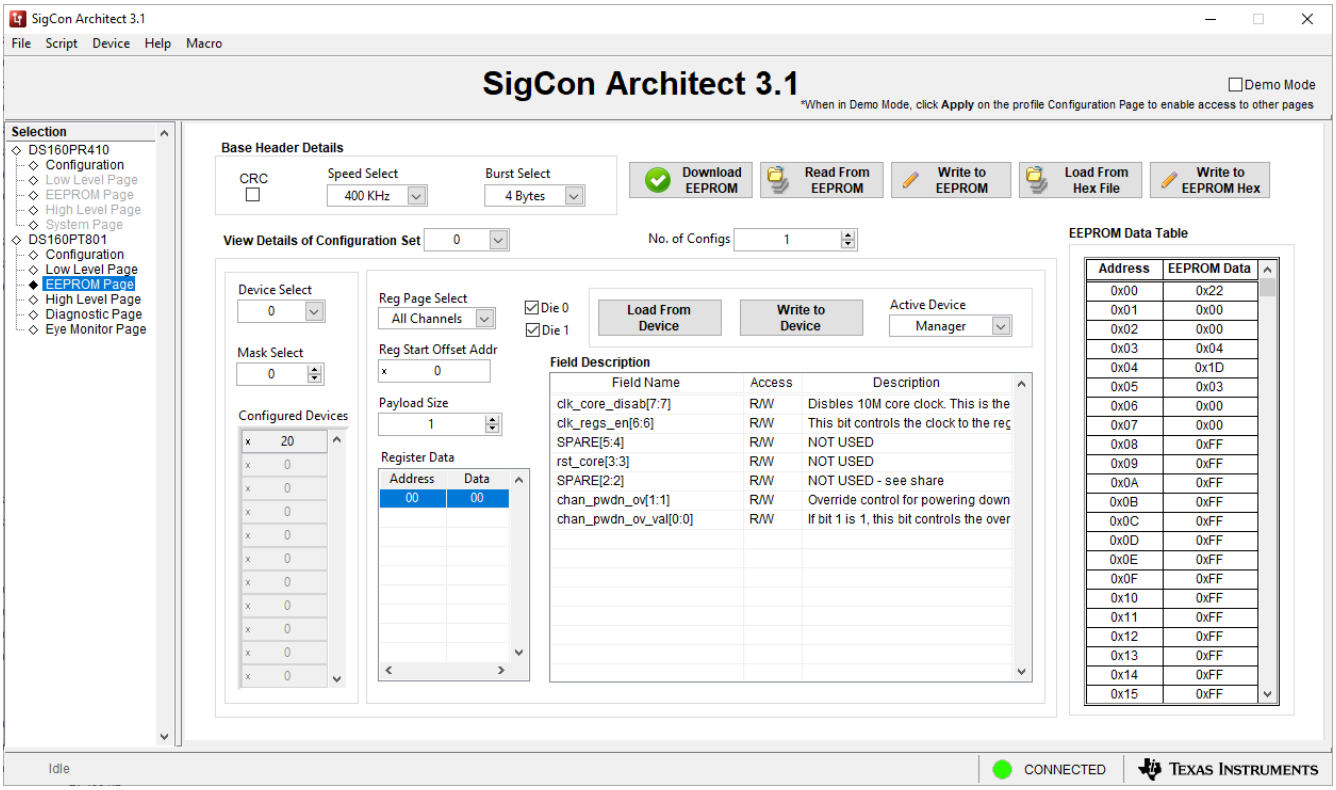


Figure 3-3. EEPROM Page Screenshot

The EEPROM page provides access to the EEPROM reading and writing functions of the retimer. It also allows a user to load or save a pre-configured EEPROM image stored in the .hex file format. For more details about EEPROM image formatting, please refer to the DS160PT801 EEPROM Programming Guide.[2]

- **CRC Check Box** sets the CRC bit to "1" in the EEPROM base header. If enabled, CRC value is computed for all configuration sets and CRC checking is performed.
- **Speed Select Dropdown** modifies the write speed field in the EEPROM base header for the current EEPROM image. This effects how quickly the EEPROM is loaded after power-up.
- **Burst Select Dropdown** modifies the EEPROM base header to change the amount of consecutive bytes per read when loading an EEPROM image.
- **Download EEPROM Button** initiates a download of the currently loaded image on the EEPROM to the retimer.
- **Read From EEPROM Button** reads the currently loaded EEPROM image and updates the GUI with its contents.
- **Write to EEPROM Button** writes the EEPROM configuration that is currently active in the GUI to the EEPROM device.
- **Load From Hex File Button** opens a file explorer window that allows the user to load a .hex file EEPROM image.
- **Write to EEPROM Hex Button** saves the currently loaded configuration in the GUI to a .hex file EEPROM image.
- **View Details of Configuration Set Dropdown** selects the current EEPROM Configuration Set that is displayed and can be edited in the GUI.
- **No. of Configs Field** shows the maximum number of configuration sets for the current configuraiton
- **Device Select Dropdown**, combined with the Mask Select dropdown, modifies the SMBus addresses that are effected by the currently displayed configuration set.
- **Mask Select Dropdown**, combined with the Device Select dropdown, modifies the SMBus addresses that are effected by the currently displayed configuration set.

[2] The DS160PT801 EEPROM Programming Guide is available upon request.

- **Configured Devices List** shows SMBus addresses of the retimers that will be effected by the currently displayed configuration set.
- **Reg Page Select Dropdown** modifies the register page for the currently displayed configuration set.
- **Reg Start Offset Addr Dropdown** modifies the starting register offset address for the currently displayed configuration set.
- **Payload Size Dropdown** determines the number of bytes to be written in the currently selected configuration set. The bytes will begin writing at the location specified by the Reg Start Offset Addr Dropdown.
- **Register Data Table** displays the SMBus addresses and corresponding values in the currently selected configuration set.
- **Die 0 Checkbox** enables Die 0 to be written to by the currently selected configuration set.
- **Die 1 Checkbox** enables Die1 to be written to by the currently selected configuration set.
- **Load From Device Button** updates the current configuration set's data with the register settings of the active device.
- **Write to Device Button** updates the register settings of the active device with the current configuration set's data.
- **Active Device Dropdown** changes the active device for the Load From Device and Write to Device commands.
- **Field Description Table** shows the register map information about the currently selected register.
- **EEPROM Data Table** shows the full raw EEPROM data that will be loaded on the retimer.

3.5 Control Panel

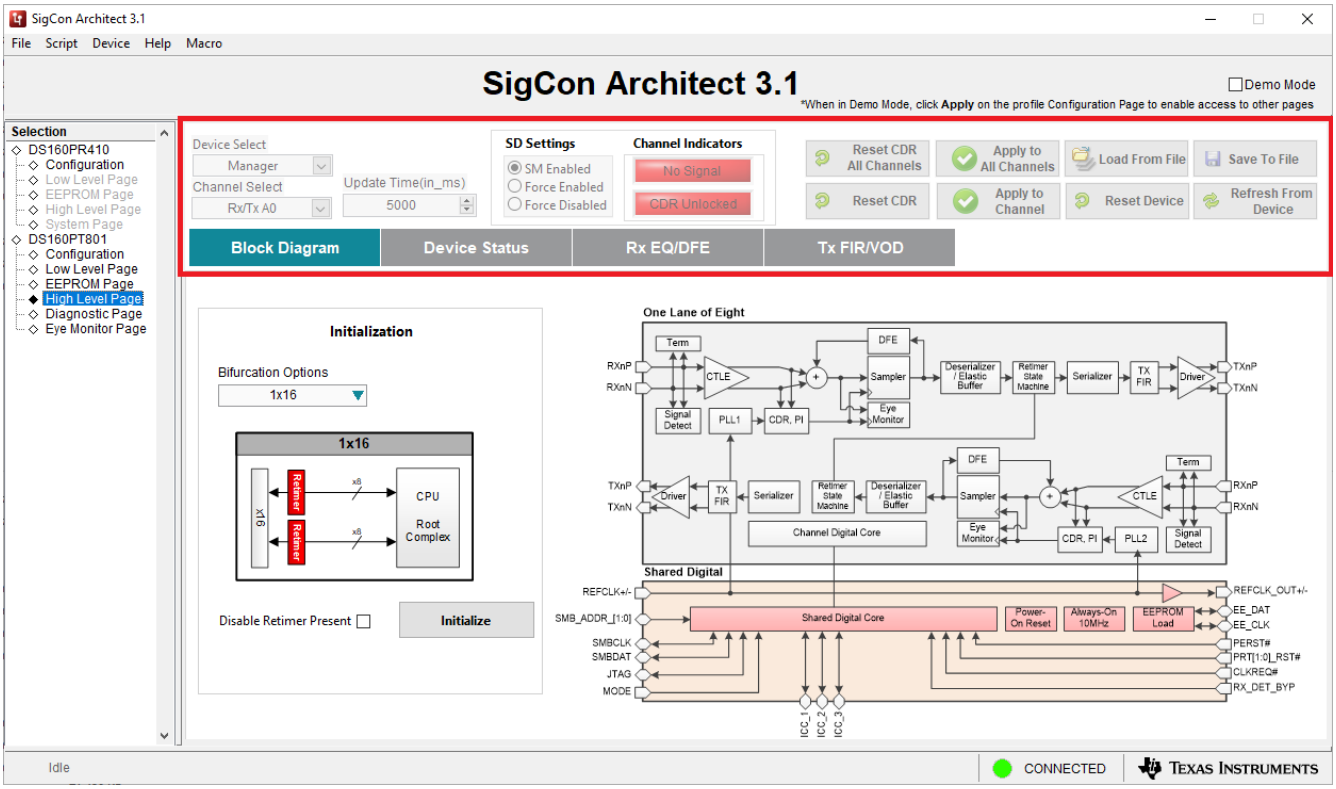


Figure 3-4. Control Panel Screenshot

The retimer control panel is present in the High-Level, Diagnostic, and Eye Monitor pages of the DS160PT801 GUI. Based on the page that a user is currently on, it will enable and disable certain functions. A list of the functions for each of the fields within the control panel is shown below:

- **Device Select Dropdown** selects the active device being configured, either the link-width manager or link-width follower. It is enabled in the High-Level page when modifying the Rx/Tx EQ settings, the Diagnostic page, and Eye Monitor pages.
- **Channel Select Dropdown** selects the active channel being configured. It is enabled in the High-Level page when modifying the Rx/Tx EQ settings, the Diagnostic page, and Eye Monitor pages.

- **Update Time Dropdown** updates the refresh rate for the GUI when the GUI is automatically polling for retimer status information, such as the Device Status section of the High-Level page.
- **SD Settings Radio Buttons** changes the Signal Detect mode of the currently selected channel between State Machine controlled, Force Enabled, and Force Disabled.
- **Channel Indicators** reports if the currently active channel is detecting a signal and if the CDR is locked onto the incoming signal.
- **Reset CDR All Channels Button** reset the CDR for all channels on the currently active device. This will break a PCIe link and should be used for evaluation only.
- **Apply to All Channels Button** applies changes specified in the GUI to all channels on the retimer. It is enabled in the High-Level page when modifying the Rx/Tx EQ settings, the Diagnostic page, and Eye Monitor pages.
- **Load From File Button** allows a user to load a previously saved configuration file.
- **Save to File Button** enables a user to save the current SMBus configuration for the retimer in a configuration file.
- **Reset CDR Button** resets the CDR for the currently selected channel.
- **Apply to Channel Button** applies signal detect settings to the currently selected channel.
- **Reset Device Button** completely resets the retimer to the default register settings. This will disable a PCIe link.
- **Refresh From Device Button** refreshes data in the GUI by downloading the current SMBus configuration of the retimer.

3.6 High-Level Page

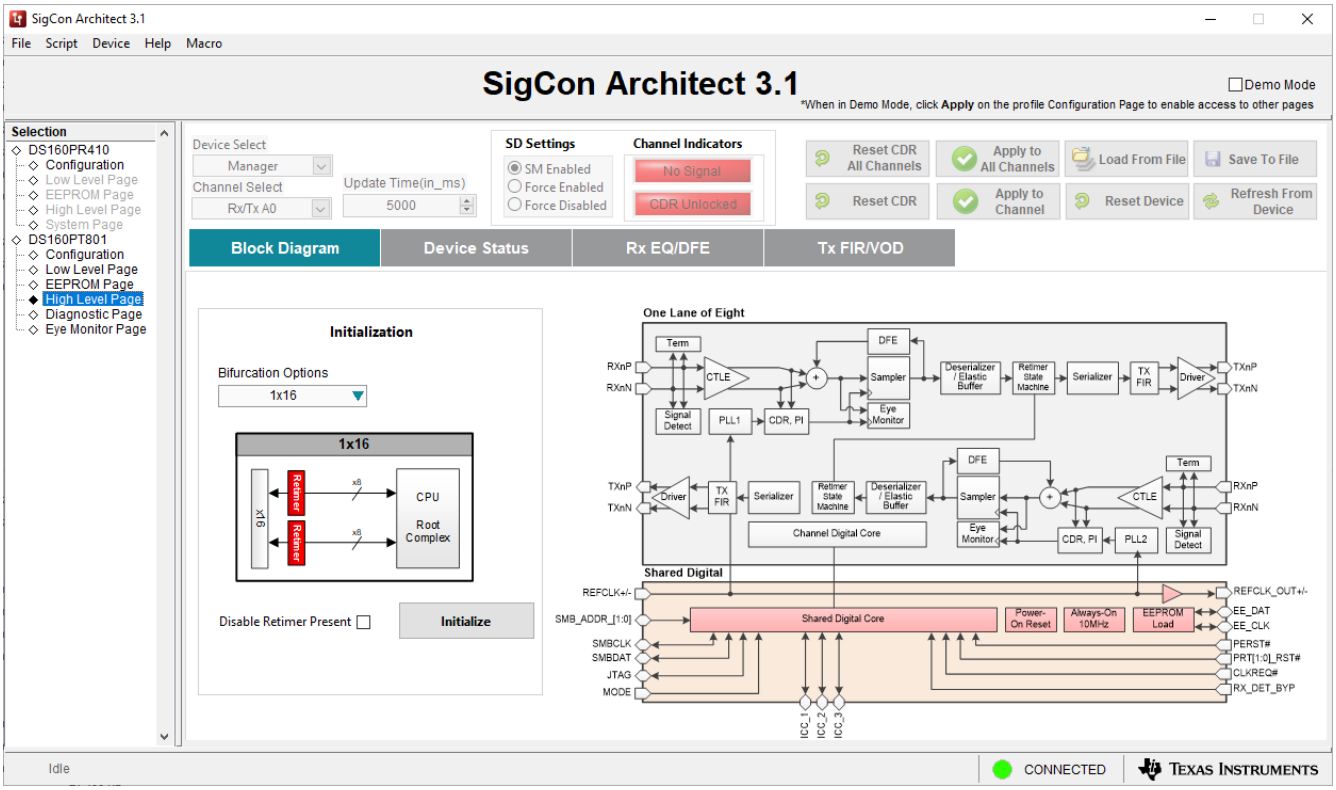
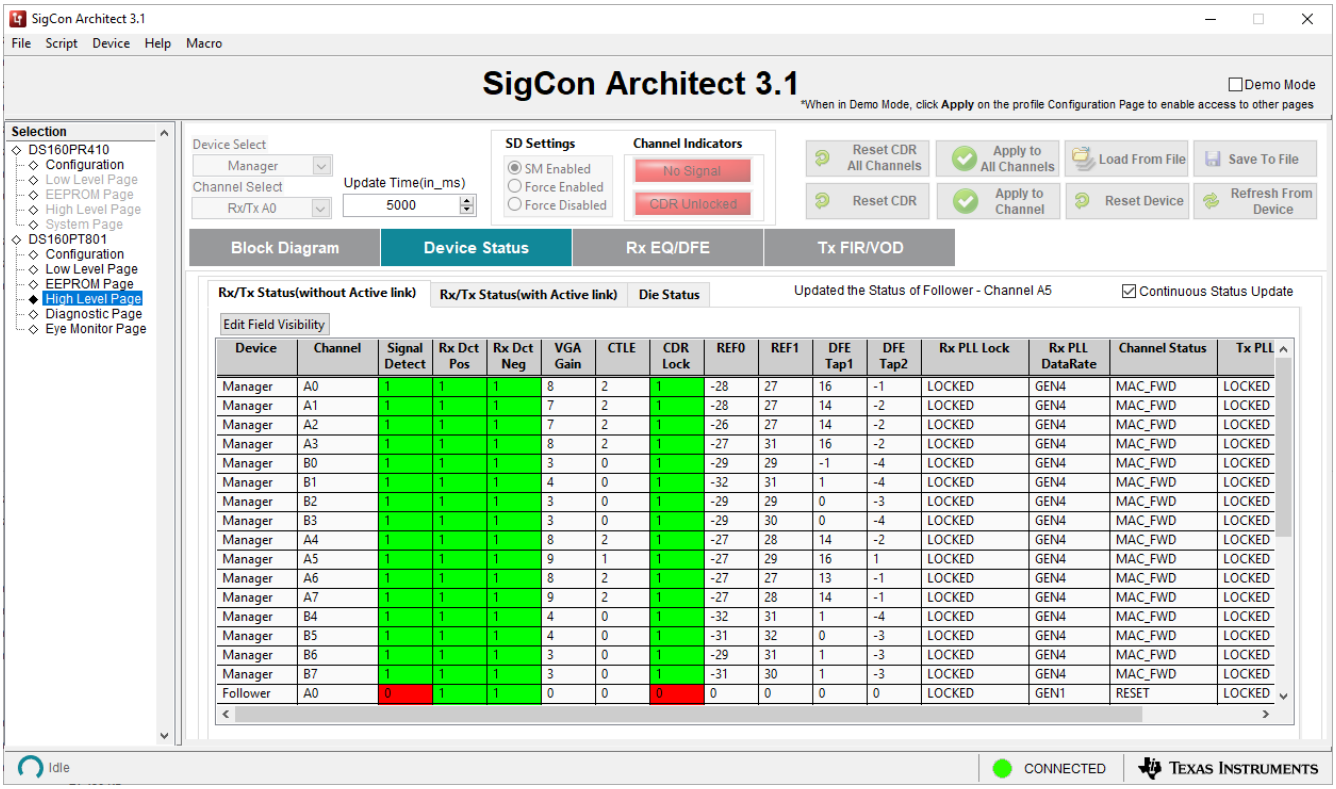


Figure 3-5. High-Level Page Screenshot

The High-Level page of the DS160PT801 SigCon Architect GUI provides a user-friendly display of the current status of the retimer along with basic configuration. It contains multiple tabs within the page; the first tab of the page is the Block Diagram, which shows the analog signal components of the DS160PT801 retimer. This page will automatically read the current register link-width setting of the retimer and display it on the left side of the window. The fields that can be used on this page are as follows:

- **Bifurcation Options Dropdown** allows a user to select from all link width bifurcation options for the PCIe link.
- **Disable Retimer Present Checkbox** allows the retimer to disable the broadcasting of its presence in the PCIe link over the PCIe protocol.
- **Initialize Button** applies the Bifurcation and Retimer Present changes to the retimer over SMBus communication. It is important to note than any SMBus settings affecting PCIe link configuration like the link-width will not take effect after a PCIe link has already been established.



Device	Channel	Signal Detect	Rx Dct Pos	Rx Dct Neg	VGA Gain	CTLE	CDR Lock	REF0	REF1	DFE Tap1	DFE Tap2	Rx PLL Lock	Rx PLL DataRate	Channel Status	Tx PLL
Manager	A0	1	1	1	8	2	1	-28	27	16	-1	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	A1	1	1	1	7	2	1	-28	27	14	-2	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	A2	1	1	1	7	2	1	-26	27	14	-2	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	A3	1	1	1	8	2	1	-27	31	16	-2	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	B0	1	1	1	3	0	1	-29	29	-1	-4	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	B1	1	1	1	4	0	1	-32	31	1	-4	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	B2	1	1	1	3	0	1	-29	29	0	-3	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	B3	1	1	1	3	0	1	-29	30	0	-4	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	A4	1	1	1	8	2	1	-27	28	14	-2	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	A5	1	1	1	9	1	1	-27	29	16	1	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	A6	1	1	1	8	2	1	-27	27	13	-1	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	A7	1	1	1	9	2	1	-27	28	14	-1	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	B4	1	1	1	4	0	1	-32	31	1	-4	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	B5	1	1	1	4	0	1	-31	32	0	-3	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	B6	1	1	1	3	0	1	-29	31	1	-3	LOCKED	GEN4	MAC_FWD	LOCKED
Manager	B7	1	1	1	3	0	1	-31	30	1	-3	LOCKED	GEN4	MAC_FWD	LOCKED
Follower	A0	0	1	1	0	0	0	0	0	0	0	LOCKED	GEN1	RESET	LOCKED

Figure 3-6. High-Level Page – Device Status Screenshot

The device status tab in the High-Level page have multiple sub-tabs with information about the retimer status. The Rx/Tx status (without Active link) shows status information that does not require an active PCIe link to be valid. This includes receiver detection, signal detection, and equalizer signal conditioning settings.

- **Edit Field Visibility Button** allows a user to show or hide different columns within the channel status table.

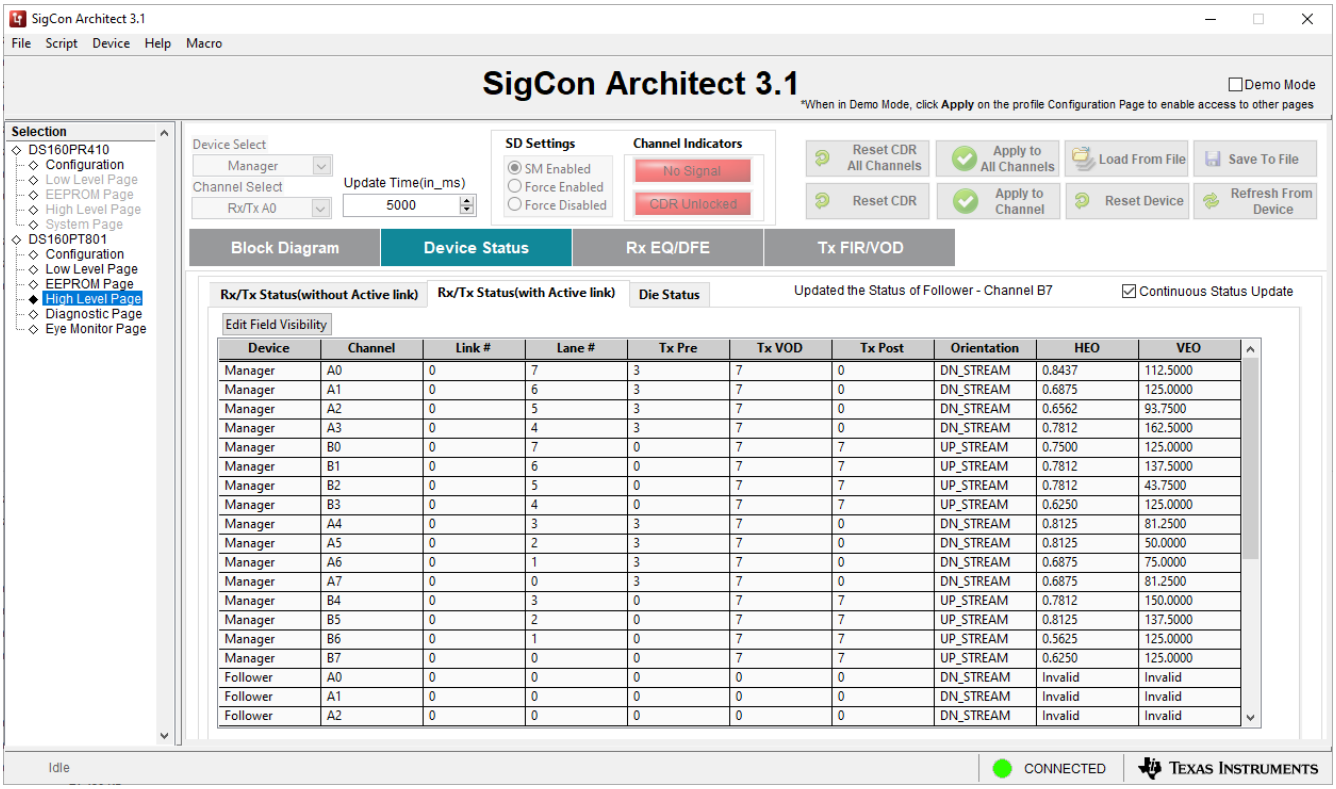


Figure 3-7. High Level Page – Device Status (Active Link) Screenshot

After a link is established, there are a number of fields that are updated in the retimer to reflect the current status of the PCIe link. This includes the Link, Lane number, and orientation of the data flow.

- **Edit Field Visibility Button** allows a user to show or hide different columns within the channel status table.

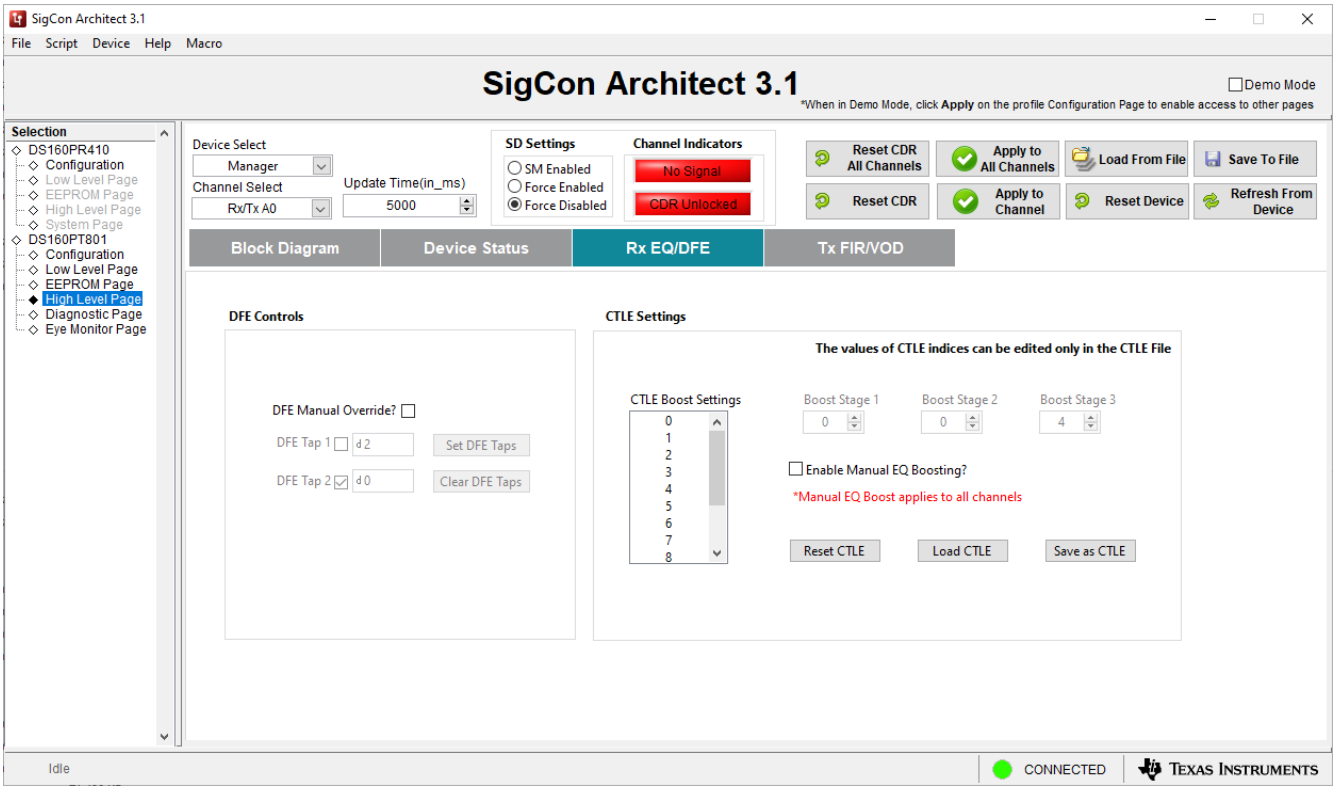


Figure 3-8. High-Level – Rx EQ/DFE Page

This section of the High-Level page allows a user to force the CTLE settings of the DS160PT801. Both the CTLE and DFE is automatically adaptive by default, and changing these values is generally not needed. However, when performing evaluation or when the retimer is not actively participating in PCIe protocol, such as during PRBS checking, it may be useful to set these to a static value.

- **DFE Manual Override? Checkbox** enables a user to override the DFE values
- **DFE Tap 1 Checkbox** enables override for DFE Tap 1
- **DFE Tap 2 Checkbox** enable override for DFE Tap 2
- **Set DFE Taps Button** applies the DFE settings shown in the GUI to the retimer through SMBus
- **Clear DFE Taps Button** resets the DFE Tap values to 0
- **CTLE Boost Settings List** allows a user to select from the pre-configured CTLE Indexes. Selecting higher values indicates a higher gain.
- **Boost Stage 1 Field** modifies the index setting for the first stage of the CTLE equalizer.
- **Boost Stage 2 Field** modifies index setting for the second stage of the CTLE equalizer.
- **Boost Stage 3 Field** modifies index setting for the third stage of the CTLE equalizer.
- **Enable Manual EQ Boosting? Checkbox** enables a user to finely control the boost stage settings for the CTLE.
- **Reset CTLE Button** resets the CTLE Index to 0
- **Load CTLE Button** loads a saved pre-configured CTLE value
- **Save as CTLE Button** saves the currently selected CTLE configuration in a .ini file.

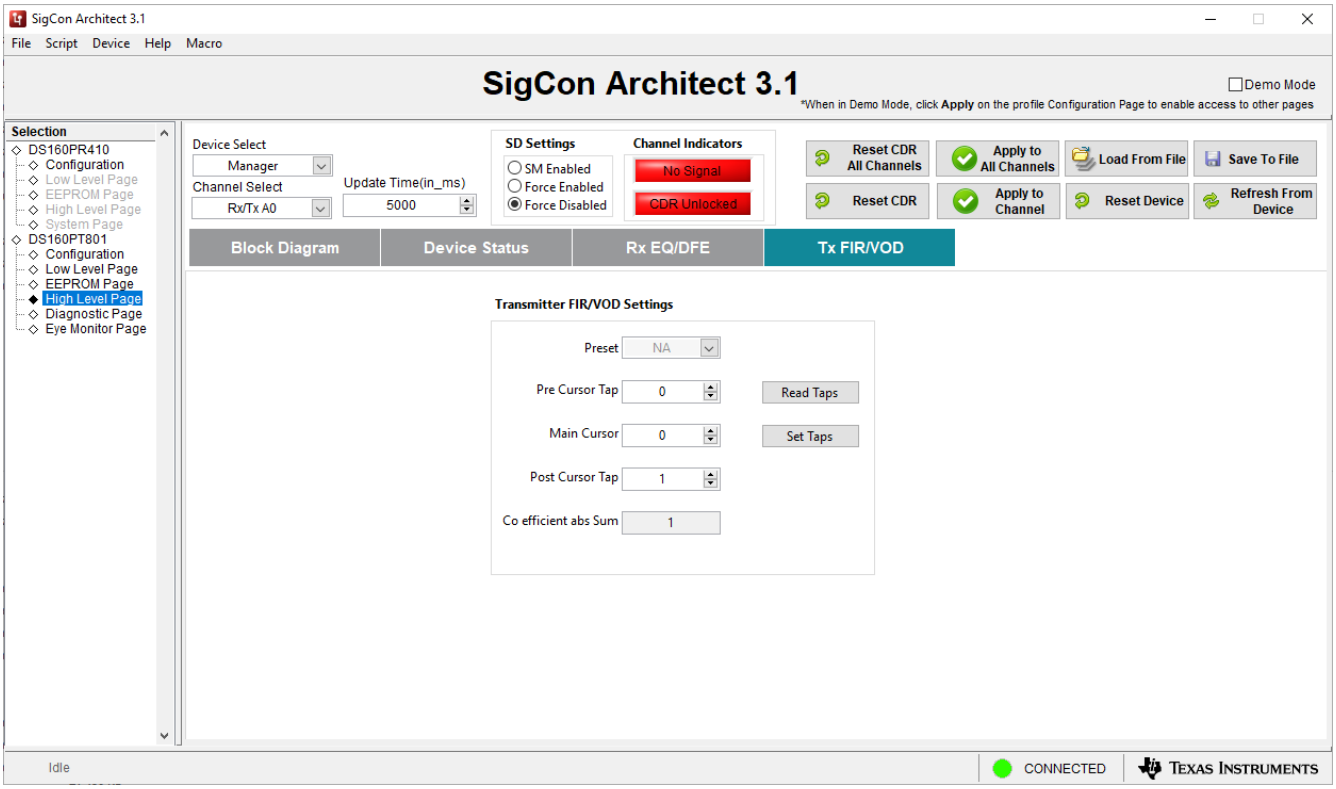


Figure 3-9. High-Level Page Tx FIR

The Tx FIR/VOD tab allows a user to control the coefficient values of the FIR filter at the transmitter of the DS160PT801. These values are auotmatically negotiated through the PCIe protocol, manually changing them would cause the retimer to operate outside of specification. For this reason the FIR values should only be changed when the retimer is not actively participating in PCIe protocol, such as while using the PRBS generator.

- **Preset Dropdown** changes the PCIe preset value of the DS160PT801's transmitters. This will update the pre, post, and main cursor value.
- **Pre Cursor Tap Field** sets the pre cursor value for the Tx FIR.
- **Main Cursor Field** sets the main cursor value for the Tx FIR.
- **Post Cursor Tap Field** sets the post cursor value for the Tx FIR.
- **Co efficient abs Sum Field** displays the absolute value of the Pre, Post, and Main cursor.

- **Read Taps Button** reads the current value of the Tx FIR taps.
- **Set Taps Button** set the Tx FIR tap values to what is currently shown in the GUI.

3.7 Diagnostic Page

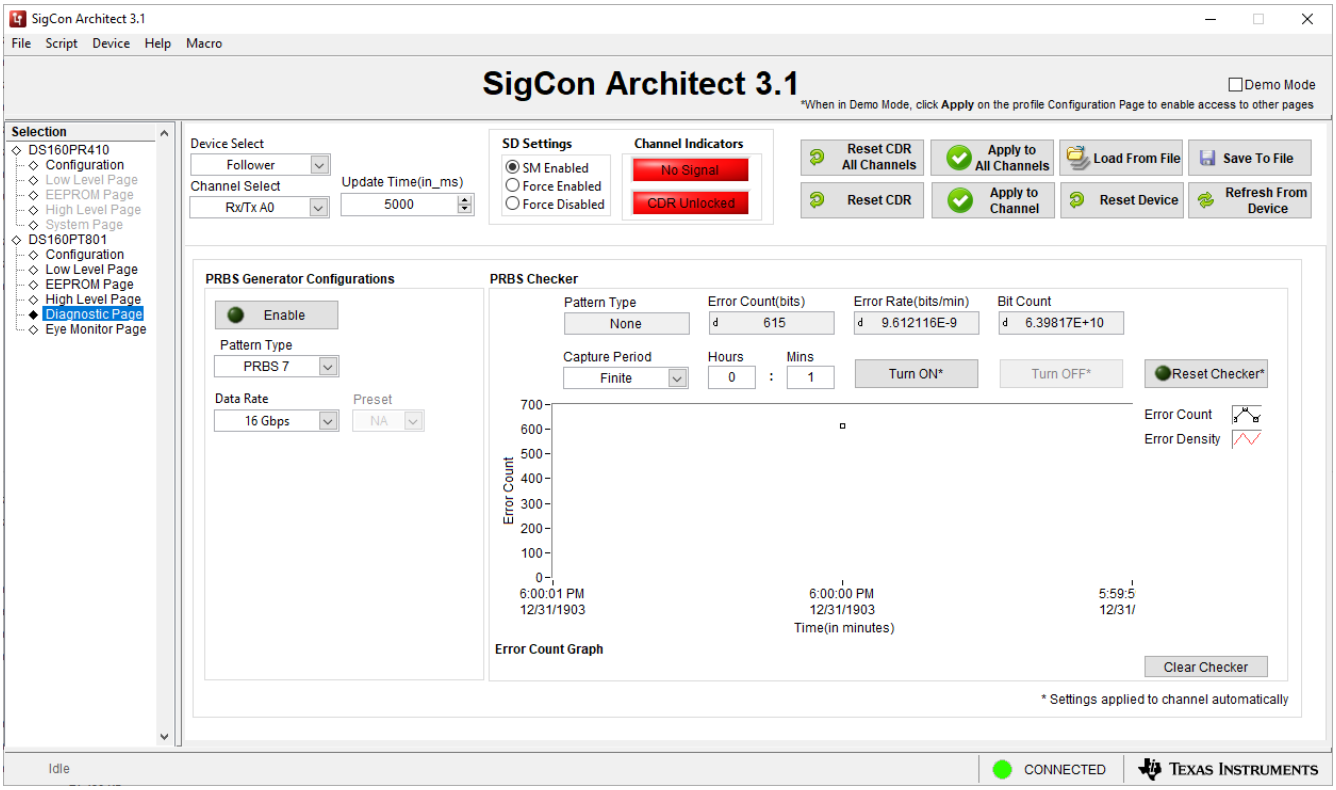


Figure 3-10. Diagnostic Page Screenshot

The Diagnostic page contains features of the retimer that are meant to be used for evaluating the signal integrity of a system. By using the PRBS Checker and PRBS Generator functions of the retimer, it is possible to determine the Bit Error Ratio (BER) of a channel. This operational mode of the retimer does not operate through the PCIe protocol. It forced the retimer to simply transmit an electrical pattern specified by a user. There is also an option to force the transmission of a specific PCIe compliance pattern. The fields available in this page are as follows:

- **Enable Button** enables or disables the PRBS or compliance pattern generator with the specified pattern type and datarate. If using a PCIe compliance pattern, it is possible to also force a specific PCIe preset value for the transmitted signal.
- **Pattern Type Dropdown** modifies the pattern that is transmitted by the retimer.
- **Data Rate Dropdown** changes the datarate of the signal transmitted.
- **Preset Dropdown** will change the PCIe of the output signal when a compliance pattern is selected in the pattern type dropdown.
- **Capture Period Dropdown** modifies the time period used to capture and count errors using the PRBS Checker.
- **Turn ON* Button** turns on the PRBS checker.
- **Turn OFF* Button** turns off the PRBS checker.
- **Reset Checker*** resets the error count for the PRBS checker.
- **Error Count Graph** displays the amount of errors accumulated by the PRBS checker over time.
- **Clear Checker Button** clears the error count graph.

3.8 Eye Monitor Page

Figure 3-11. Eye Monitor Page Screenshot

The Eye Monitor page allows a user to check the eye openining of a signal at the retimer receiver after completing CTLE and DFE equalization. This feature can only be used reliably when a PCIe link is stable enough to maintain the L0 link state. The fields available in the Eye Monitor page are as follows:

- **Single Capture Button** creates a single eye diagram from in the incoming signal on the selected channel and stops capturing.
- **Continuous Capture** monitors the eye diagram from in the incoming signal on the selected channel by continuously creating eye diagrams unil the user stops the capture.
- **Stop Capture** stops a continuous capture.
- **Recompute HEO/VEO** performs a quick measurement of the HEO and VEO of a channel. This method uses the same technique on the high-level device status page to calculate the HEO and VEO.
- **Rx Margin Count Select Dropdown** selects the number of bits used when performing Rx margining.
- **Rx Margin Error Select** modifies the maximum number of errors allowed for each sample point when performing Rx margining.
- **Export Raw Data Button** exports the pass or fail results of an eye diagram measurement.
- **Export Density** exports the results of an eye diagram including error density information.
- **Clear Plots** clears the Raw Data, Error Hit Count, and Contour data graphs.

4 PCB Material Information

4.1 DS160PT801 PCB Design

- 62 mils – 12 layer design
- PCIe data traces are 85-Ω target
- PCIe clock traces are 100-Ω target

4.2 DS160PT801 PCB Stackup

Figure 4-1 illustrates the DS160PT801X16EVM PCB stackup.

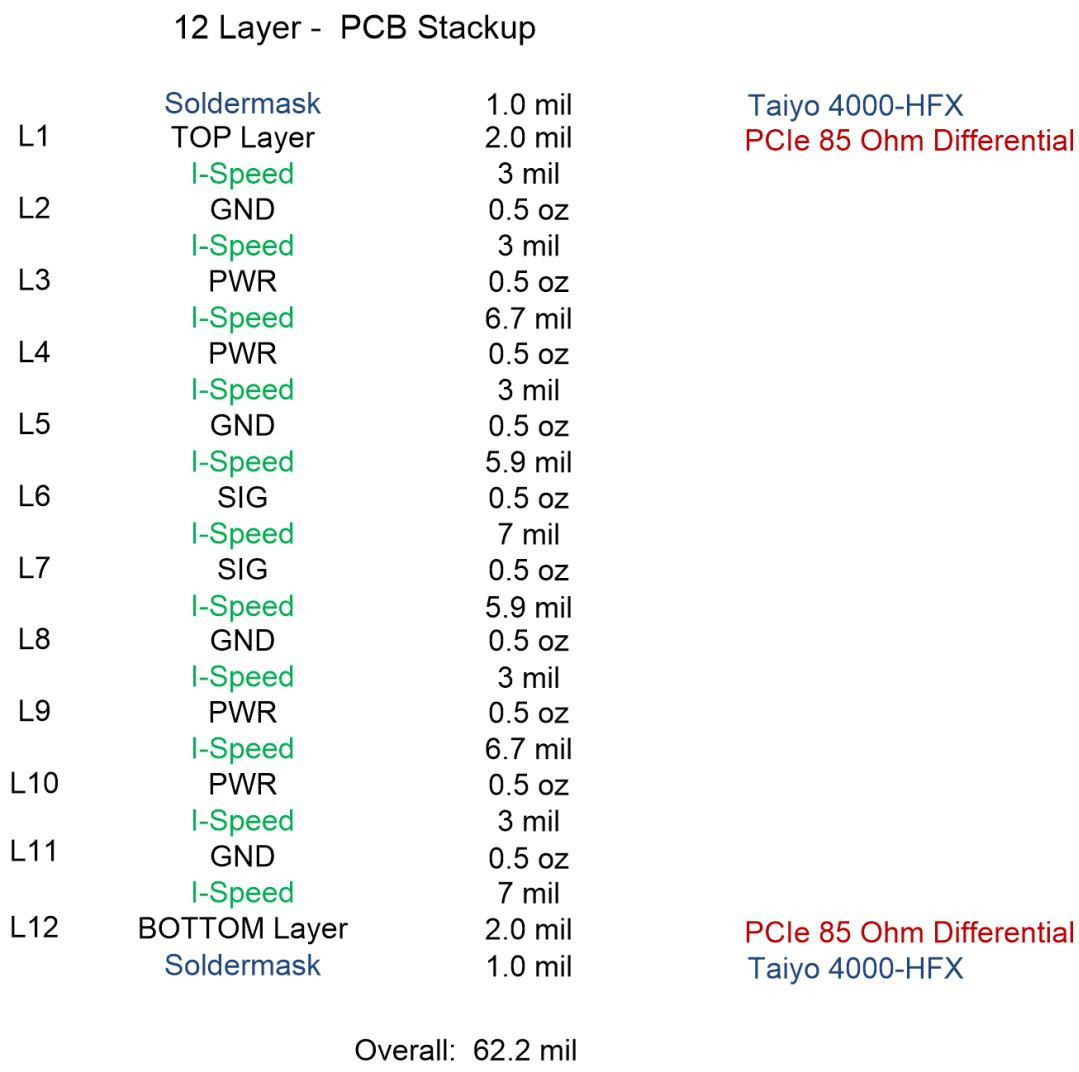


Figure 4-1. DS160PT801X16EVM PCB Stackup

4.3 DS160PT801 PCB Power Distribution

The riser card power distribution network was designed for observation and performance. Four power layers were dedicated to retimer supply voltages. This improves isolation between sensitive analog circuits and reduces losses where high dynamic currents are present.

Layer 3 and Layer 4 in the stackup are dedicated to the high-speed analog and digital supply rails. Both of these rails are nominally 1.1-V voltage levels. Using two layers as close to the mounted DS160PT801 as possible improves decoupling performance and aligns with internal package power supply design. Note that previous designs with a single PWR2_HSD supply are completely compatible with the Revision C pre-production silicon used on this EVM.

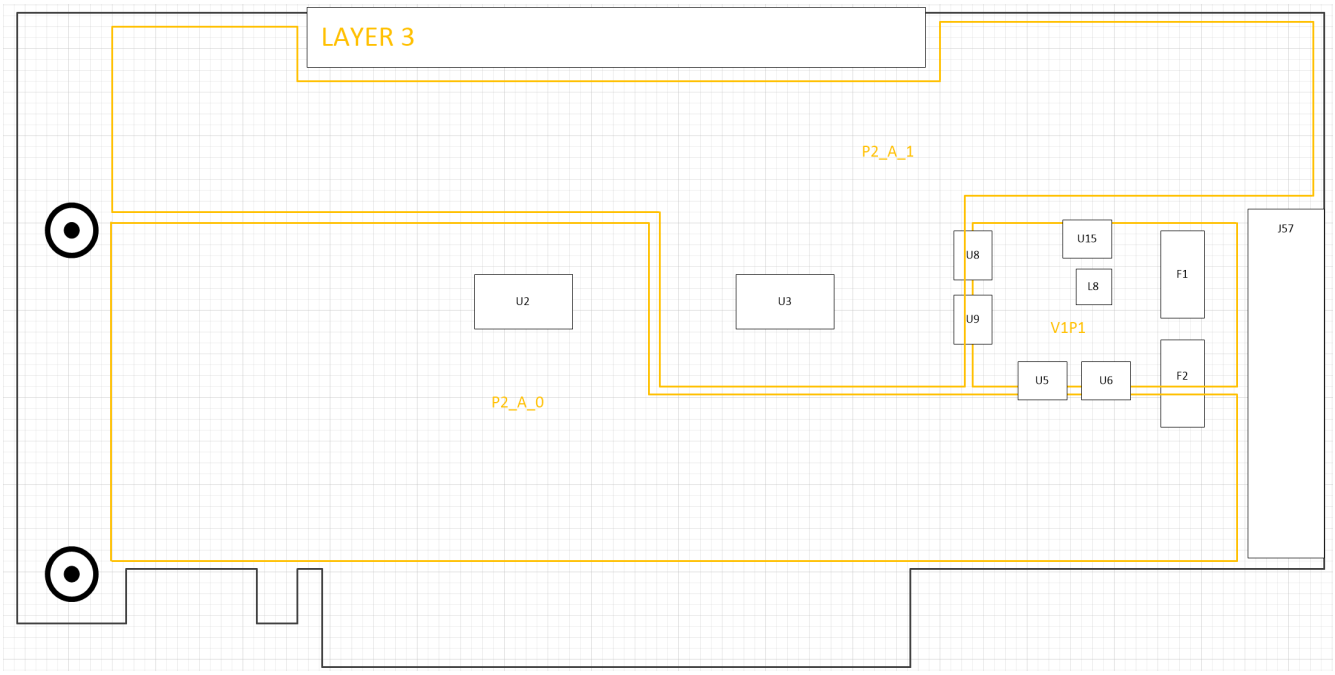


Figure 4-2. Layer 3 High-Speed Analog Analog Power Rails

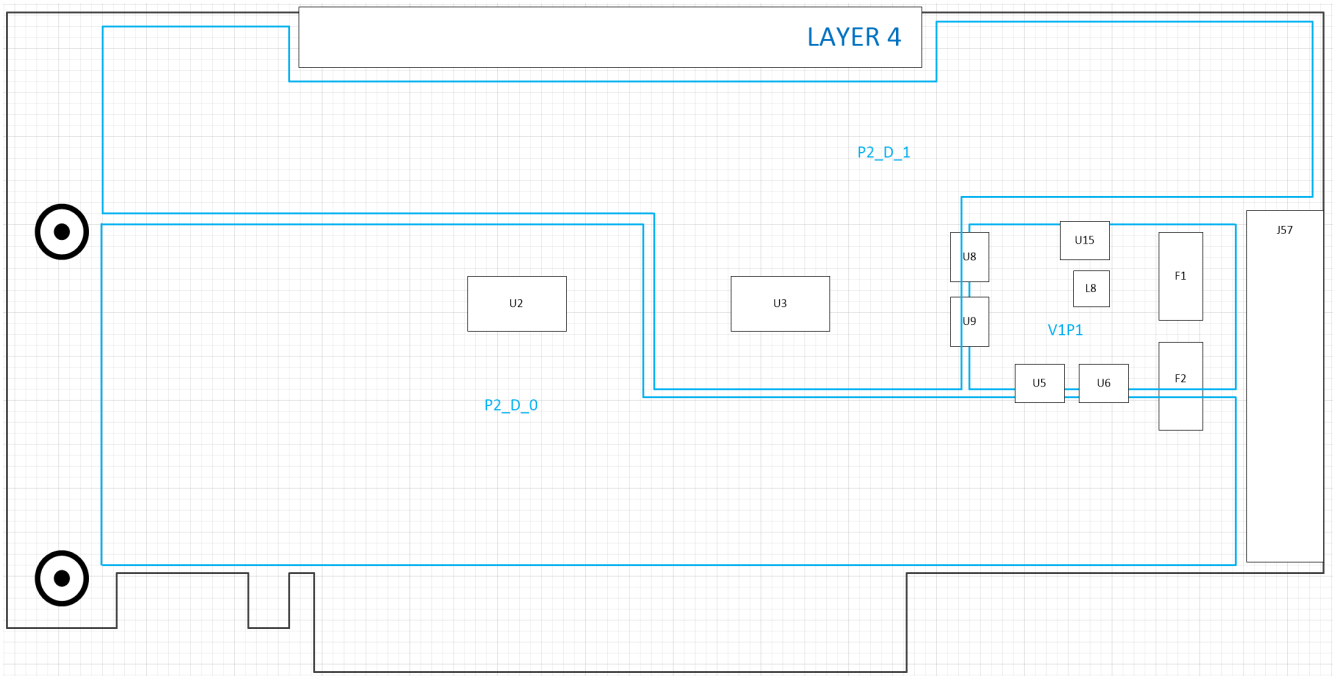


Figure 4-3. Layer 4 Digital Power Rails

Layer 9 and Layer 10 are used to supply the analog voltages. These retimer supplies are lower current and have relatively constant demand so placements lower in the PCB stackup match their requirements. In addition to retimer supply needs, these layers are also used to provide 3-V and 12-V levels to the attached endpoint and regulator inputs.

As with any Serdes, hardware design power distribution is important to the overall device performance. To ensure optimal voltage levels at the retimer devices, the main 1.1-V regulator uses a remote sense line directly to the U2 retimer. This helps to compensate for any losses on the PCB between the regulator and the device load.

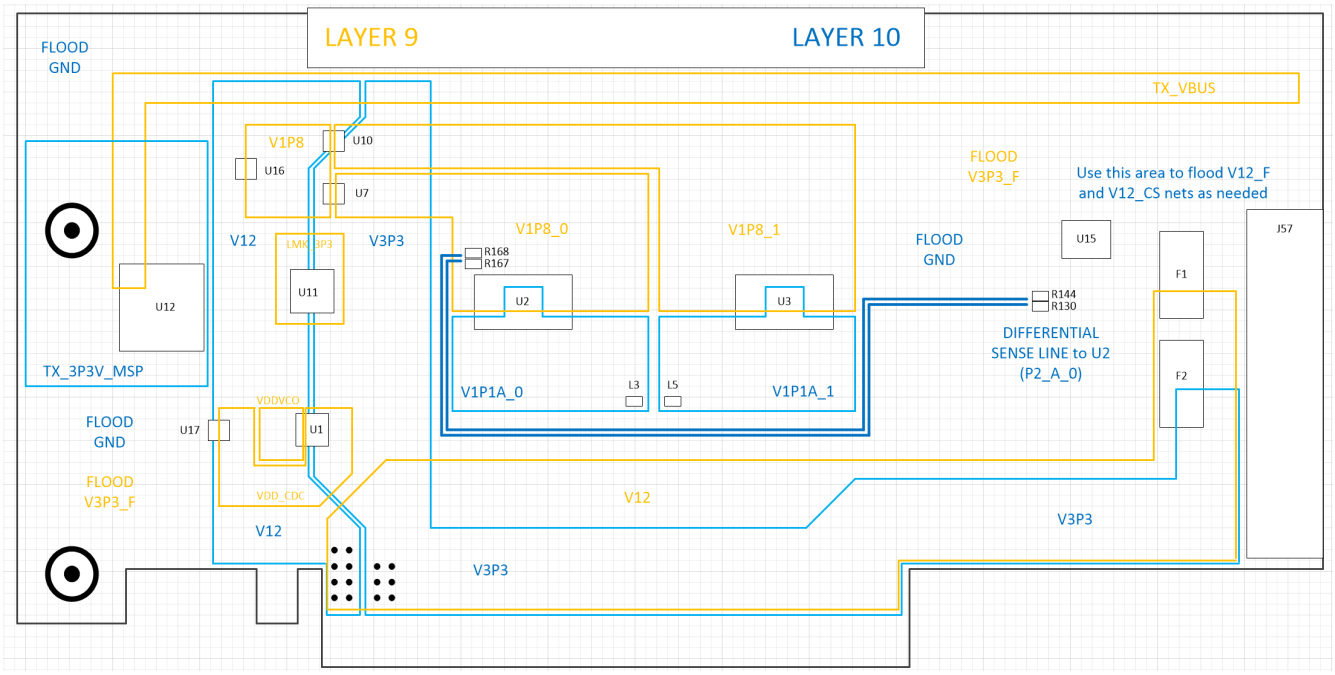


Figure 4-4. Layer 9 and 10 Power Distribution

4.4 DS160PT801 Local Decoupling

To complement the PCB power layers, decoupling capacitors have been arranged to filter device noise. The design of the high-current analog and digital decoupling uses *Top* and *Bottom* layer capacitors to optimize the overall frequency response of the decoupling solution.

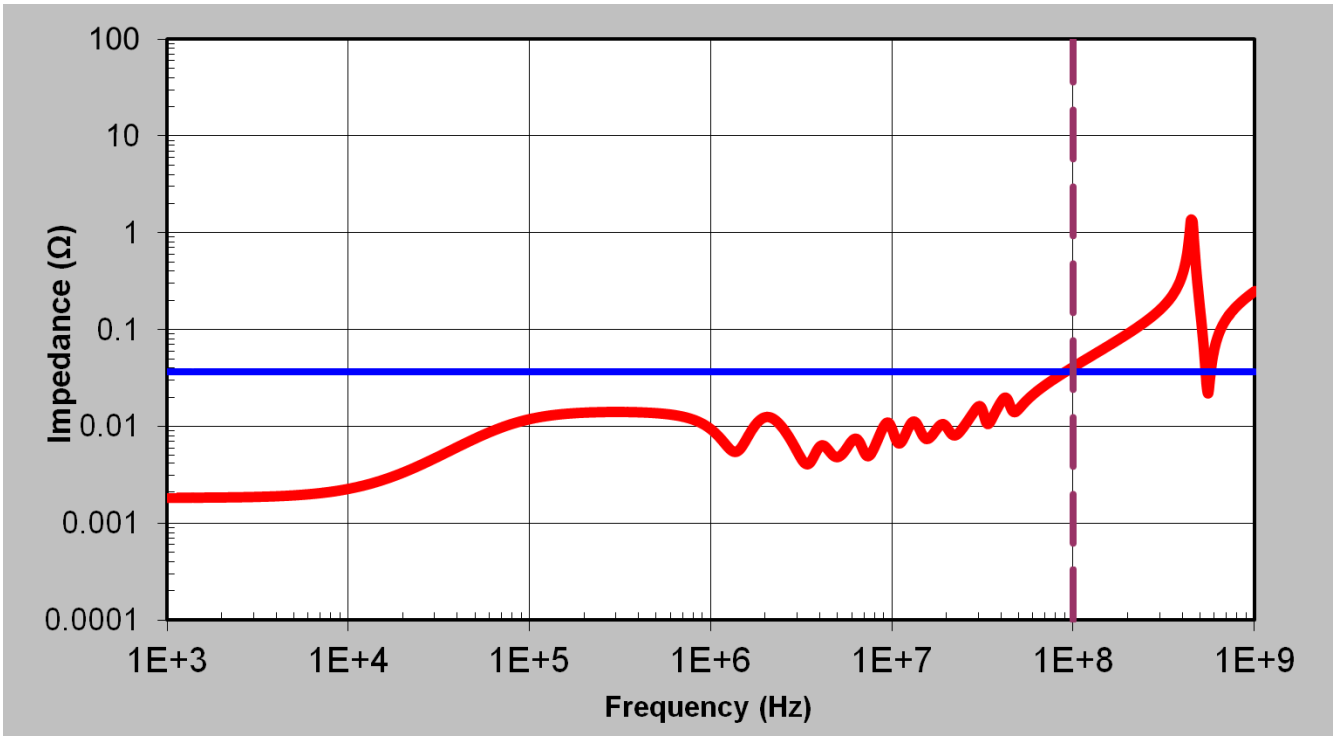


Figure 4-5. Decoupling Solution Frequency Response

Extending the targeted frequency range out to 100 MHz ensures digital noise associated with the PCIe reference clock is minimized. The highest frequency components require very low inductance to perform well. Placing the high current supplies close to the *top layer* surface ensures the lowest inductance possible to the supply plane and ultimately to the device itself.

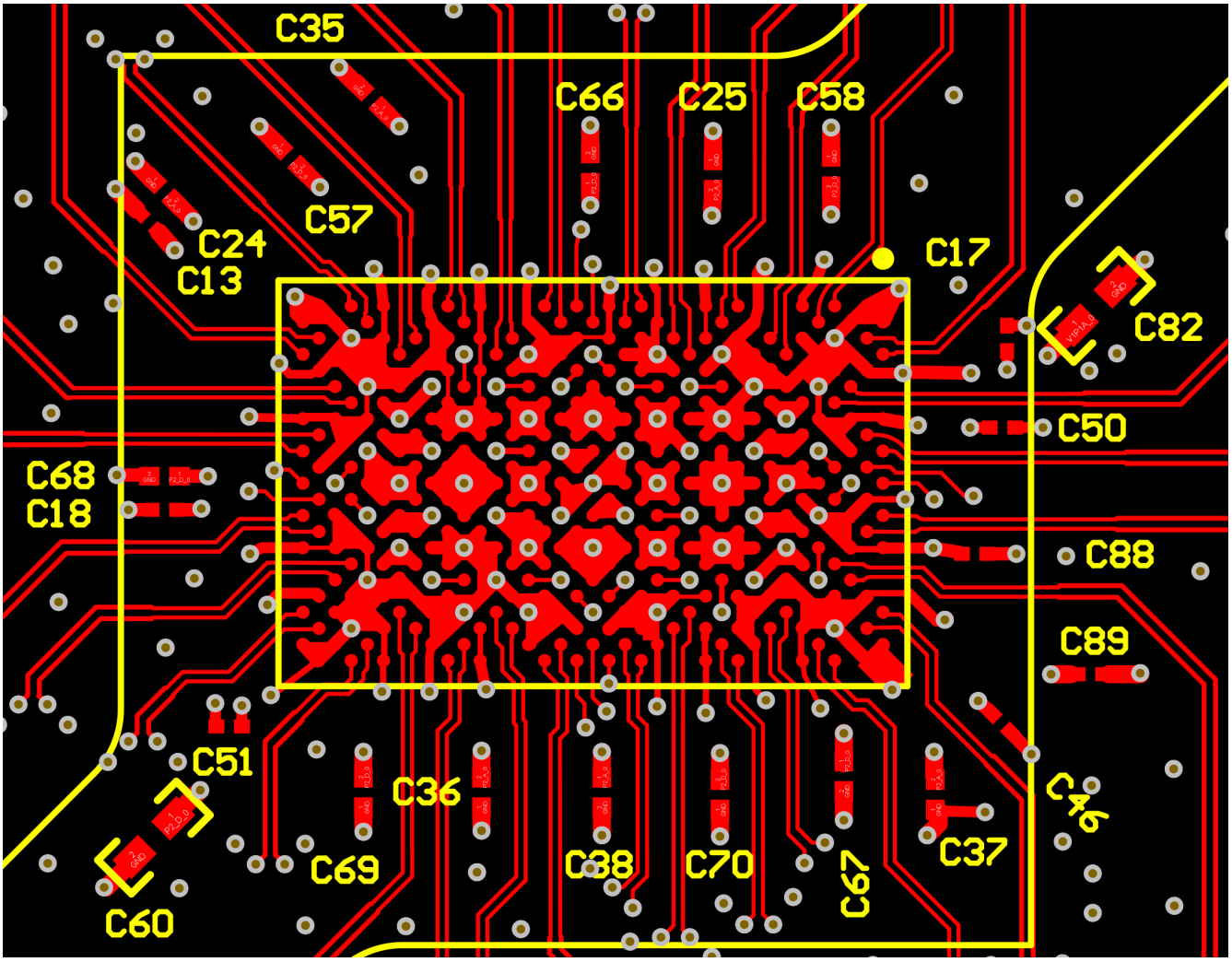


Figure 4-6. PCB Top Layer

5 DS160PT801X16EVM Schematic

Figure 5-1 through Figure 5-2 illustrate the DS160PT801X16EVM schematics.

Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A

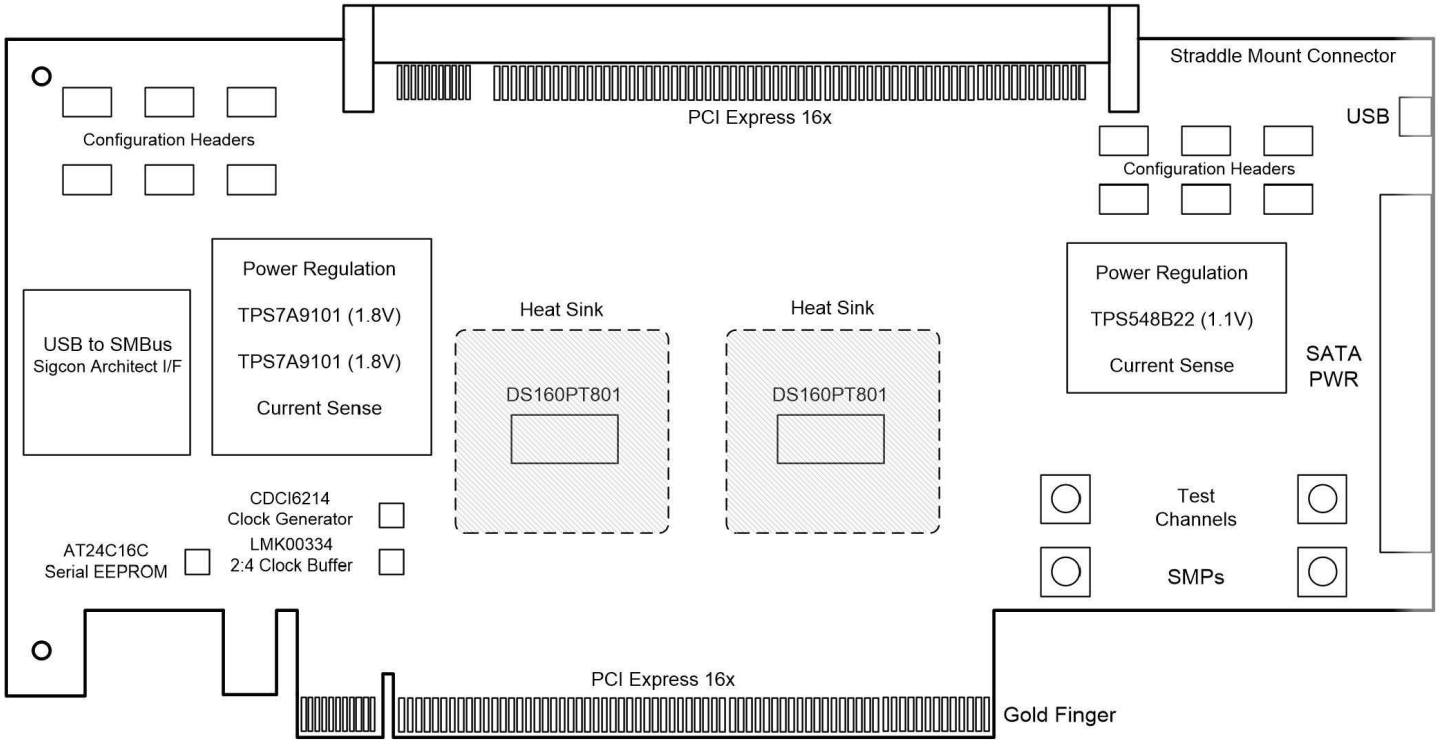


Figure 5-1. Schematic – Cover Sheet

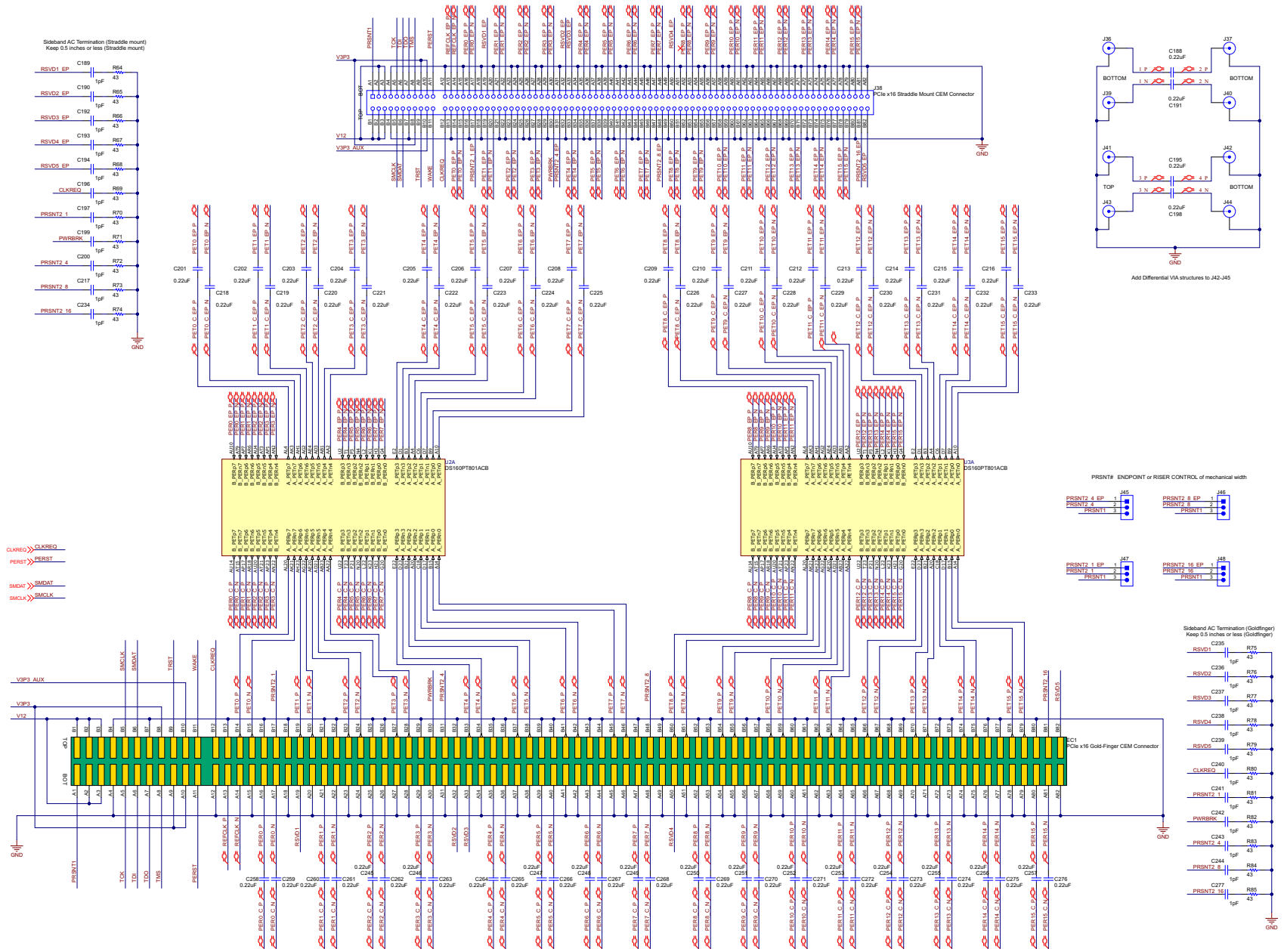


Figure 5-2. Schematic – High Speed

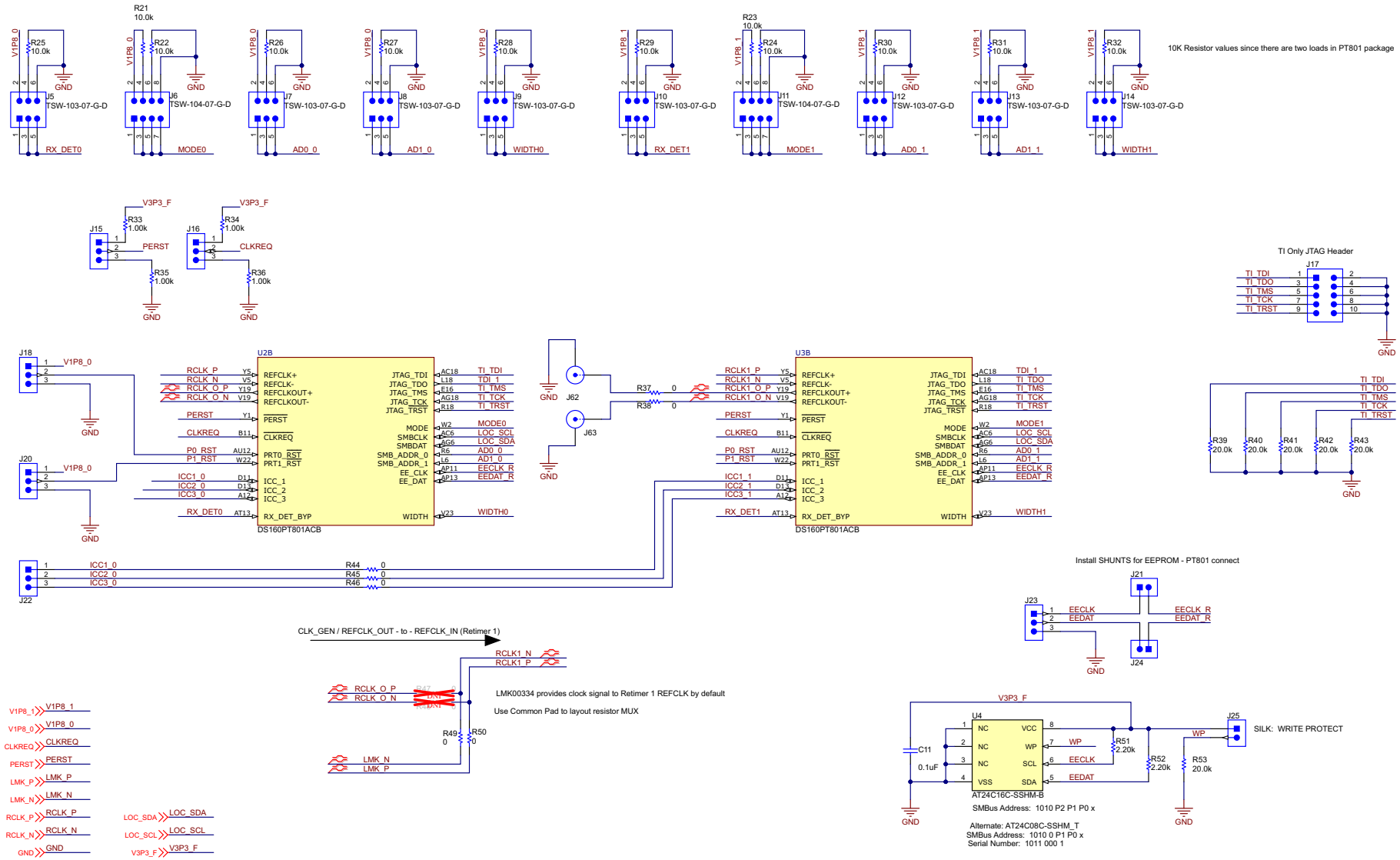


Figure 5-3. Schematic – Control

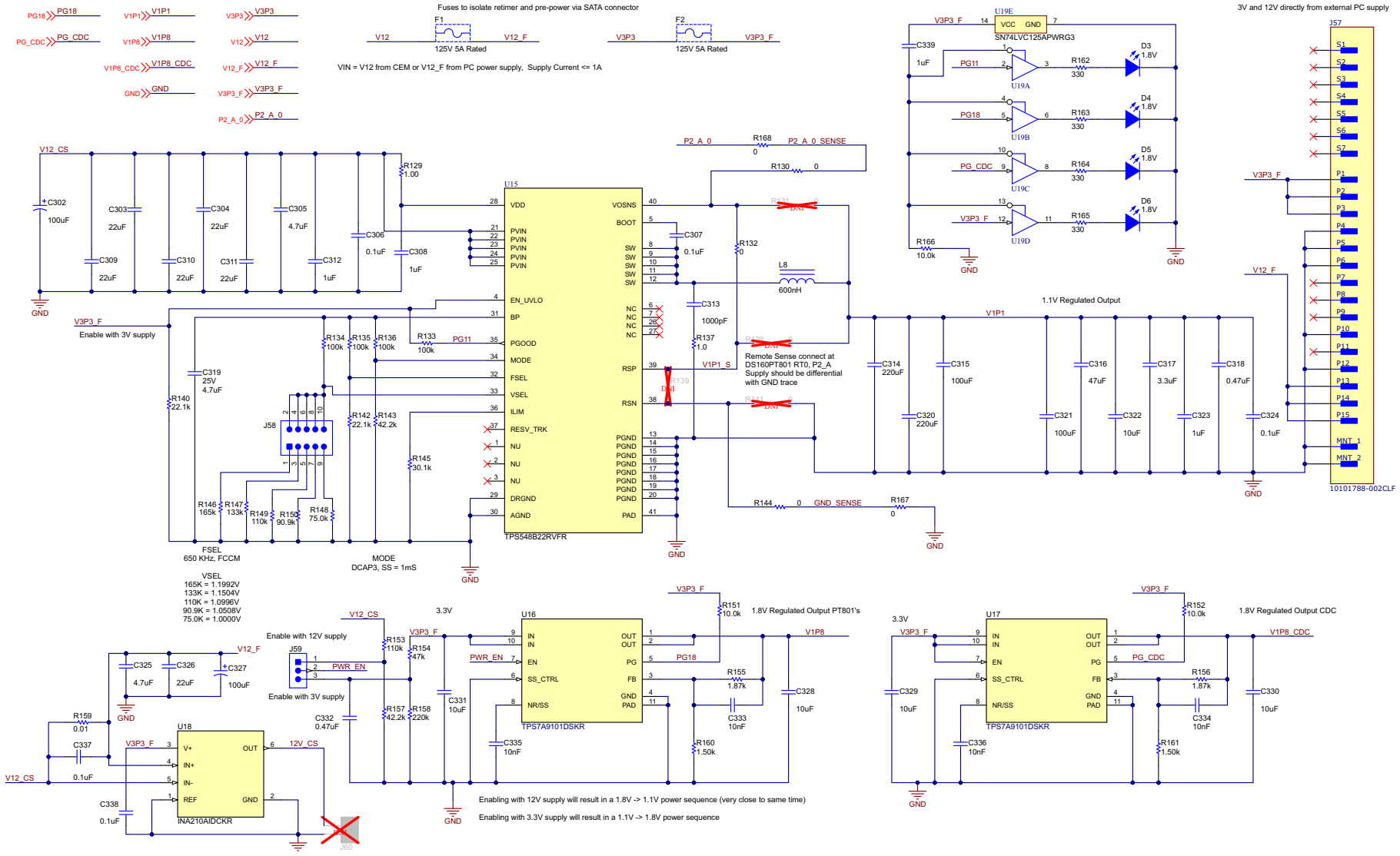


Figure 5-4. Schematic – Supply Voltage Regulators

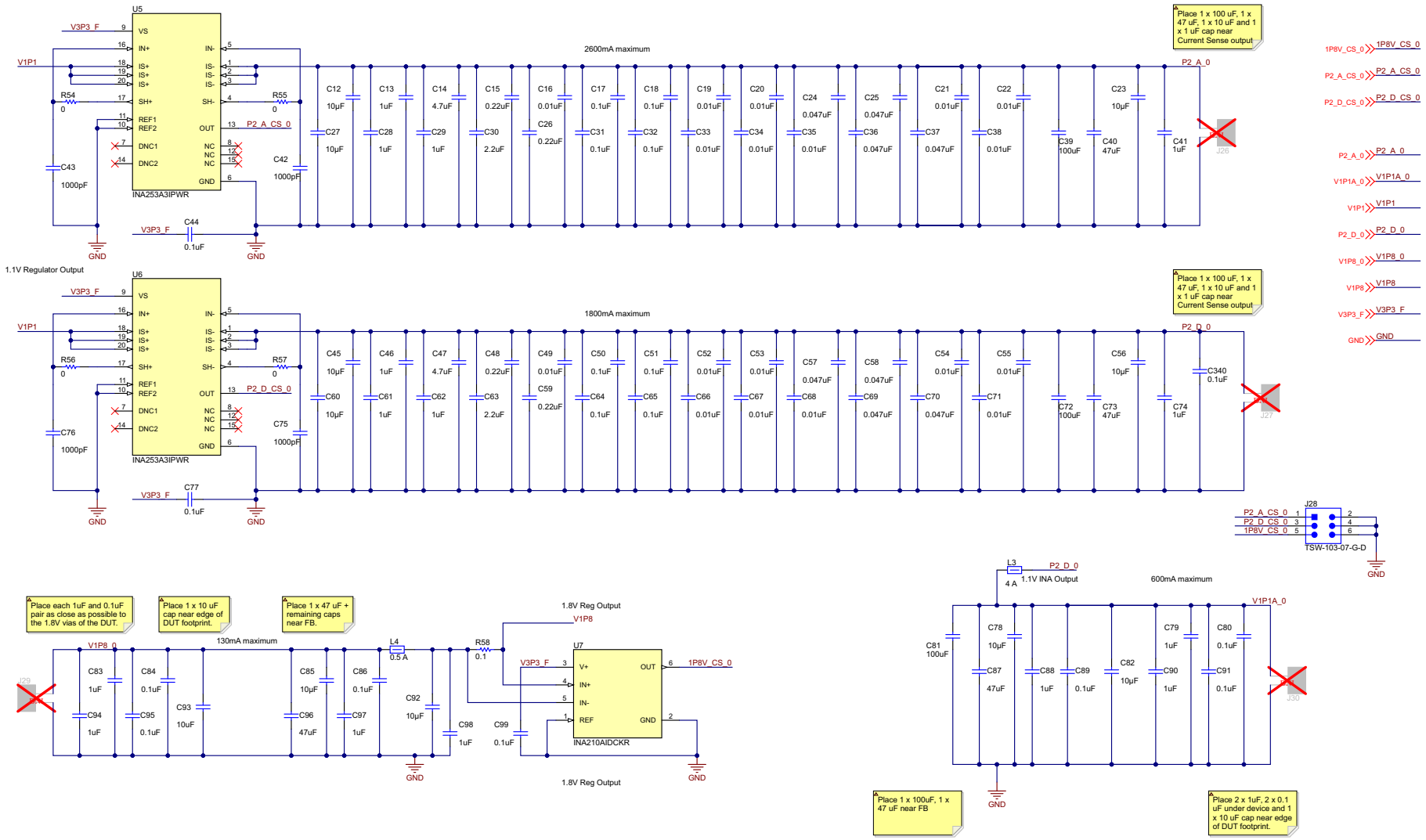


Figure 5-5. Schematic – Retimer 1 Current Sense and Decoupling

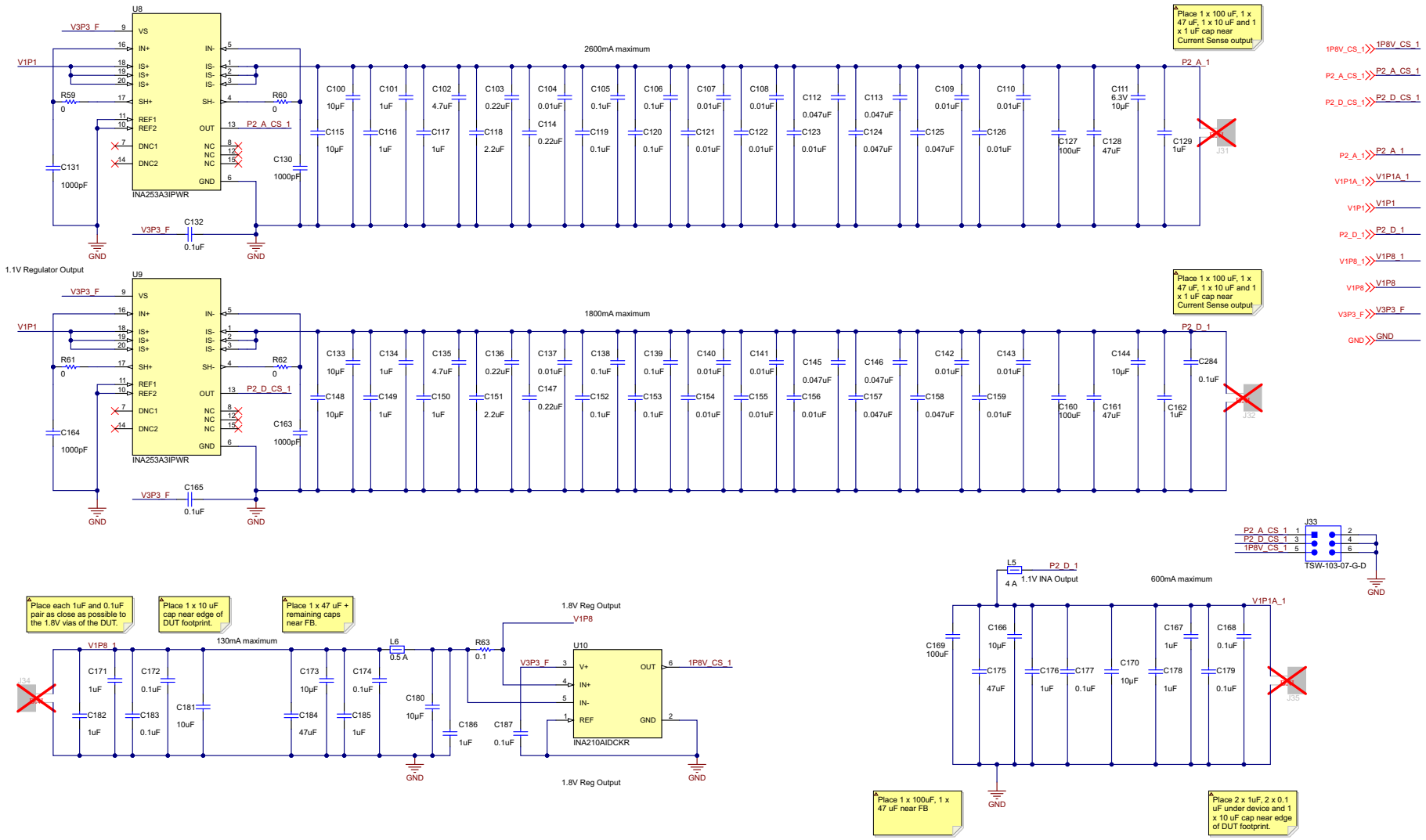


Figure 5-6. Schematic – Retimer 0 Current Sense and Decoupling

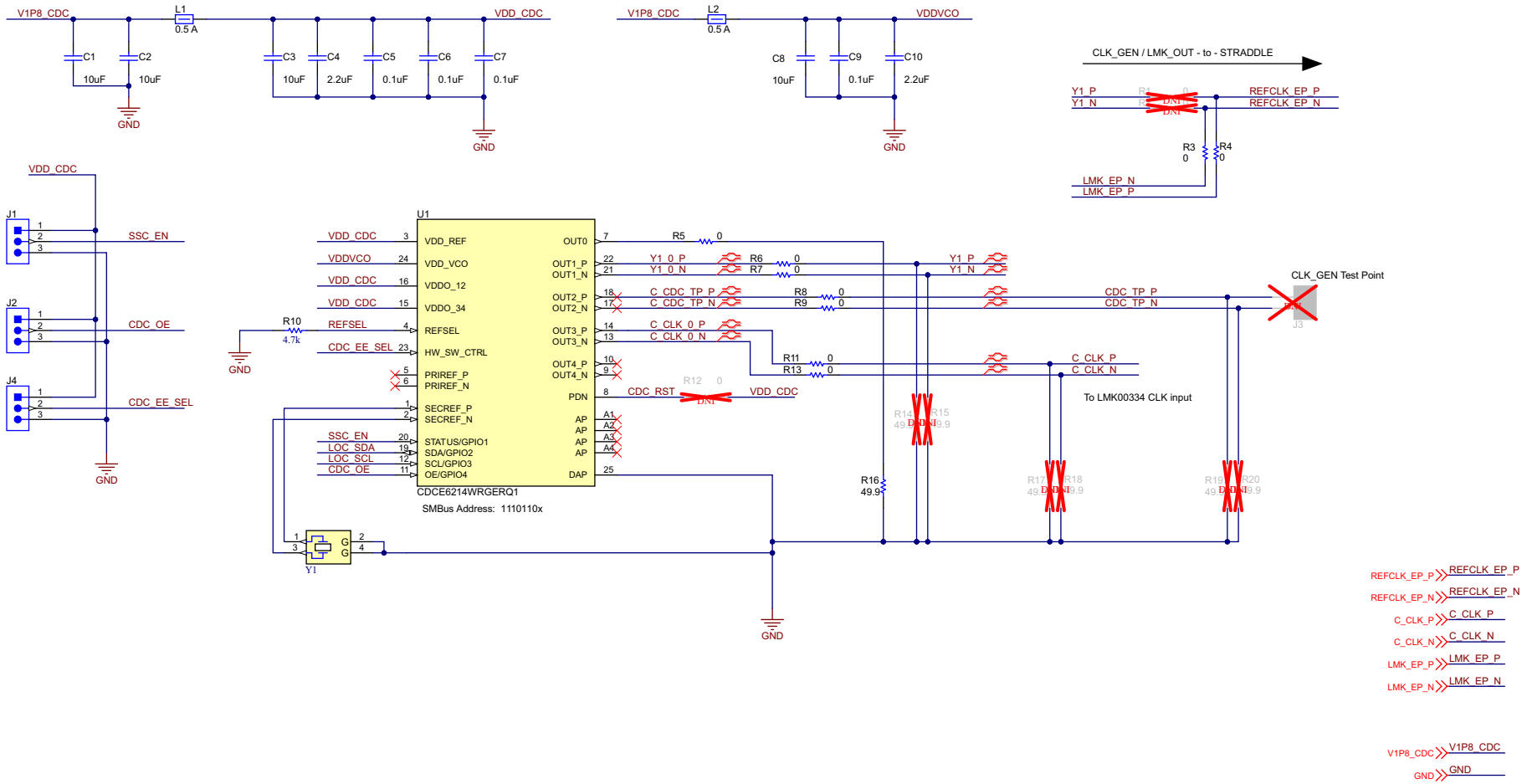


Figure 5-7. Schematic – PCIe Gen4 Clock Generation

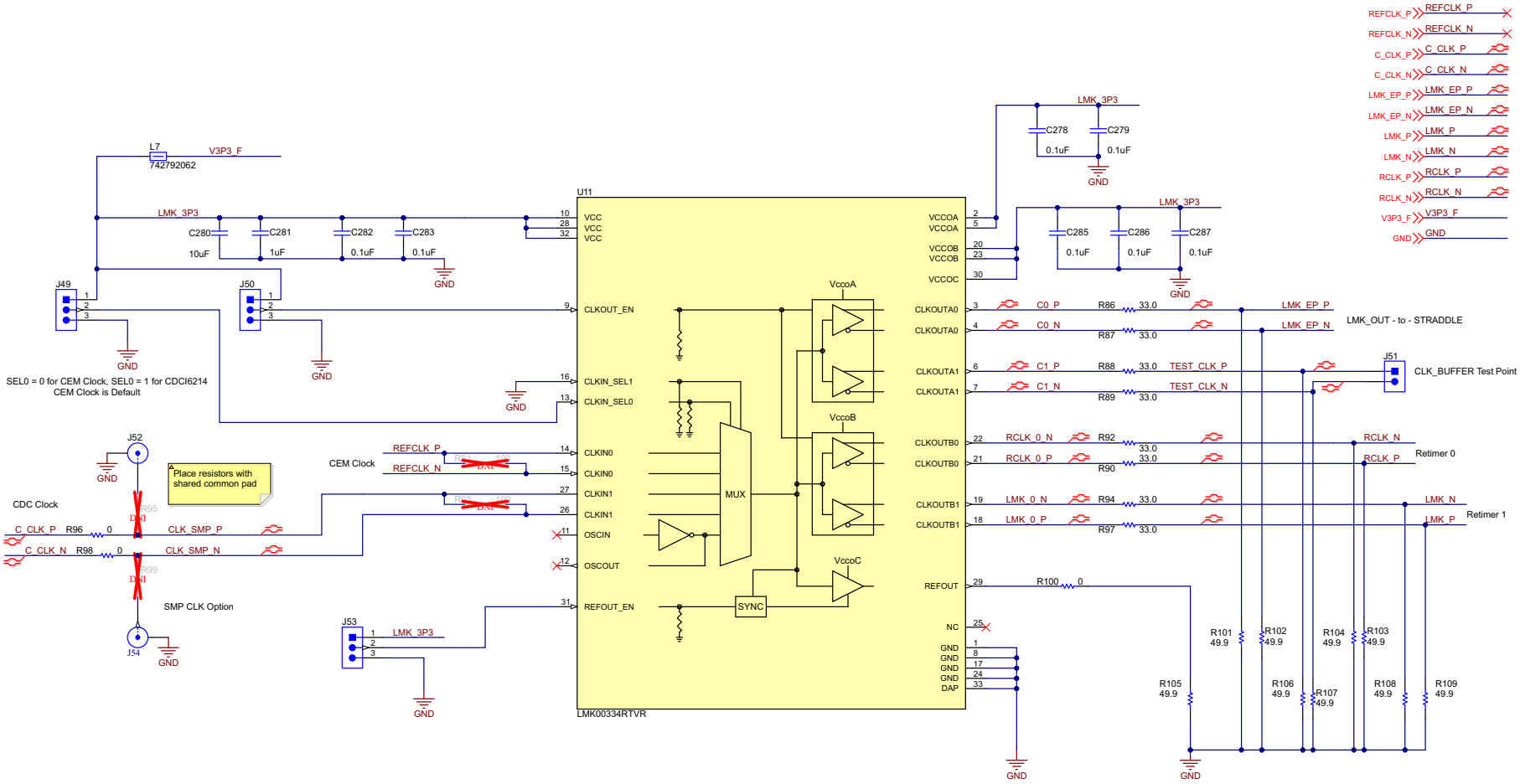


Figure 5-8. Schematic – PCIe Gen4 Clock Buffer

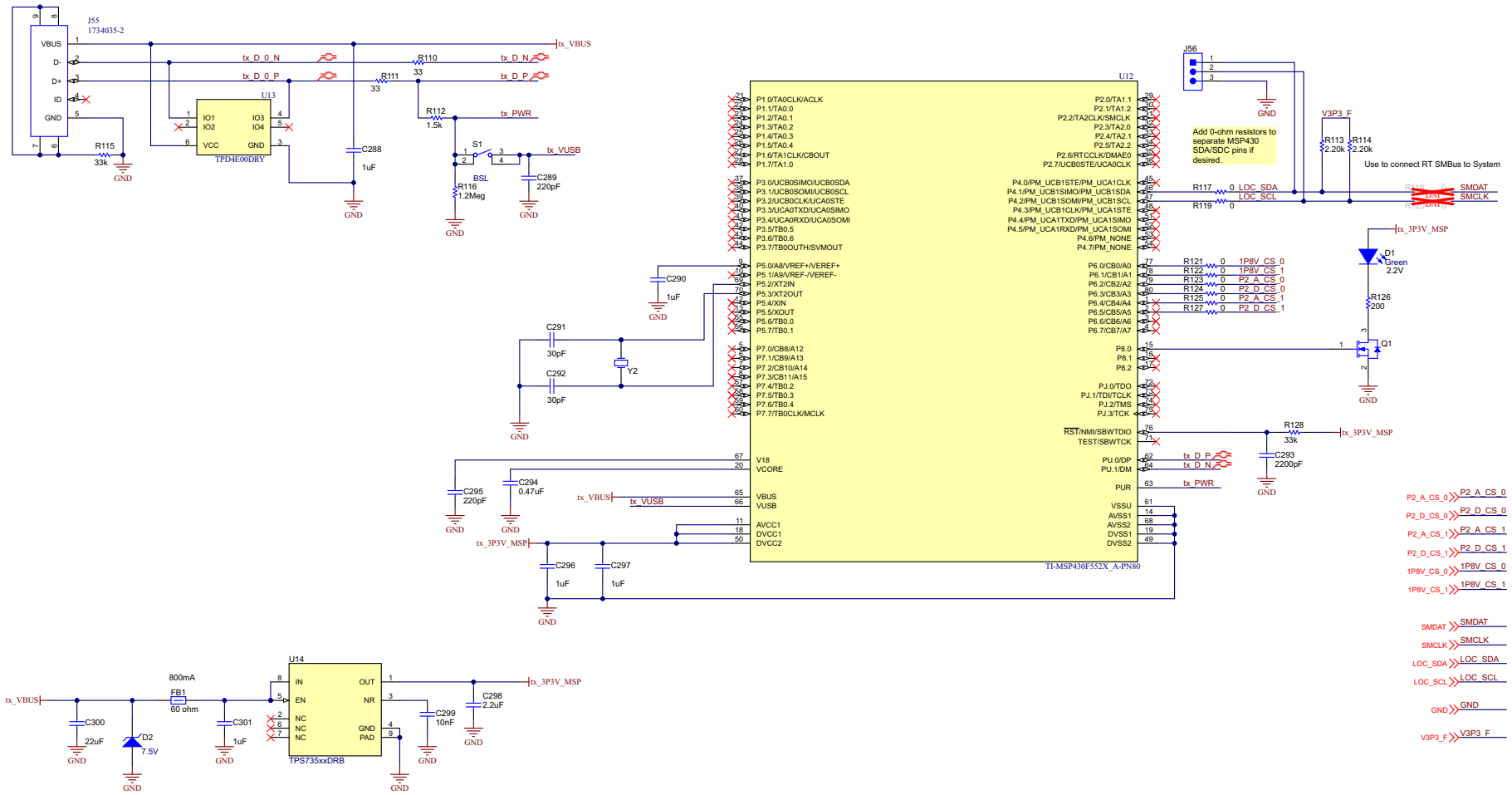


Figure 5-9. Schematic – MSP430 Microcontroller

6 Hardware BOM

Table 6-1 lists the DS160PT801X16EVM BOM.

Table 6-1. DS160PT801X16EVM Bill of Materials

Designator	QTY	Value	Description	Package	Part Number	Manufacturer
C1, C2, C3, C8, C93, C181, C280, C322, C328, C329, C330, C331	12	10 µF	CAP, CERM, 10 µF, 10 V, ± 10%, X5R, 0805	0805	C0805C106K8PACTU	Kemet
C4, C10	2	2.2 µF	CAP, CERM, 2.2 µF, 6.3 V, ± 10%, X6S, 0402	0402	GRM155C80J225KE95D	MuRata
C5, C6, C7, C9, C11, C17, C18, C31, C32, C44, C50, C51, C64, C65, C77, C80, C84, C86, C89, C91, C95, C99, C105, C106, C119, C120, C132, C138, C139, C152, C153, C165, C168, C172, C174, C177, C179, C183, C187, C278, C279, C282, C283, C284, C285, C286, C287, C338, C340	49	0.1 µF	CAP, CERM, 0.1 µF, 6.3 V, ± 10%, X5R, 0201	0201	GRM033R60J104KE19D	MuRata
C12, C23, C27, C45, C56, C60, C78, C82, C85, C92, C100, C111, C115, C133, C144, C148, C166, C170, C173, C180	20	10 µF	CAP, CERM, 10 µF, 6.3 V,± 20%, X5R, 0402	0402	GRM155R60J106ME47D	MuRata
C13, C28, C29, C41, C46, C61, C62, C74, C79, C83, C88, C90, C94, C97, C98, C101, C116, C117, C129, C134, C149, C150, C162, C167, C171, C176, C178, C182, C185, C186, C281	31	1 µF	CAP, CERM, 1 µF, 6.3 V, ± 20%, X5R, 0201	0201	GRM033R60J105MEA2D	MuRata
C14, C47, C102, C135	4	4.7 µF	CAP, CERM, 4.7 µF, 6.3 V, ± 20%, X5R, 0402	0402	GRM155R60J475ME87D	MuRata
C15, C26, C48, C59, C103, C114, C136, C147, C188, C191, C195, C198, C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C218, C219, C220, C221, C222, C223, C224, C225, C226, C227, C228, C229, C230, C231, C232, C233, C245, C246, C247, C248, C249, C250, C251, C252, C253, C254, C255, C256, C257, C258, C259, C260, C261, C262, C263, C264, C265, C266, C267, C268, C269, C270, C271, C272, C273, C274, C275, C276	76	0.22 µF	CAP, CERM, 0.22 µF, 6.3 V, ± 20%, X5R, 0201	0201	GRM033R60J224ME90	MuRata
C16, C19, C20, C21, C22, C33, C34, C35, C38, C49, C52, C53, C54, C55, C66, C67, C68, C71, C104, C107, C108, C109, C110, C121, C122, C123, C126, C137, C140, C141, C142, C143, C154, C155, C156, C159	36	0.01 µF	CAP, CERM, 0.01 µF, 6.3 V, ± 10%, X7R, 0201	0201	GRM033R70J103KA01D	MuRata
C24, C25, C36, C37, C57, C58, C69, C70, C112, C113, C124, C125, C145, C146, C157, C158	16	0.047 µF	CAP, CERM, 0.047 µF, 6.3 V, ± 10%, X5R, 0201	0201	GRM033R60J473KE19D	MuRata
C30, C63, C118, C151	4	2.2 µF	CAP, CERM, 2.2 µF, 6.3 V,± 20%, X5R, 0201	0201	GRM033R60J225ME47D	MuRata
C39, C72, C81, C127, C160, C169, C315, C321	8	100 µF	CAP, CERM, 100 µF, 4 V, ± 20%, X6T, 1206	1206	GRM31CD80G107ME39L	MuRata

Table 6-1. DS160PT801X16EVM Bill of Materials (continued)

Designator	QTY	Value	Description	Package	Part Number	Manufacturer
C40, C73, C87, C96, C128, C161, C175, C184, C316	9	47 µF	CAP, CERM, 47 µF, 6.3 V, ± 20%, X7S, 1206	1206	C3216X7S0J476M160AC	TDK
C42, C43, C75, C76, C130, C131, C163, C164	8	1000 pF	CAP, CERM, 1000 pF, 50 V, ± 1%, C0G/NP0, 0402	0402	GRM1555C1H102FA01D	MuRata
C189, C190, C192, C193, C194, C196, C197, C199, C200, C217, C234, C235, C236, C237, C238, C239, C240, C241, C242, C243, C244, C277	22	1 pF	CAP, CERM, 1 pF, 50 V, ± 10%, C0G/NP0, 0402	0402	GJM1555C1H1R0BB01D	MuRata
C288, C290, C296, C297, C301, C308, C312, C323, C339	9	1 µF	CAP, CERM, 1 µF, 25 V, ± 10%, X5R, 0402	0402	GRM155R61E105KA12D	MuRata
C289, C295	2	220 pF	CAP, CERM, 220 pF, 50 V, ± 1%, C0G/NP0, 0603	0603	06035A221FAT2A	AVX
C291, C292	2	30 pF	CAP, CERM, 30 pF, 50 V, ± 5%, C0G/NP0, 0603	0603	06035A300JAT2A	AVX
C293	1	2200 pF	CAP, CERM, 2200 pF, 50 V, ± 10%, X7R, 0603	0603	C0603X222K5RACTU	Kemet
C294	1	0.47 µF	CAP, CERM, 0.47 µF, 10 V, +80/-20%, Y5V, 0603	0603	C0603C474Z8VACTU	Kemet
C298	1	2.2 µF	CAP, CERM, 2.2 µF, 16 V, ± 10%, X5R, 0805	0805	0805YD225KAT2A	AVX
C299, C333, C334, C335, C336	5	0.01 µF	CAP, CERM, 0.01 µF, 100 V,± 10%, X7R, 0603	0603	885012206114	Wurth Elektronik
C300	1	22 µF	CAP, CERM, 22 µF, 16 V, ± 20%, X5R, 0805	0805	EMK212BBJ226MG-T	Taiyo Yuden
C302, C327	2	100 µF	CAP, Tantalum Polymer, 100 µF, 20 V, ± 20%, 0.055 Ω, 7.3x4.3 mm SMD	7.3x4.3 mm	20TQC100MYF	Panasonic
C303, C304, C309, C310, C311, C326	6	22 µF	CAP, CERM, 22 µF, 25 V, ± 20%, X5R, 1206_190	1206_190	TMK316BBJ226ML-T	Taiyo Yuden
C305, C319, C325	3	4.7 µF	CAP, CERM, 4.7 µF, 25 V, ± 10%, X6S, 0603	0603	GRM188C81E475KE11D	MuRata
C306, C307, C324, C337	4	0.1 µF	CAP, CERM, 0.1 µF, 25 V, ± 20%, X7R, 0402	0402	TMK105B7104MV-FR	Taiyo Yuden
C313	1	1000 pF	CAP, CERM, 1000 pF, 25 V, ± 5%, X7R, 0402	0402	C0402C102J3RACTU	Kemet
C314, C320	2	220 µF	CAP, CERM, 220 µF, 4 V, ± 20%, X5R, 1206_190	1206_190	GRM31CR60G227ME11L	MuRata
C317	1	3.3 µF	CAP, CERM, 3.3 µF, 16 V, ± 10%, X5R, 1206	1206	C1206C335K4PACTU	Kemet
C318	1	0.47 µF	CAP, CERM, 0.47 µF, 25 V, ± 10%, X7R, 1206	1206	12063C474KAT2A	AVX
C332	1	0.47 µF	CAP, CERM, 0.47 µF, 25 V, ± 10%, X5R, 0805	0805	08053D474KAT2A	AVX
D1	1	Green	LED, Green, SMD	LED, GREEN, 0603	SML-LX0603GW-TR	Lumex
D2	1	7.5 V	Diode, Zener, 7.5 V, 500 mW, SOD-123	SOD-123	MMSZ5236B-7-F	Diodes Inc.
D3, D4, D5, D6	4	Green	LED, Green, SMD	2x1.4 mm	LG M67K-G1J2-24-Z	OSRAM
F1, F2	2		FUSE HLDR CARTRIDGE 125V 5A SMD	12x5.2 mm	0031.7701.11	Schurter
F3, F4	2		Fuse, 3 A, 63VAC/VDC, SMD	7.4x3.1 mm	3402.0014.11	Schurter

Table 6-1. DS160PT801X16EVM Bill of Materials (continued)

Designator	QTY	Value	Description	Package	Part Number	Manufacturer
FB1	1	60 Ω	Ferrite Bead, 60 Ω at 100 MHz, 0.8 A, 0603	0603	BK1608HS600-T	Taiyo Yuden
H1, H2	2		MACHINE SCREW PAN PHILLIPS 4-40	Machine Screw, 4-40, 1/4 inch	PMSSS 440 0025 PH	B&F Fastener Supply
J1, J2, J4, J15, J16, J18, J20, J22, J23, J45, J46, J47, J48, J49, J50, J53, J56, J59	18		Header, 2.54mm, 3x1, Gold, TH	Header, 2.54 mm, 3x1, TH	961103-6804-AR	3M
J5, J7, J8, J9, J10, J12, J13, J14, J28, J33	10		Header, 100mil, 3x2, Gold, TH	3x2 Header	TSW-103-07-G-D	Samtec
J6, J11	2		Header, 100mil, 4x2, Gold, TH	4x2 Header	TSW-104-07-G-D	Samtec
J17, J58	2		Header, 2.54 mm, 5x2, Gold, Black, TH	Header, 2.54 mm, 5x2, TH	TSW-105-07-F-D	Samtec
J21, J24, J25, J51	4		Header, 2.54 mm, 2x1, TH	Header, 2.54 mm, 2x1, TH	961102-6404-AR	3M
J36, J37, J39, J40, J41, J42, J43, J44, J52, J54, J62, J63	12		Plug, 50 Ω, Straight, SMT	SMA Plug, Straight, SMT	0853050232	Molex
J38	1		Receptacle, 1 mm, 82x2, Gold, SMT	Receptacle, 1 mm, 82x2, SMT	GWE82DHRN-T9410	Sullins Connector Solutions
J55	1		Connector, Receptacle, Mini-USB Type B, R/A, Top Mount SMT	USB Mini Type B	1734035-2	TE Connectivity
J57	1		Conn SATA PL 22 POS Solder RA SMD 22 Terminal 1 Port T/R	CONN_SMT_SATA	10101788-002CLF	Amphenol
L1, L2, L4, L6, L7	5	80 Ω	Ferrite Bead, 80 Ω at 100 MHz, 0.5 A, 0805	0805	742792062	Wurth Elektronik
L3, L5	2	33 Ω	Ferrite Bead, 33 Ω at 100 MHz, 4 A, 0805	0805	742792012	Wurth Elektronik
L8	1	600 nH	Inductor, Shielded, Composite, 600 nH, 17.7 A, 0.00411 Ω, AEC-Q200 Grade 1, SMD	5.3x31.x5.5 mm	XAL5030-601MEB	Coilcraft
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
MP1, MP2	2		HEATSINK 19X15MM DIAGONAL PLASTIC PUSH PIN	HTSNK_19MM97_19MM50	960-19-15-D-AB-0	Wakefield-Vette
MP3	1		PCI bracket	PCI_BRCKT_NPTH_2	9B90-0000A	Gompf Brackets, Inc.
Q1	1	50 V	MOSFET, N-CH, 50 V, .2 A, AEC-Q101, SOT-23	SOT-23	BSS138LT3G	ON Semiconductor
R3, R4, R5, R6, R7, R8, R9, R11, R13, R37, R38, R44, R45, R46, R49, R50, R54, R55, R56, R57, R59, R60, R61, R62, R96, R98, R100, R117, R119, R121, R122, R123, R124, R125, R127, R167, R168	37	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic

Table 6-1. DS160PT801X16EVM Bill of Materials (continued)

Designator	QTY	Value	Description	Package	Part Number	Manufacturer
R10	1	4.7k	RES, 4.7 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K70JNED	Vishay-Dale
R16, R101, R102, R103, R104, R105, R106, R107, R108, R109	10	49.9	RES, 49.9, 1%, 0.063 W, 0402	0402	RC0402FR-0749R9L	Yageo America
R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R152	13	10.0k	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040210K0FKED	Vishay-Dale
R33, R34, R35, R36	4	1.00k	RES, 1.00 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K00FKED	Vishay-Dale
R39, R40, R41, R42, R43, R53	6	20.0k	RES, 20.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040220K0FKED	Vishay-Dale
R51, R52, R113, R114	4	2.20k	RES, 2.20 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K20FKED	Vishay-Dale
R58, R63	2	0.1	RES, 0.1, 1%, 0.25 W, 0805	0805	CRM0805-FX-R100ELF	Bourns
R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85	22	43	RES, 43, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040243R0JNED	Vishay-Dale
R86, R87, R88, R89, R90, R92, R94, R97	8	33	RES, 33.0, 1%, 0.062 W, 0402	0402	RC0402FR-0733RL	Yageo America
R110, R111	2	33	RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040233R0JNED	Vishay-Dale
R112	1	1.5k	RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K50JNED	Vishay-Dale
R115, R128	2	33k	RES, 33 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040233K0JNED	Vishay-Dale
R116	1	1.2Meg	RES, 1.2 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031M20JNEA	Vishay-Dale
R126	1	200	RES, 200, 1%, 0.1 W, 0603	0603	RC0603FR-07200RL	Yageo
R129	1	1	RES, 1.00, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021R00FKED	Vishay-Dale
R130, R132, R144	3	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc
R133, R134, R135, R136	4	100k	RES, 100 k, 1%, 0.0625 W, 0402	0402	RC0402FR-07100KL	Yageo America
R137	1	1	RES, 1.0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW08051R00JNEA	Vishay-Dale
R140, R142	2	22.1k	RES, 22.1 k, 1%, 0.1 W, 0603	0603	RC0603FR-0722K1L	Yageo
R143, R157	2	42.2k	RES, 42.2 k, 1%, 0.1 W, 0603	0603	RC0603FR-0742K2L	Yageo
R145	1	30.1k	RES, 30.1 k, 1%, 0.1 W, 0603	0603	RC0603FR-0730K1L	Yageo
R146	1	165k	RES, 165 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402165KFKED	Vishay-Dale

Table 6-1. DS160PT801X16EVM Bill of Materials (continued)

Designator	QTY	Value	Description	Package	Part Number	Manufacturer
R147	1	133k	RES, 133 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402133KFKED	Vishay-Dale
R148	1	75.0k	RES, 75.0 k, 1%, 0.05 W, 0201	0201	RC0201FR-0775KL	Yageo America
R149, R153	2	110k	RES, 110 k, 1%, 0.05 W, 0201	0201	RC0201FR-07110KL	Yageo America
R150	1	90.9k	RES, 90.9 k, 1%, 0.05 W, 0201	0201	RC0201FR-0790K9L	Yageo America
R151, R166	2	10.0k	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	AC0402FR-0710KL	Yageo America
R154	1	47k	RES, 47 k, 5%, 0.05 W, 0201	0201	RC0201JR-0747KL	Yageo America
R155, R156	2	1.87k	RES, 1.87 k, 1%, 0.1 W, 0603	0603	RC0603FR-071K87L	Yageo
R158	1	220k	RES, 220 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603220KJNEA	Vishay-Dale
R159	1	0.01	RES, 0.01, 1%, 1 W, 0612	0612	PRL1632-R010-F-T1	Susumu Co Ltd
R160, R161	2	1.50k	RES, 1.50 k, 1%, 0.1 W, 0603	0603	RC0603FR-071K5L	Yageo
R162, R163, R164, R165	4	330	RES, 330, 1%, 0.1 W, 0603	0603	RC0603FR-07330RL	Yageo
S1	1		Switch, SPST-NO, Off-Mom, 0.05 A, 12 VDC, SMD	6x6 mm	PTS645SM43SMTR92 LFS	C&K Components
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J15, SH-J16, SH-J17, SH-J18, SH-J19, SH-J20, SH-J21, SH-J22, SH-J23	22	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
U1	1		CDCE6214WRGERQ1, RGE0024P (VQFN-24)	RGE0024P	CDCE6214WRGERQ1	Texas Instruments
U2, U3	2		8-Lane (16-Channel) PCI-Express Gen-4 Retimer	FCBGA332	DS160PT801ACB	Texas Instruments
U4	1		Two-wire Serial Electrically Erasable and Programmable Read-only Memory 16K (2048 x 8), SOIC-8	SOIC-8	AT24C16C-SSHM-B	Atmel
U5, U6, U8, U9	4		Low- or High-Side, Bidirectional, Zero-Drift, Current-Shunt Monitor with Integrated Precision Low Inductive Shunt Resistor, PW0020A (TSSOP-20)	PW0020A	INA253A3IPWR	Texas Instruments
U7, U10, U18	3		26-V, Bi-Directional, Zero-Drift, High Accuracy, Low-/High-Side, Voltage Out Current Shunt Monitor, DCK0006A (SOT-SC70-6)	DCK0006A	INA210AIDCKR	Texas Instruments
U11	1		LMK00334 4-Output PCIe Gen1/Gen2/Gen3/ Gen4 Clock Buffer/Level Translator, RTV0032A (WQFN-32)	RTV0032A	LMK00334RTVR	Texas Instruments
U12	1		25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	PN0080A	MSP430F5529IPN	Texas Instruments

Table 6-1. DS160PT801X16EVM Bill of Materials (continued)

Designator	QTY	Value	Description	Package	Part Number	Manufacturer
U13	1		4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	DRY0006A	TPD4E004DRYR	Texas Instruments
U14	1		500 mA, Adjustable, Low Quiescent Current, Low-Noise, High-PSRR, Single-Output LDO Regulator, DRB0008A (VSON-8)	DRB0008A	TPS73533DRBR	Texas Instruments
U15	1		1.5-V to 16-V VIN, 4.5-V to 22-V VDD, 25-A SWIFT Synchronous Step-Down Converter with Full Differential Sense, RVF0040A (LQFN-CLIP-40)	RVF0040A	TPS548B22RVFR	Texas Instruments
U16, U17	2		1-A, High-Accuracy, Low-Noise LDO Voltage Regulator, DSK0010A (WSON-10)	DSK0010A	TPS7A9101DSKR	Texas Instruments
U19	1		Quadruple Bus Buffer Gate With 3-State Outputs, PW0014A, LARGE T&R	PW0014A	SN74LVC125APWRG3	Texas Instruments
Y1	1		Crystal, 25 MHz, 8 pF, SMD	3.2x0.75x2.5 mm	NX3225GA-25.000M-STD-CRG-2	NDK
Y2	1		Crystal, 24 MHz, 18 pF, SMD	ABM3	ABM3-24.000MHZ-D2Y-T	Abracon Corporation
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J3, J26, J27, J29, J30, J31, J32, J34, J35, J60	0		Header, 100mil, 2x1, Gold, SMD	SMD, 2-Leads, Body 100x200mil, Pitch 100mil	HW-02-15-T-S-340-SM	Samtec
R1, R2, R12, R47, R48, R95, R99, R118, R120	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic
R14, R15, R17, R18, R19, R20	0	49.9	RES, 49.9, 1%, 0.063 W, 0402	0402	RC0402FR-0749R9L	Yageo America
R91, R93	0	100	RES, 100, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402100RFKED	Vishay-Dale
R131, R138, R139, R141	0	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2020) to Revision A (July 2022)	Page
• First public release of user's guide	3

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。
上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿 6 丁目 2 4 番 1 号
西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265