

# DS125BR111EVM User's Guide SMA Evaluation Kit

## User's Guide



Literature Number: SNLU168A  
August 2014—Revised August 2014

## **DS125BR111EVM User's Guide** **SMA Evaluation Kit**

The DS125BR111EVM – SMA evaluation kit provides a complete high bandwidth platform to evaluate the 10GbE, PCIe, and SAS/SATA signal conditioning features of the Texas Instruments DS125BR111 repeater/redriver. The DS125BR111EVM can be used for standard compliance testing, performance evaluation, and initial system prototyping. The SMA edge launch connectors used for the DS125BR111EVM will interface to multiple system connector types via commercially available breakout cables, adaptors, and boards (not included). This flexible connectivity enables integrated system level testing between TI repeaters and 3rd party ASIC/FPGA host boards.

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## 1 Features

- Two Channel Repeater up to 12 Gbps Rate
  - DS125BR111: 1x Bidirectional Lane
- Low 65mW/channel Power Consumption, with Option to Power Down Unused Channels
- Advanced Signal Conditioning Features
  - Linear Equalization (up to 10 dB @ 6 GHz)
  - Linear output drive
  - Output voltage range over 1200 mV
- Fully Programmable via Pin Selection or SMBus Interface
- Selectable Single Supply Operation
- 5 kV HBM ESD Rating
- 3.3 V LVCMOS Input Tolerant for SMBus Interface
- Flow-Thru Pinout Package: 24-Pin QFN (4 mm x 4 mm)
- Industrial –40 to 85°C Operating Temperature Range

## 2 Applications

- High-Speed Cables and Backplanes in Communication Systems
- PCIe, SAS I/II/III, SATA 3/6 Gbps (with OOB detection) and many others

## 3 Demo Kit Contents

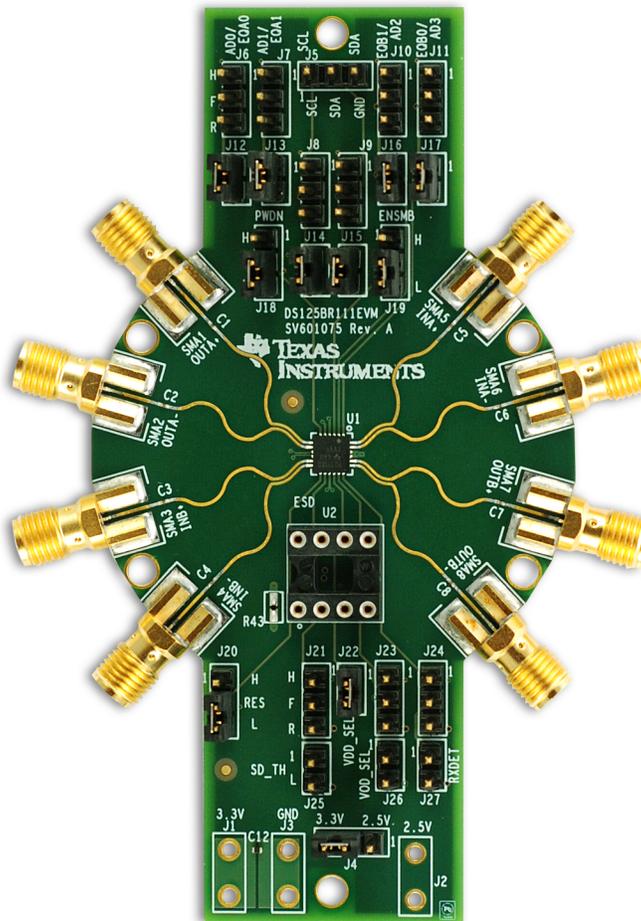
- DS125BR111EVM Board

## 4 Ordering Information

**Table 1. DS125BR111EVM Ordering Information**

DEVICE	QUANTITY
DS125BR111RTWR	1000
DS125BR111RTWT	250
<b>SMA Evaluation Kit: DS125BR111EVM</b>	

## 5 Evaluation Board



**Figure 1. DS125BR111EVM Evaluation Board**

## 6 Setup

The DS125BR111EVM – SMA evaluation kit can be used in three different modes:

1. **Pin Control** (provides access to selected signal integrity settings)
2. **SMBus Mode** (full access to signal integrity and control settings)
3. **EEPROM Mode** (full access to signal integrity and control settings)

The EEPROM mode is a convenient method of programming one or more DS125BRxxx devices on system power-up when a SMBus master (microcontroller or similar) is unavailable in the design. It is recommended to use a 1 MHz capable EEPROM. The EEPROM must be 8-kbits or smaller.

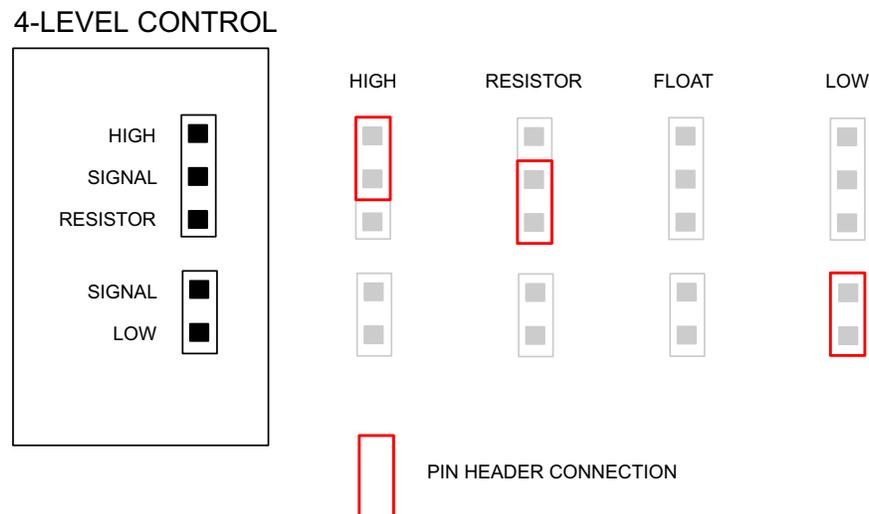
## 6.1 DS125BR111 Pin Control

Uses the external control pins on the DS125BR111 to configure the signal integrity and control settings of the device. Due to the limited number of control pins, a limited bandwidth 4-level input scheme has been implemented across the control pin interface. This allows for improved EQ and VOD control with fewer physical pins.

The 4 levels are defined as:

1. **Low:** 1 K $\Omega$  to GND
2. **Resistor:** 20 K $\Omega$  to GND
3. **Float:** No External Connection
4. **High:** 1 K $\Omega$  to VDD

The EVM interfaces to this 4-level IO using the setup below. Only one shunt connection is required to access any of the 4 levels. This methodology minimizes the risk of improper connections that could damage the board or board power supply.



The DS125BR111EVM is quickly setup for use in pin control configuration. Jumpers listed below should be installed on the EVM for pin control.

1. J4 – 3.3 V operation: Use the J1 and J3 connectors to supply 3.3 V power to the EVM. The EVM power connections are designed to accommodate 1287-ST quick connect tabs or directly soldered to power leads for connection to a lab power supply.
2. J18 – PWDN = LOW: Device is enabled.
3. J19 – ENSMB = LOW: PIN CONTROL configuration mode.
4. J22 – VDD\_SEL = LOW: Uses DS125BR111 internal regulator to convert 3.3 V supply to proper internal supply level of 2.5 V. Note: The 2.5 V level may be observed on the device VDD pins or the J2 connector.
5. VOD\_SEL = 1: Recommended output amplitude settings for CH A and CH B in SAS/SATA and PCIe applications.

## 6.2 SMBus Mode

The SMBus can also be used to control the DS125BR111 devices. This method has the advantage of independent control and finer signal conditioning granularity.

**Table 2. Typical DS125BR111 Register Writes**

Register Address	Function	Description
Register 0x0F	CHA EQ	Write EQ setting 03'h
Register 0x11	CHA VOD_DB	Write VOD_DB setting for bits [2:0] = 000'b
Register 0x23	CHA VOD	Write VOD setting for bits [4:2] = 111'b
Register 0x06	CRC DIS	Write bit [3] = 1'b send register updates directly to channel without any CRC check.

## 6.3 EEPROM Mode

A serial EEPROM may also be used to configure one or more DS125BR111 devices. This configuration mode is accessed by setting the ENSMB 4-level input to FLOAT. For additional information please see the device datasheet.

## 7 Expected Results

This evaluation board has been designed to evaluate the cable and/or FR4 signal conditioning performance of the DS125BR111. Adding additional cables or adaptor boards into the signal path will have some impact on the optimal settings, but keeping the adaptor boards small and using short high-quality SMA cables will minimize this effect.

### 7.1 Performance

When used in a PCIe or SAS system, it is generally expected that the DS125BR111 will be receiving a signal with embedded TX FIR information. The DS125BR111 works to extend the reach possible by adding active linear equalization to the channel, boosting attenuated signals so that they can be more easily recovered at the SAS-3 Rx. The outputs are specially designed to be transparent to TX FIR signaling passing this information critical for optimal link training to the SAS-3 Rx. The typical device settings used in most SAS-3 environments are EQ = Level 4, VOD\_DB = 0 and VOD\_SEL = 1 in Pin mode or EQ = 03'h, VOD = 111'b, and VOD\_DB = 000'b in SMBus mode.

SETUP1: PRBS7 Generator (no TX FIR) → 10" FR4 → DS125BR111EVM → Scope

DS125BR111 Settings

1. VOD\_SEL = 1
2. VOD\_DB = 0
3. EQ0 = 1

Additional documentation and device performance is available in the device datasheet.

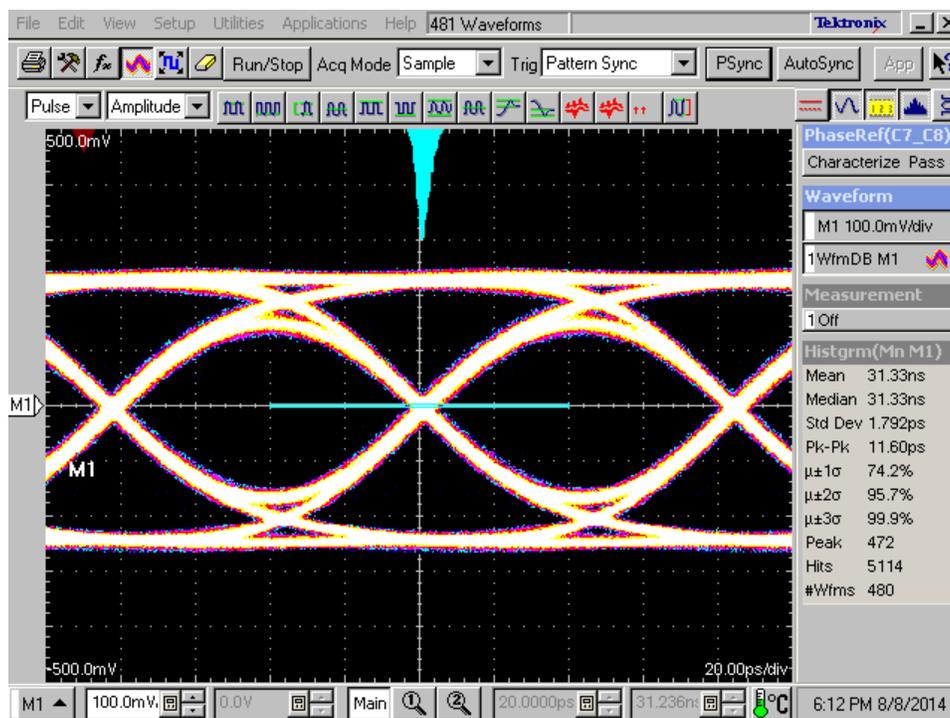


Figure 3. 12 Gbps Eye Diagram at SCOPE in SETUP1

8 Schematic

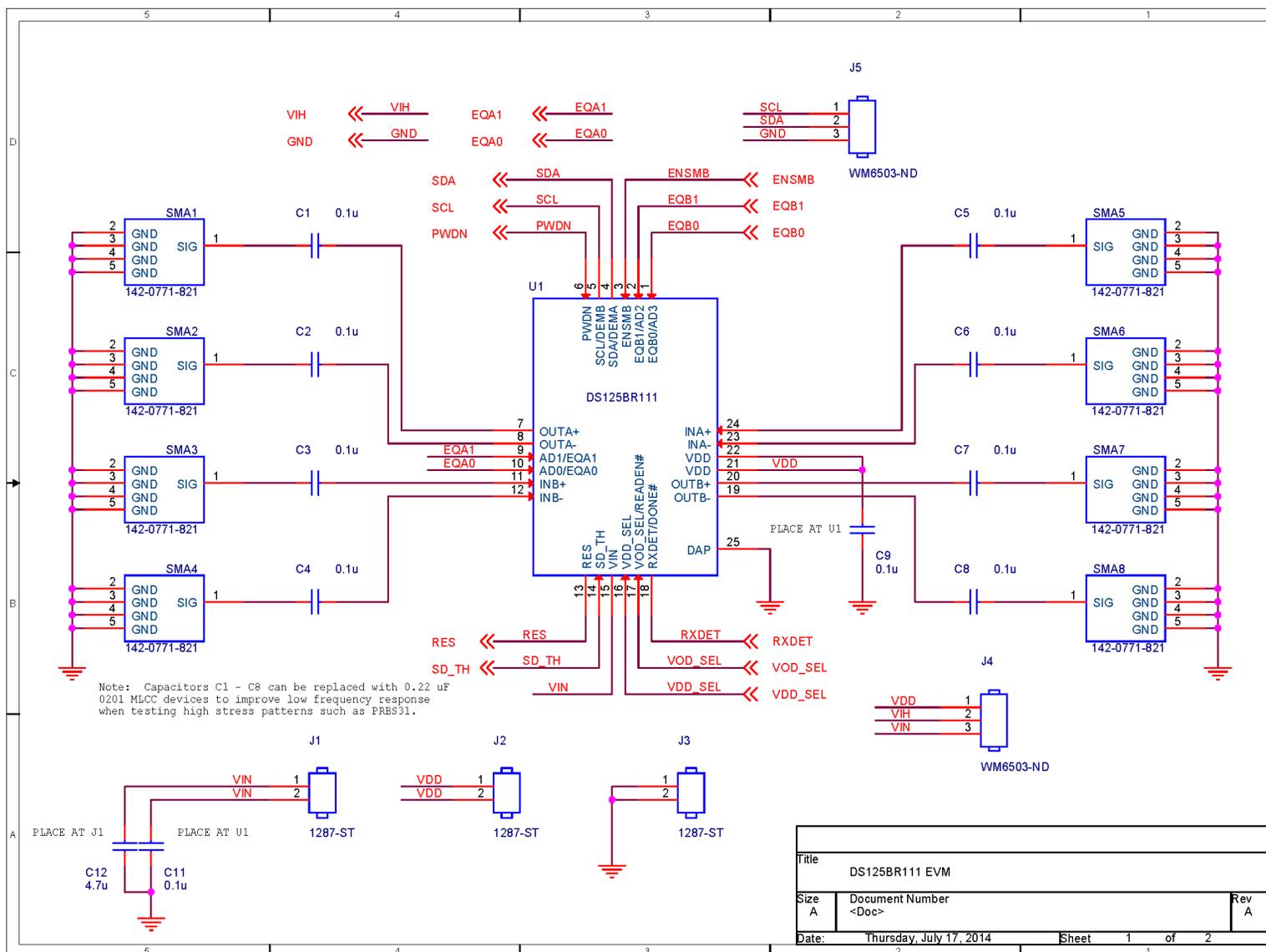


Figure 4. DS125BR111EVM Schematic

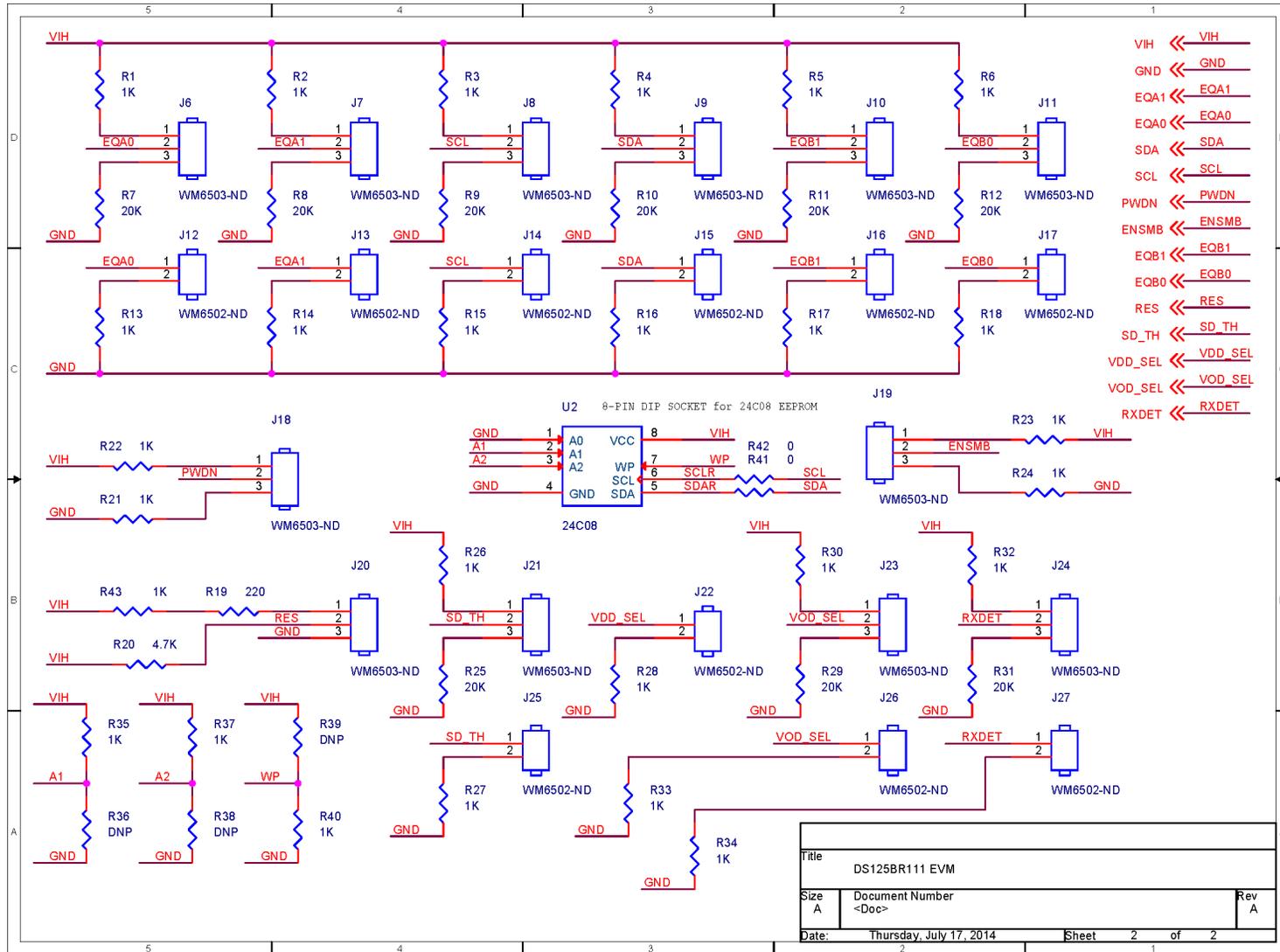


Figure 5. DS125BR111EVM Schematic

**9 Bill of Materials**

Item	Quantity	Reference	Digikey PN	Manufacture PN	Descriptions
1	1	PCB		SV601075	DS125BR111EVM PCB ASSY
2	10	C1, C2, C3, C4, C5, C6, C7, C8, C9, C11	445-1796-1-ND	C0603X5R0J104K	CAP CERAMIC .1UF 6.3 V X5R 0201
3	1	C12	1276-1482-1-ND	CL05A475MP5NRNC	CAP CER 4.7UF 10V 20% X5R 0402
4	10	SMA1, SMA2, SMA3, SMA4, SMA5, SMA6, SMA7, SMA8, SMA9, SMA10, SMA11, SMA12	J807-ND	142-0771-821	CONN JACK SMA 50 Ω PC MOUNT
5	14	J4, J5, J6, J7, J8, J9, J10, J11, J18, J19, J20, J21, J23, J24	WM6503-ND	22-28-4033	CONN HEADER 3POS .100 VERT GOLD
6	10	J12, J13, J14, J15, J16, J17, J22, J25, J26, J27	WM6502-ND	22-28-4023	CONN HEADER 2POS .100 VERT GOLD
7	27	R1, R2, R3, R4, R5, R6, R13, R14, R15, R16, R17, R18, R21, R22, R23, R24, R26, R27, R28, R30, R32, R33, R34, R35, R37, R40, R43	P1.0KJCT-ND	ERJ-2GEJ102X	RES 1.0K Ω 1/10W 5% 0402 SMD
8	9	R7,R8,R9, R10,R11,R12, R25, R29,R31	P20.0KLCT-ND	ERJ-2RKF2002X	RES 20.0K Ω 1/10W 1% 0402 SMD
9	1	R19	P220JCT-ND	ERJ-2GEJ221X	RES 220 Ω 1/10W 5% 0402 SMD
10	1	R20	P4.7KJCT-ND	ERJ-2GEJ472X	RES 4.7K Ω 1/10W 5% 0402 SMD
11	1	R41, R42	P0.0JCT-ND	ERJ-2GE0R00X	RES 0.0 Ω 1/10W 5% 0402 SMD
12	1	U1		DS125BR111RTW	IC REPEATER 2CH 24-QFN (4x4mm)
13	1	U2	ED90197-ND	115-43-308-41- 001000	IC SOCKET 8PIN DIP
14	12	J30, J31, J32, J33 J34, J35, J36, J37, J38, J39, J40, J41	3M9580-ND	969102-0000-DA	SHUNT JUMPER .1" BLACK GOLD
15	3	J1, J2, J3	1287-STK-ND	1287-ST	Connector TAB 0.250 Solder
16	3	R36, R38, R39	DNP	DNP	DNP

## Revision History

### Changes from Original (August 2014) to A Revision

**Page**

- 
- Changed EVM Photo..... [4](#)
- 

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user's authority to operate the equipment.

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##### **FCC Interference Statement for Class B EVM devices**

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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#### **For EVMs Annotated as IC – INDUSTRY CANADA Compliant:**

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Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

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Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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