Application Note

Implementing Pin Compatible Ethernet Redrivers and Retimers

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ABSTRACT

TI has a variety of Ethernet redriver and retimer devices spanning different channels counts and signal conditioning capabilities. Several of these devices share pin compatible packages but have different signal conditioning capabilities. In some cases, this can be unclear what level of signal conditioning is required for an application. This application note discusses TI Ethernet signal conditioning devices with pin compatible packages and design considerations that can be made to allow a socket to support multiple devices with different signal conditioning capabilities.

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1 Introduction

Signal conditioning devices can be broken into two distinct categories: retimers and redrivers. Retimers are more advanced signal conditioning devices that contain a clock and data recovery functional block. Ths enables retimers to "reset" the jitter a signal has and transmit a clean signal. The clock recovery block also enables more digital signal equalization on retimers, such as DFE and FIR filters.

Redrivers are more simple signal conditioning devices that are largely analog. Redrivers are capable of equalizing jitter due to ISI using CTLE.

When selecting signal conditioning for a system, conditioning is not immediately clear whether a redriver or retimer is required to meet performance requirements. TI has several pin to pin redrivers and retimers that enable system designers to test both a redriver and retimer in the same socket to determine which device is a good choice. This application note details differences between pin compatible devices and design considerations when developing a common socket for both redriver and retimer devices.

2 Codesign: 25GbE 4-Channel Retimer or Redriver with Crosspoint

TI has one 4-channel retimer and one 4-channel redriver which support 25G Ethernet. These devices, DS250DF410 and DS560MB410 respectively, both use a 6mm × 6mm, 101-pin BGA package and are nearly pin-to-pin compatible. A single board codesign can implement either device, allowing designers to perform system-level testing before determining if the retimer or redriver is better designed for a particular application.

Table 2-1 shows a comparison of features between DS250DF410 and DS560MB410.

Table 2-1. DS250DF410 and DS560MB410 Feature Comparison

Type	DS250DF410	DS560MB410
Equalization capability	35dB	18dB
Receiver equalization	CTLE and DFE	CTLE
Transmitter equalization	3-tap FIR filter	None
Signal chain linearity	Nonlinear	Linear
Crosspoint	2x2 crosspoint	2x2 crosspoint
Crosspoint control	Register	Register or MUX pins
Calibration clock	25MHz clock required	Not required, can buffer 25MHz clock
Supply voltage	2.5V	2.5V
Maximum current	665mA	364mA

2.1 DS250DF410 Retimer Overview

The DS250DF410 retimer is a 4 channel retimer device that can lock to rates from 20.2752Gbps to 25.8Gbps and supported subrates. This device can equalize channels with up to 35dB insertion loss at 12.89GHz using a combination of CTLE and DFE. The DS250DF410 also has a 3-tap FIR filter which allows for pre- and post-cursor equalization.

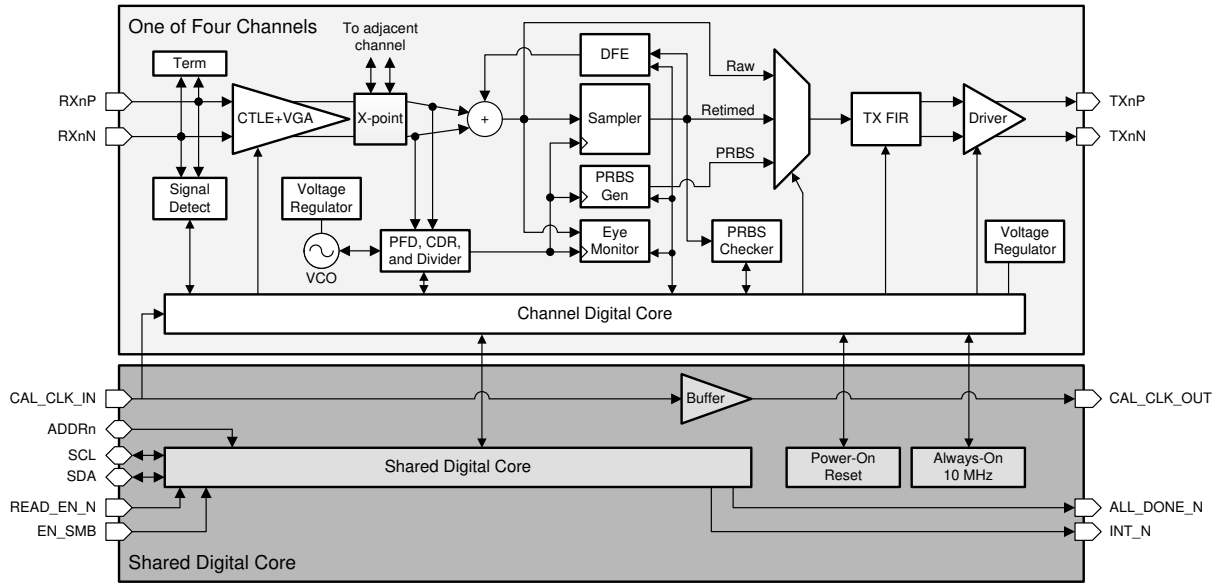

Figure 2-1. DS250DF410 Functional Block Diagram

Figure 2-2. DS250DF410 Pin Configuration

2.2 DS560MB410 Redriver Overview

The DS560MB410 redriver is a 4 channel linear redriver device supporting up to 32GBd NRZ or 28GBd PAM4. This device provides reach extension of up to 18dB beyond normal ASIC to ASIC capability at 13.28GHz through the receiver CTLE.

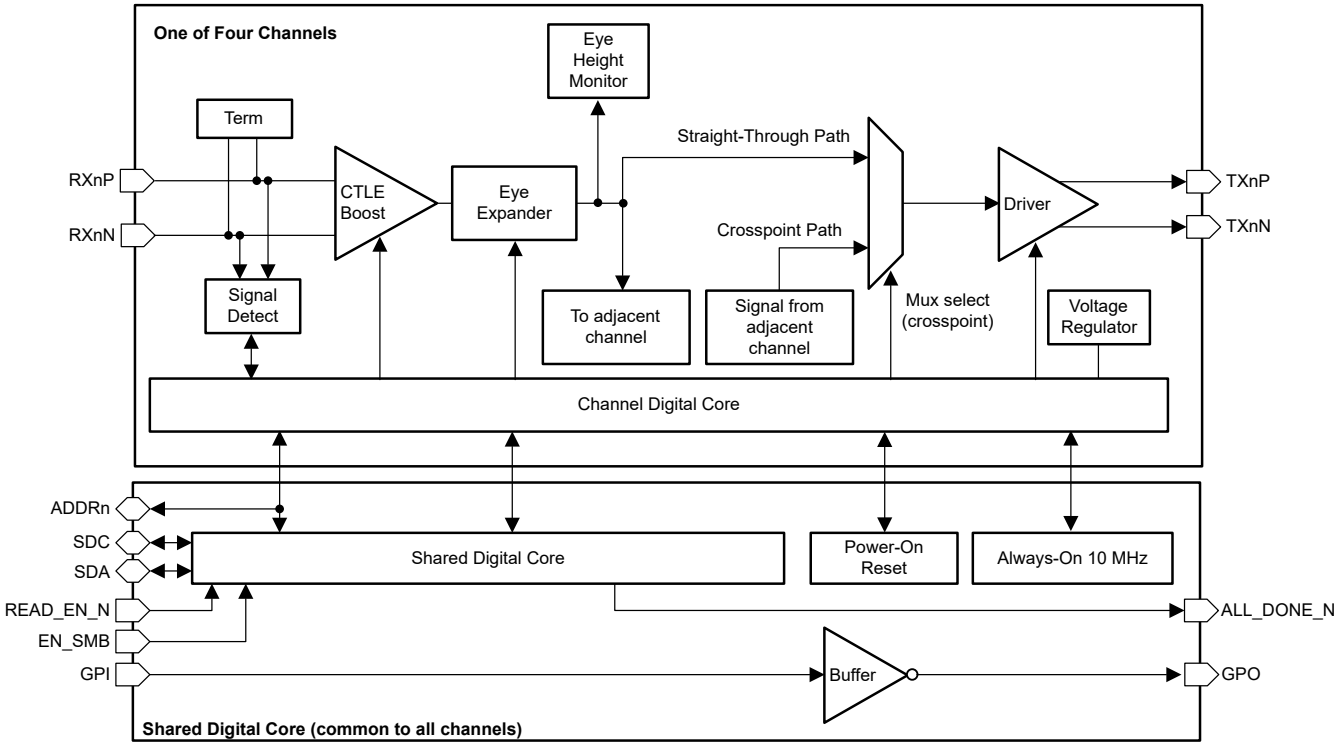

Figure 2-3. DS560MB410 Functional Block Diagram

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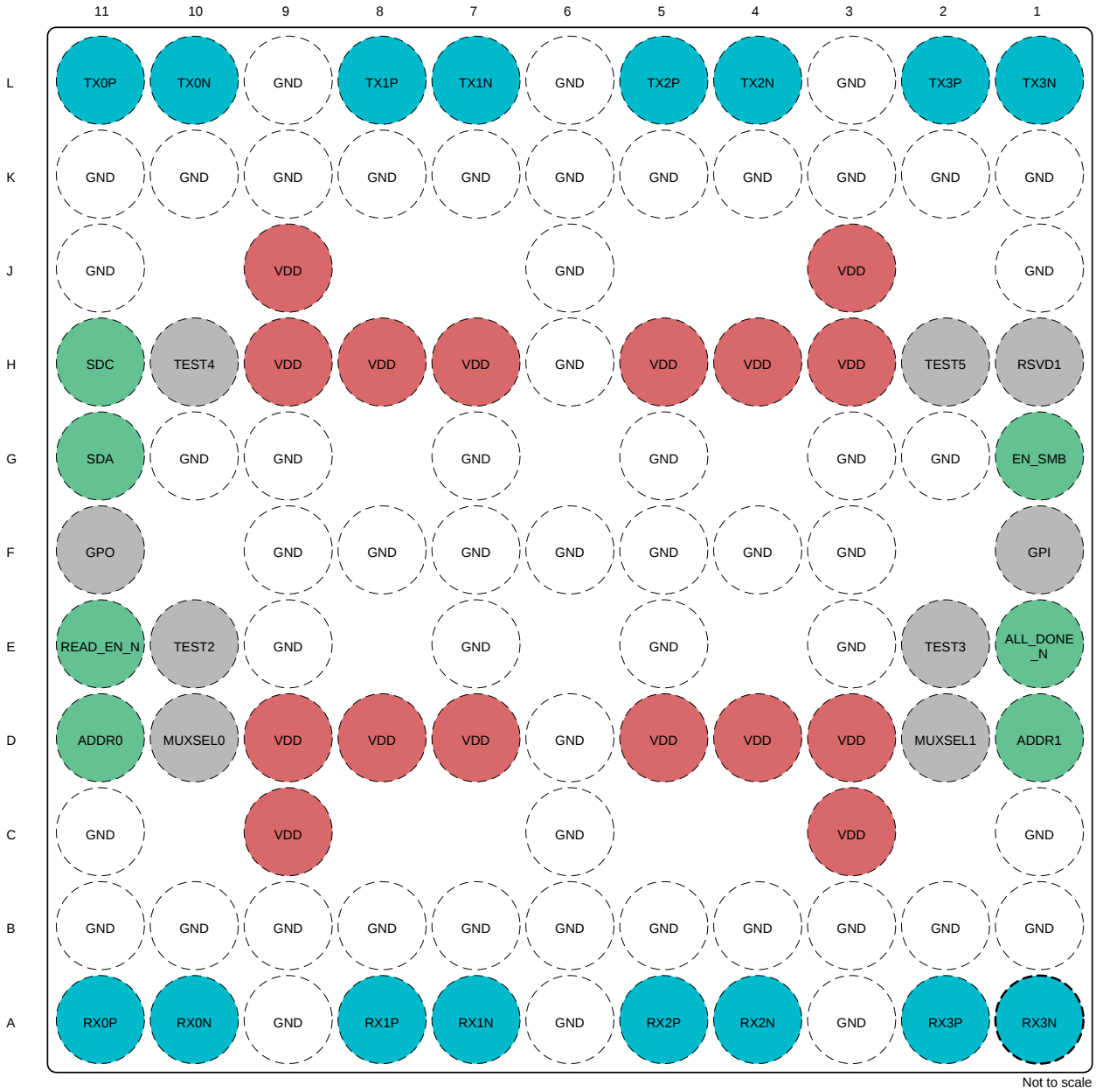

Figure 2-4. DS560MB410 Pin Configuration

2.3 Pin Comparison Table

Table 2-2 compares pin functionality of DS250DF410 retimer and DS560MB410 redriver and lists if any design provisions are necessary to support each device with the same codesign.

Table 2-2. 4-Channel Retimer or Redriver Pin Comparison Table

Pin Number	DS250DF410 Pin Name	DS560MB410 Pin Name	Provision Needed?	Details
A10, A11, A7, A8, A4, A5, A1, A2	RXnP/N	RXnP/N	No	High-speed inputs require AC coupling.
L10, L11, L7, L8, L4, L5, L1, L2	TXnP/N	TXnP/N	No	High-speed outputs require AC coupling.
F1	CAL_CLK_IN	GPI	Optional	**DS250DF410:** Requires a 25MHz calibration clock input. **DS560MB410:** Can optionally buffer an input signal up to 25MHz.
F11	CAL_CLK_OUT	GPO	Optional	**DS250DF410:** 2.5V buffered replica of CAL_CLK_IN. **DS560MB410:** Inverted buffer output from GPI.
D11, D1	ADDR0/1	ADDR0/1	No	4-level straps to configure SMBus Address.
G1	EN_SMB	EN_SMB	No	4-level strap to select SMBus target mode or controller mode.
G11, H11	SDA/SDC	SDA/SDC	No	SMBus data and clock I/Os. Require 2-5kΩ pull-up resistors.
E1	ALL_DONE_N	ALL_DONE_N	No	EEPROM load status when using SMBus controller mode.
E11	READ_EN_N	READ_EN_N	No	**SMBus target mode:** Pull high or leave floating for normal operation. **SMBus controller mode:** Pull low to initiate EEPROM load.
H1	INT_N	RSVD1	Yes	**DS250DF410:** Interrupt open-drain output. Requires 2-5kΩ pull-up resistor. **DS560MB410:** Reserved. Can be left floating or pulled low.
D10, D2	TEST0/1	MUXSEL0/1	Optional	**DS250DF410:** Reserved test pins. Can be left floating, tied to GND, or tied to 2.5V. **DS560MB410:** Mux select control input. Can be left floating or tied to GND if unused.
E10, E2, H10, H2	TEST2-5	TEST2-5	No	Reserved test pins. Can be left floating, tied to GND, or tied to 2.5V.

Table 2-2. 4-Channel Retimer or Redriver Pin Comparison Table (continued)

Pin Number	DS250DF410 Pin Name	DS560MB410 Pin Name	Provision Needed?	Details
A3, A6, A9, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, C1, C6, C11, D6, E3, E5, E7, E9, F3, F4, F5, F6, F7, F8, F9, G2, G3, G5, G7, G9, G10, H6, J1, J6, J11, K1, K2, K3, K4, K5, K6, K7, K8, K9, K10, K11, L3, L6, L9	GND	GND	No	Ground reference.
C3, C9, D3, D4, D5, D7, D8, D9, H3, H4, H5, H7, H8, H9, J3, J9	VDD	VDD	No	2.5V power supply. TI recommends connecting at least 6 decoupling capacitors as close to the device as possible.

2.4 Codesign Schematic Example

Figure 2-5 and Figure 2-6 show schematic diagrams for an example codesign which can be used with DS250DF410 retimer and DS560MB410 redriver. A few component replacements are necessary to use each device with this codesign.

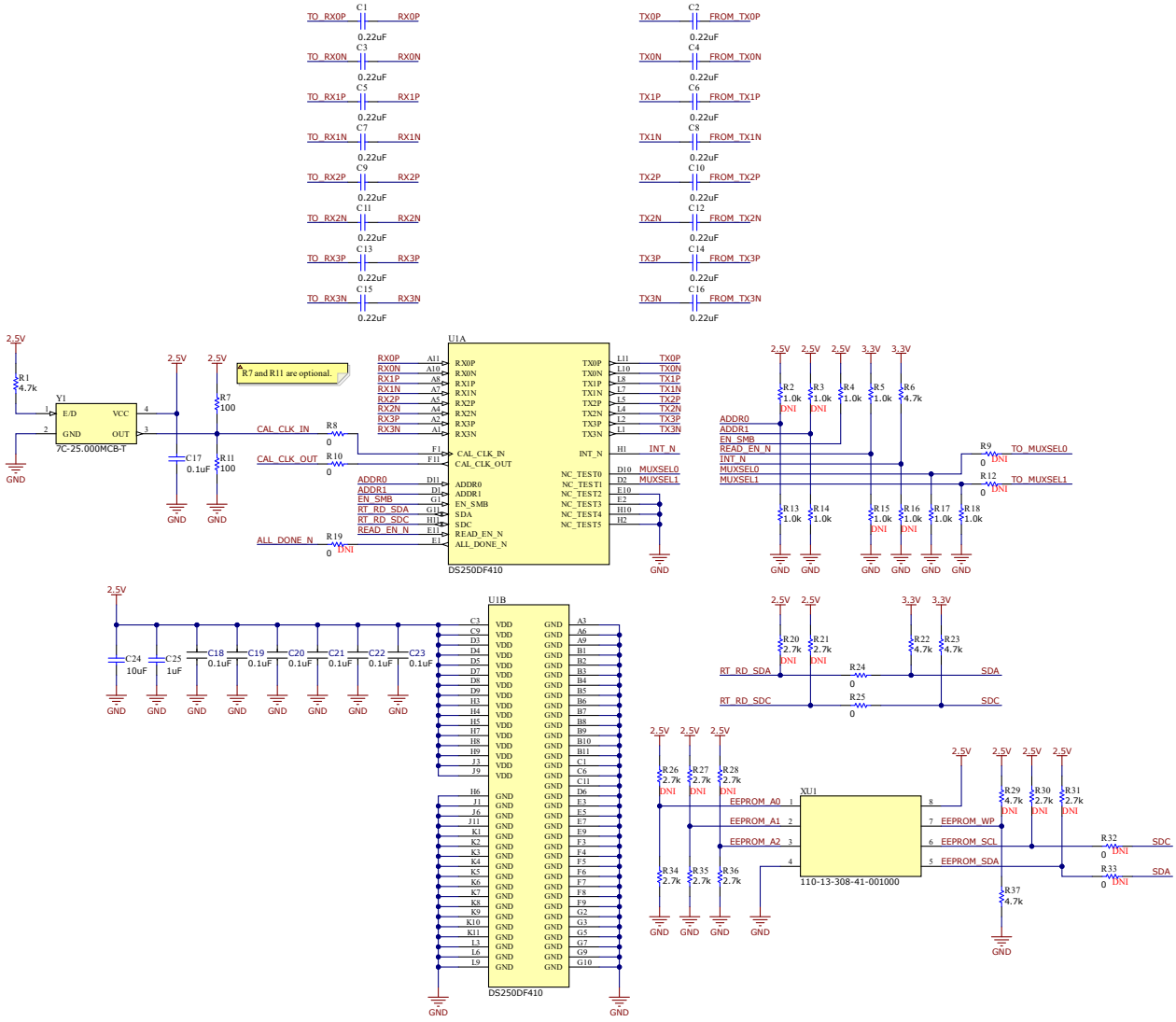

Figure 2-5. DS250DF410 Schematic Example

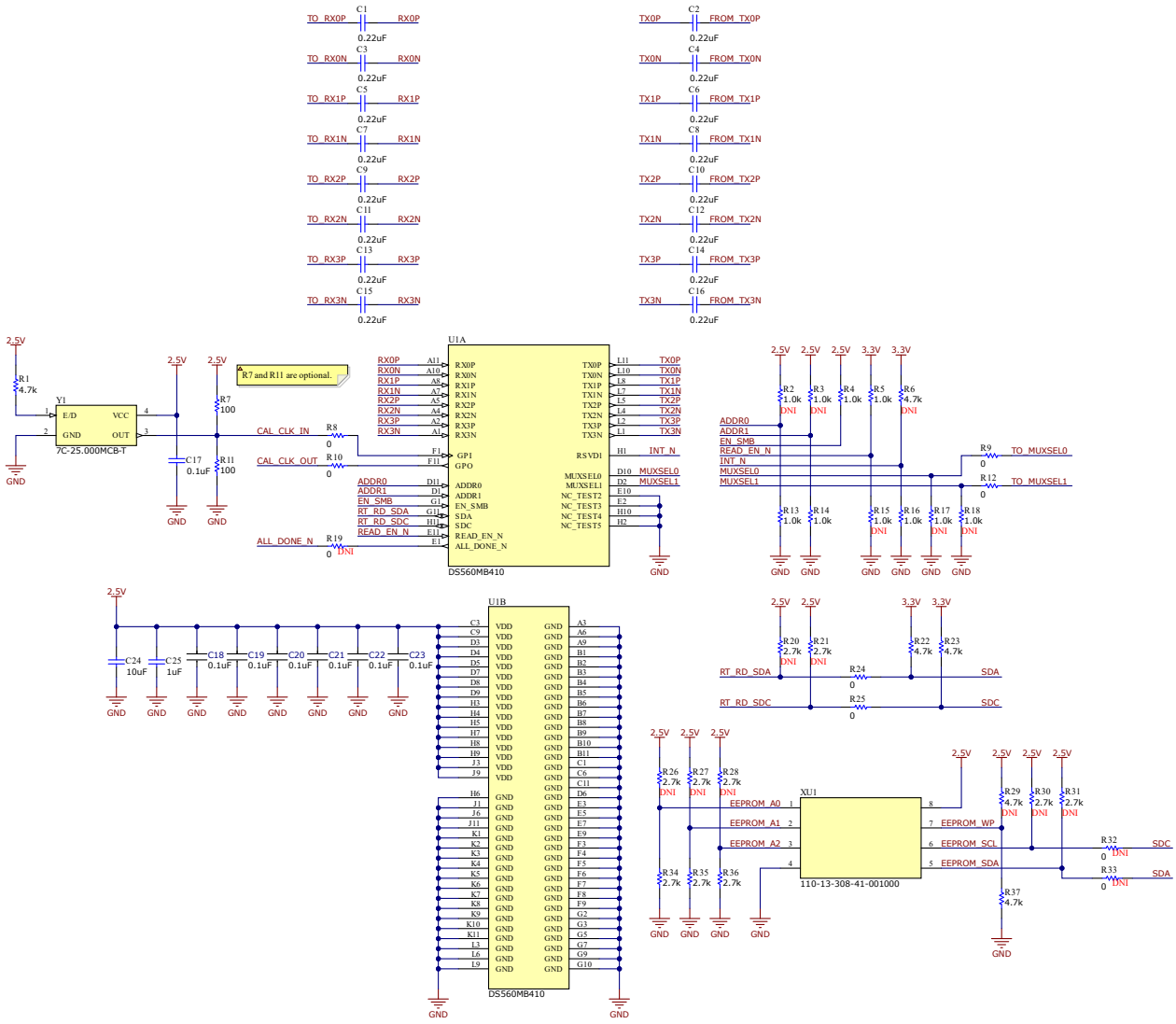

Figure 2-6. DS560MB410 Schematic Example

2.5 Notable Codesign Elements

2.5.1 Calibration Clock

DS250DF410 requires a 25MHz (±100PPM) 2.5V single-ended clock from external oscillator to be connected to pin F1 (CAL_CLK_IN). A 25MHz oscillator Y1 is included in the codesign schematic example. Pin F11 (CAL_CLK_OUT) outputs a 2.5V buffered replica of the calibration clock input for connecting multiple devices in a daisy-chained fashion.

DS560MB410 does not require an external calibration clock. Pin F1 (GPI) operates as a 2.5V LVCMOS inverted buffer input supporting general purpose LVCMOS signals up to 25MHz. Pin F11 (GPO) operates as the inverted buffer output from the GPI pin.

There are two options regarding calibration clock connections to DS560MB410 within this codesign example.

1. Depopulate resistors R8 and R10 to disconnect the calibration clock input and output signals from the device.
2. Keep R8 and R10 populated to buffer the 25MHz reference clock signal. This option is most useful if the reference clock is connected to multiple devices in a daisy-chained fashion. Note that the buffer output is inverted. This can possibly impact other connected devices.

2.5.2 SMBus Address

Pins D11 (ADDR0) and D1 (ADDR1) are connected such that the 8-bit SMBus address for both DS250DF410 and DS560MB410 is 0x30 by default. Strap resistors R2, R3, R13, and R14 can be populated/depopulated with different values to select a different SMBus address. The four defined strap options are:

- 0: 1kΩ to GND
- R: 20kΩ to GND
- F: Float
- 1: 1kΩ to VDD

Table 2-3. SMBus Address Map

7-BIT TARGET ADDRESS	8-BIT WRITE ADDRESS	REQUIRED ADDRESS PIN STRAP VALUE	
		ADDR1	ADDR0
0x18	0x30	0	0
0x19	0x32	0	R
0x1A	0x34	0	F
0x1B	0x36	0	1
0x1C	0x38	R	0
0x1D	0x3A	R	R
0x1E	0x3C	R	F
0x1F	0x3E	R	1
0x20	0x40	F	0
0x21	0x42	F	R
0x22	0x44	F	F
0x23	0x46	F	1
0x24	0x48	1	0
0x25	0x4A	1	R
0x26	0x4C	1	F
0x27	0x4E	1	1

2.5.3 SMBus Controller Mode

Pin G1 (EN_SMB) is connected such that SMBus Target mode is selected for both DS250DF410 and DS560MB410 by default. In SMBus Target mode, a controller accesses and modifies the retimer's or redriver's register configuration via the SMBus interface. In SMBus Controller mode, the retimer or redriver attempts to self-configure by reading the device settings stored in an external EEPROM.

DS250DF410 and DS560MB410 can be reconfigured in SMBus Controller mode within this codesign example. The following design modifications need to be made.

1. Depopulate R4 to select SMBus Controller mode on the EN_SMB pin.
2. Depopulate R5 and populate R15 with a 1kΩ resistor. This pulls the READ_EN_N pin low to initiate EEPROM load.
3. Populate R19 with a 0Ω resistor to connect the ALL_DONE_N pin output. If multiple devices share a single EEPROM, then connect the ALL_DONE_N output of the first device to the READ_EN_N input of the next device to prevent multiple devices attempting to read the EEPROM at the same time.
4. Populate R32 and R33 with 0Ω resistors to connect the EEPROM SMBus interface to the retimer or redriver SDA and SDC pins.
5. Place an external EEPROM in dipsocket XU1. Modify resistor straps R26 – R31, R34 – R36 as necessary. Note that the EEPROM 8-bit address must be 0xA0 and capable of 400kHz operation at 2.5V or 3.3V supply.

2.5.4 SMBus Pull-Up Resistors

The SMBus interface uses open-drain clock and data inputs or outputs to enable device communication. The SDA and SDC lines each require a single 2kΩ to 5kΩ pull-up resistor. This codesign example offers multiple pull-up options.

- R22 and R23 are populated by default. These are 4.7kΩ pull-ups to 3.3V supply.
- R20 and R21 can be populated to use 2.7kΩ pull-ups to 2.5V supply near the retimer or redriver. These can be useful for debug purposes if the device SDA/SDC pins need to be disconnected from the main SMBus interface (by depopulating R24 and R25).
- R30 and R31 can be populated to use 2.7kΩ pull-ups to 2.5V supply near the external EEPROM. These can be useful for debug purposes if the EEPROM SDA/SDC pins need to be disconnected from the main SMBus interface (by depopulating R32 and R33).

2.5.5 Interrupt Output

DS250DF410 includes an interrupt output on pin H1 (INT_N) which is pulled low when an interrupt event occurs. This output is open-drain and requires a single 2kΩ to 5kΩ pull-up resistor. This codesign example includes a 4.7kΩ pull-up to 3.3V supply when R6 is populated and R16 is depopulated.

DS560MB410 does not include an interrupt output. Pin H1 (RSVD1) is a no connect on package and can be left floating or tied to GND. This codesign example includes a 1kΩ pull-down to GND when R16 is populated and R6 is depopulated.

2.5.6 Mux Select Inputs

DS560MB410 includes mux select inputs on pins D10 (MUXSEL0) and D2 (MUXSEL1). MUXSEL0 controls the crosspoint for channels 0–1, and MUXSEL1 controls the crosspoint for channels 2–3. The crosspoint can also be controlled entirely via SMBus register writes.

There are 2 options regarding mux select input connections to DS560MB410 within this codesign example.

1. Populate R9 and R12 with 0Ω resistors and depopulate R17 and R18. This allows an external device to control the crosspoint via LVCMOS voltage level inputs.
2. Populate R17 and R18 with 1kΩ resistors and depopulate R9 and R12. This option is most useful if the mux select inputs are unused.

DS250DF410 does not include mux select inputs. The crosspoint on this device is controlled entirely via SMBus register writes. Pins D10 (TEST0) and D2 (TEST1) are reserved TI test pins which can be left floating, tied to GND, or connected to a 2.5V output. This codesign example includes 1kΩ pull-downs to GND when R17 and R18 are populated and R9 and R12 are depopulated.

3 Codesign: 25GbE 8-Channel Retimer or Redriver with Crosspoint

TI has two 8-channel retimers and three 8-channel redrivers which support 25G Ethernet. The retimer part numbers are DS250DF810 and DS280DF810, while the redriver part numbers are DS280BR810, DS280BR820, and DS280MB810. All of these devices use a 8mm × 13mm, 135-pin BGA package and are nearly pin-to-pin compatible. A single board codesign can implement all 5 devices with minimal modifications, allowing designers to perform system-level testing before determining which device is best designed for a particular application.

Table 3-1 shows a comparison of features between DS2x0DF810, DS280BR8x0, and DS280MB810.

Table 3-1. DS2x0DF810, DS280BR8x0, and DS280MB810 Feature Comparison

Type	DS2x0DF810	DS280BR8x0	DS280MB810
Equalization capability	35dB	15-17dB	17dB
Receiver equalization	CTLE and DFE	CTLE	CTLE
Transmitter equalization	3-tap FIR filter	Fixed delay 3-tap FIR filter	None
Signal chain linearity	Nonlinear	Linear or nonlinear	Linear
Crosspoint	2x2 crosspoint	None	2x2 crosspoint
Crosspoint control	Register	N/A	Register or MUX pins
Calibration clock	25MHz clock required	Not required, can buffer 25MHz clock	Not required, can buffer 25MHz clock
Supply voltage	2.5V	2.5V	2.5V
Maximum current	1330mA	426mA	389mA

3.1 DS250DF810 and DS280DF810 Retimers Overview

The DS250DF810 and DS280DF810 retimers are both 8 channel retimer devices. The key differentiation between these devices is that DS250DF810 can lock to rates from 20.2752Gbps to 25.8Gbps and supported subrates, while the DS280DF810 can lock to rates from 20.2Gbps to 28.4Gbps and supported subrates. These devices can equalize channels with up to 35dB insertion loss at 12.89GHz using a combination of CTLE and DFE. The DS2x0DF810 also has a 3-tap FIR filter which allows for pre- and post- cursor equalization.

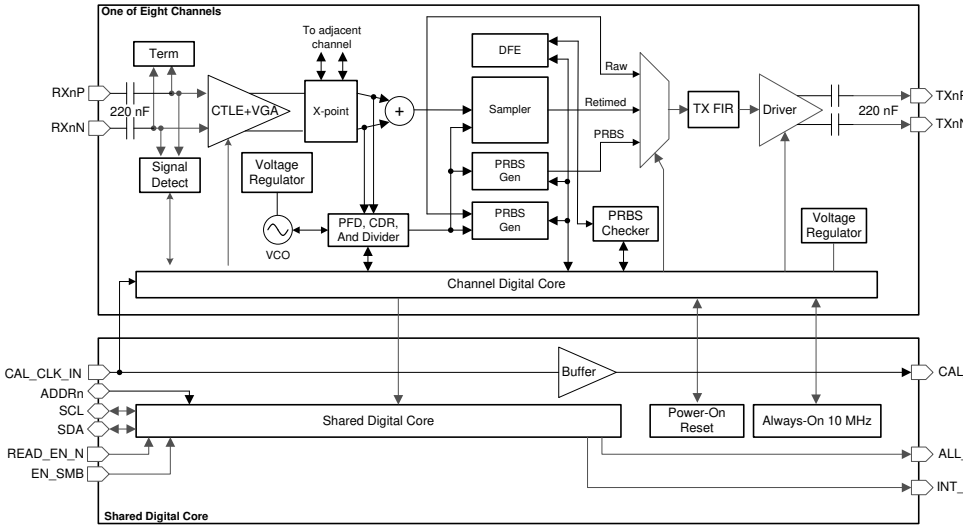

Figure 3-1. DS2x0DF810 Functional Block Diagram

Figure 3-2. DS2x0DF810 Pin Configuration

3.2 DS280BR810, DS280BR820, and DS280MB810 Redrivers Overview

The DS280BR810, DS280BR820, and DS280MB810 are 8 channel linear redriver devices supporting up to 28GBd NRZ. The key differentiation between DS280BR810 and DS280BR820 is that DS280BR810 has on-chip AC coupling for both RX and TX, while DS280BR820 has on-chip AC coupling for only RX. TI has observed better high speed performance with DS280BR820 over the DS280BR810, allowing for reach extension of over 17dB with DS280BR820 compared to over 15dB with DS280BR810. For new designs, TI recommends selecting DS280BR820 over DS280BR810. The DS280BR8x0 devices also have a limiting signal chain with fixed delay 3-tap TX FIR filter.

The DS280MB810 provides reach extension of over 17dB beyond normal ASIC to ASIC capability at 13.28GHz through the receiver CTLE. The differentiation between this device and DS280BR8x0 devices is that the device has a 2x2 cross point, but lacks the 3-tap TX FIR.

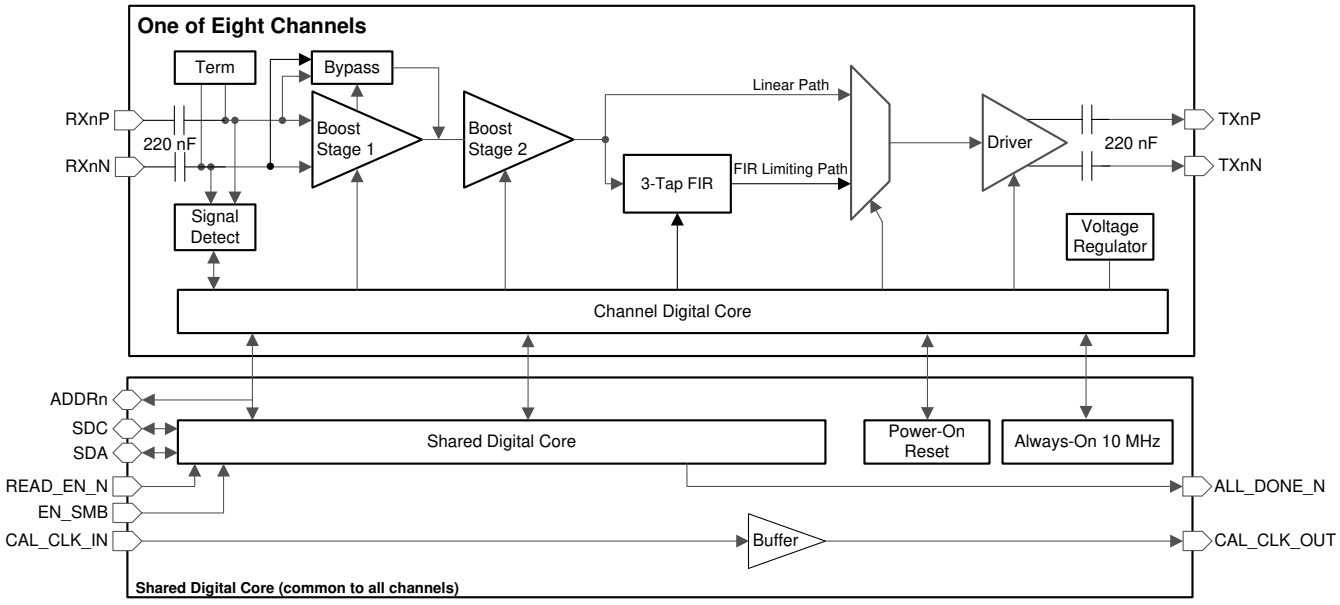

Figure 3-3. DS280BR810 Functional Block Diagram

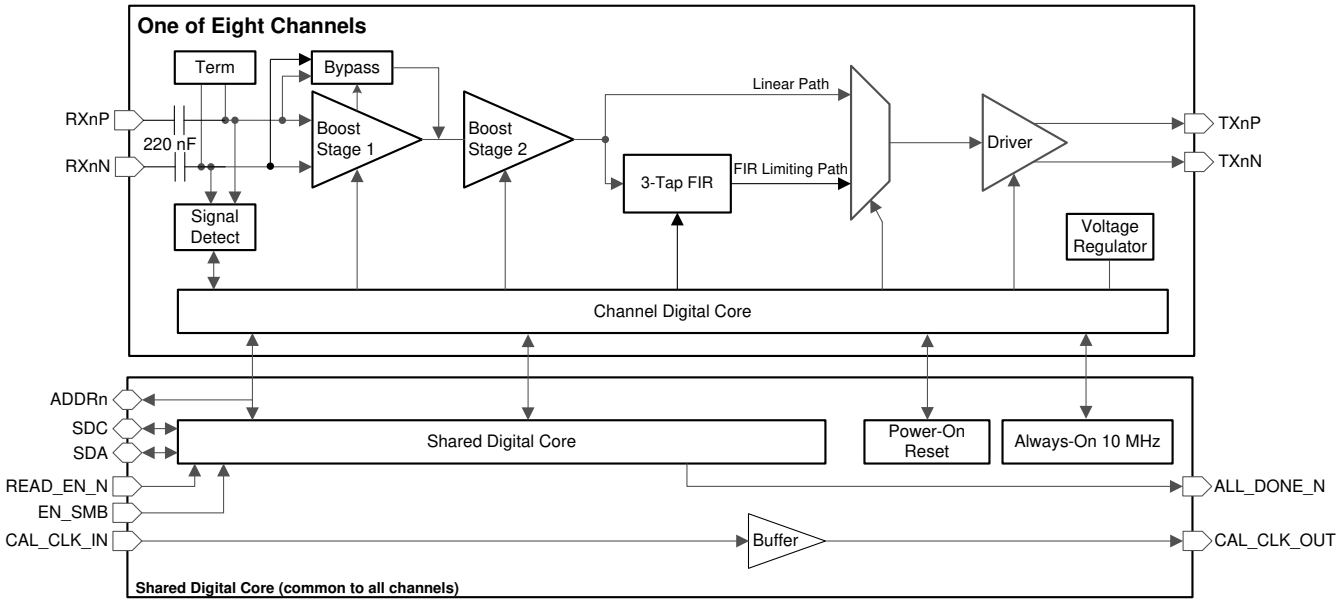

Figure 3-4. DS280BR820 Functional Block Diagram

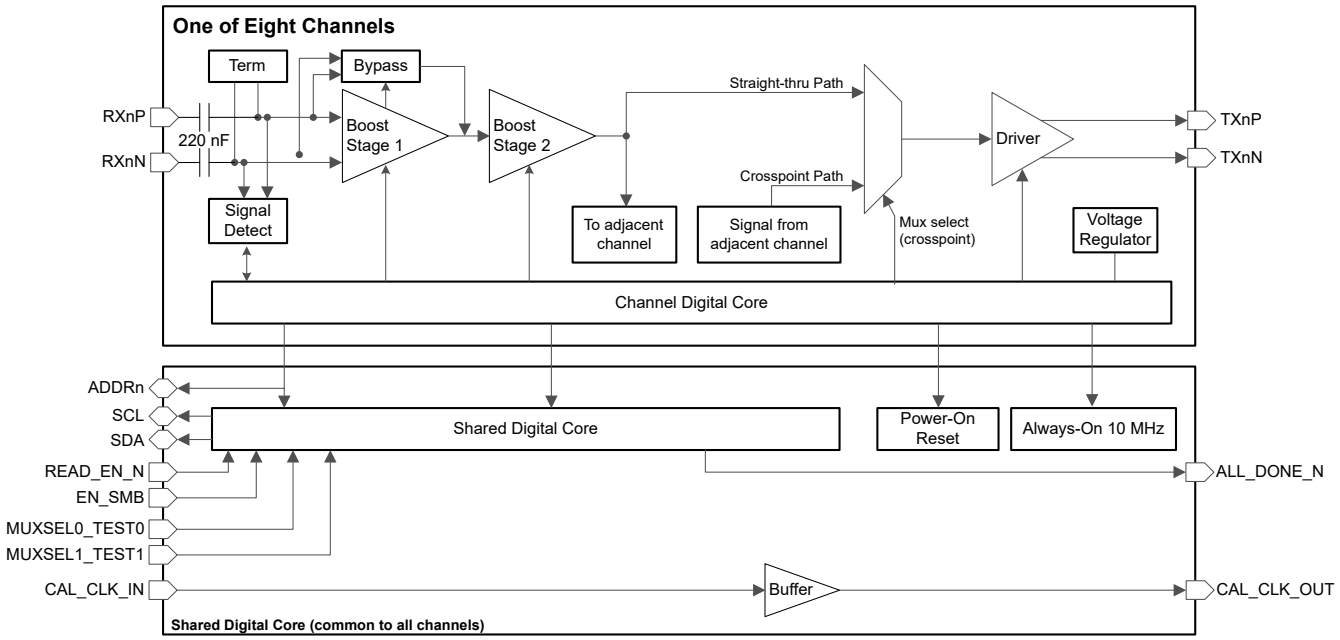

Figure 3-5. DS280MB810 Functional Block Diagram

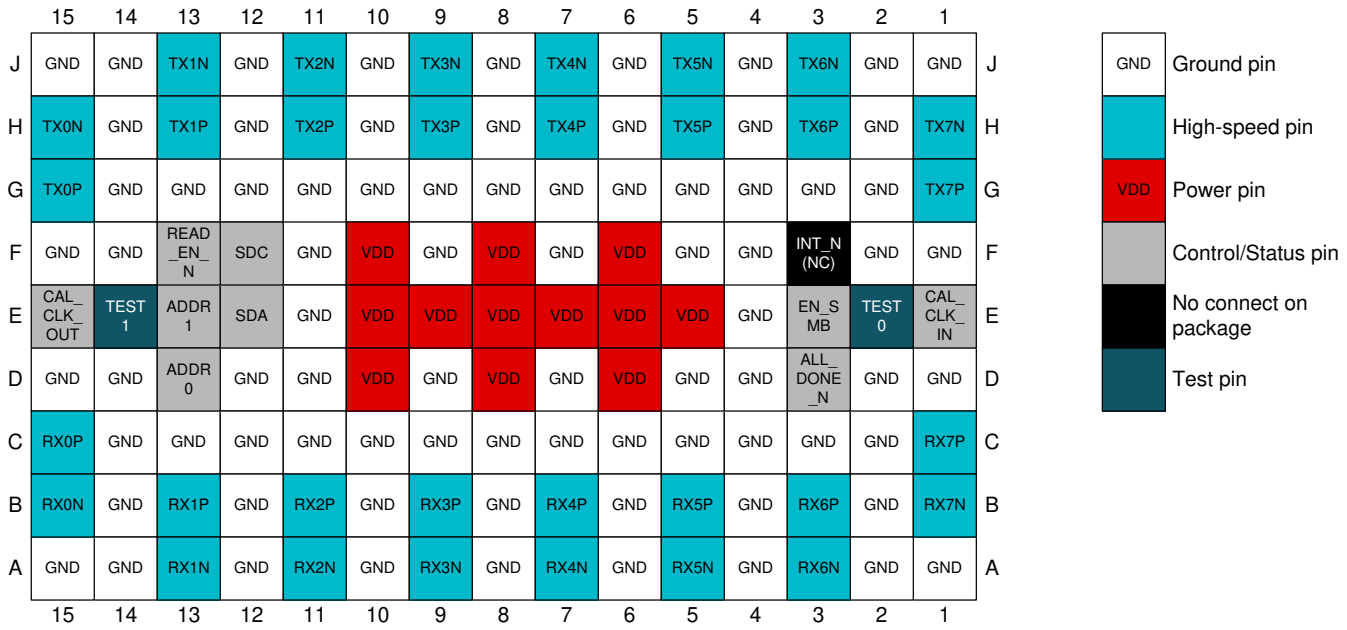

Figure 3-6. DS280BR8x0 Pin Configuration

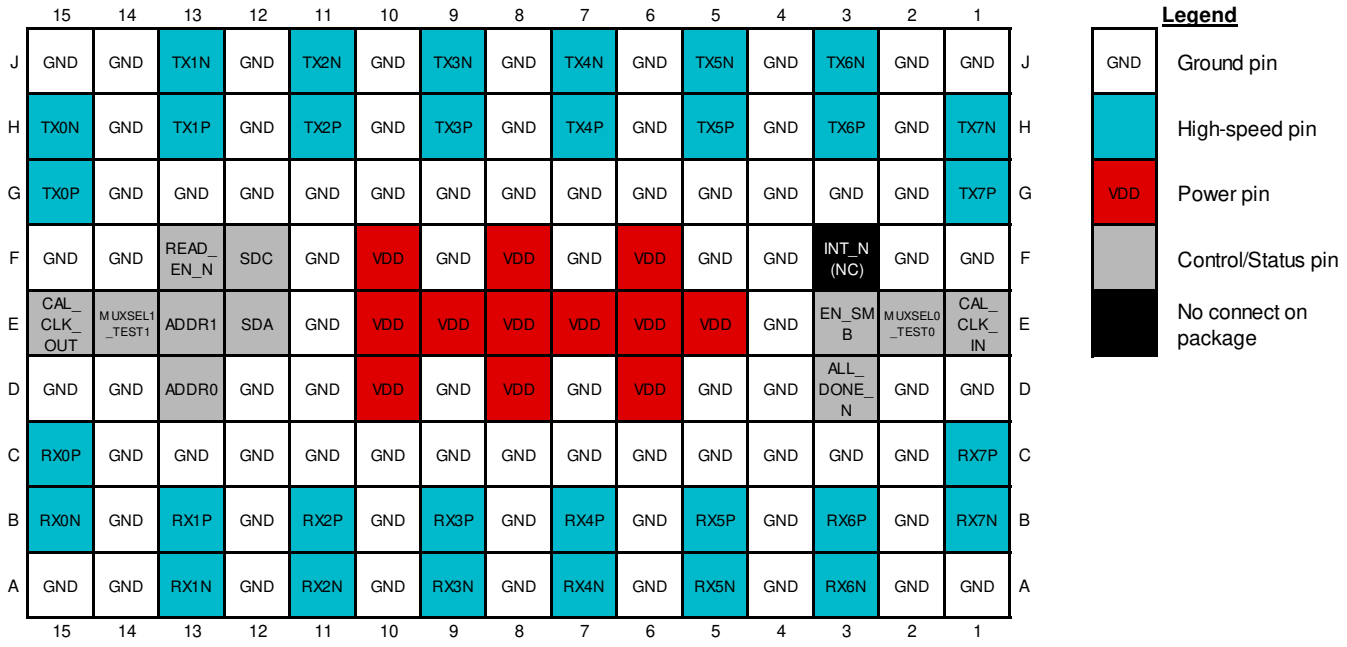

Figure 3-7. DS280MB810 Pin Configuration

3.3 Pin Comparison Table

Table 3-2 compares pin functionality of DS2x0DF810 retimers, DS280BR8x0 redrivers, and DS280MB810 redriver with crosspoint and lists if any design provisions are necessary to support each device with the same codesign.

Table 3-2. 8-Channel Retimer/Redriver Pin Comparison Table

Pin Number	DS2x0DF810 Pin Name	DS280BR8x0 Pin Name	DS280MB810 Pin Name	Provision Needed?	Details
C15, B15, B13, A13, B11, A11, B9, A9, B7, A7, B5, A5, B3, A3, C1, B1	RXnP/N	RXnP/N	RXnP/N	No	High-speed inputs AC coupled on-chip.
G15, H15, H13, J13, H11, J11, H9, J9, H7, J7, H5, J5, H3, J3, G1, H1	TXnP/N	TXnP/N	TXnP/N	Yes	**DS2x0DF810, DS280BR810:** High-speed outputs AC coupled on-chip. **DS280BR820, DS280MB810:** High-speed outputs require external AC coupling.
E1	CAL_CLK_IN	CAL_CLK_IN	CAL_CLK_IN	Optional	**DS2x0DF810:** Requires a 25MHz calibration clock input. **DS280BR8x0, DS280MB810:** Can optionally buffer a 25MHz clock input. No calibration clock required.
E15	CAL_CLK_OUT	CAL_CLK_OUT	CAL_CLK_OUT	Optional	2.5V buffered replica of CAL_CLK_IN.
D13, E13	ADDR0/1	ADDR0/1	ADDR0/1	No	4-level straps to configure SMBus Address.
E3	EN_SMB	EN_SMB	EN_SMB	No	4-level strap to select SMBus target mode or controller mode.
E12, F12	SDA/SDC	SDA/SDC	SDA/SDC	No	SMBus data and clock I/Os. Require 2-5kΩ pull-up resistors.
F13	READ_EN_N	READ_EN_N	READ_EN_N	No	**SMBus target mode:** Pull high or leave floating for normal operation. **SMBus controller mode:** Pull low to initiate EEPROM load.
D3	ALL_DONE_N	ALL_DONE_N	ALL_DONE_N	No	EEPROM load status when using SMBus controller mode.

Table 3-2. 8-Channel Retimer/Redriver Pin Comparison Table (continued)

Pin Number	DS2x0DF810 Pin Name	DS280BR8x0 Pin Name	DS280MB810 Pin Name	Provision Needed?	Details
F3	INT_N	INT_N	INT_N	No	**DS2x0DF810:** Interrupt open-drain output. Requires 2-5kΩ pull-up resistor. **DS280BR8x0, DS280MB810:** No connect on package. Can be pulled high for codesign compatibility with DS2x0DF810.
E2, E14	TEST0/1	TEST0/1	MUXSEL0/1	Optional	**DS2x0DF810, DS280BR8x0:** Reserved test pins. Can be left floating, tied to GND, or tied to 2.5V. **DS280MB810:** Mux select control input. Can be left floating or tied to GND if unused.
F4, E4, D4, D12	TEST4-7	GND	GND	No	**DS2x0DF810:** Reserved test pins. Can be left floating or tied to GND. **DS280BR8x0, DS280MB810:** Ground reference.
D6, D8, D10, E5, E6, E7, E8, E9, E10, F6, F8, F10	VDD	VDD	VDD	No	2.5V power supply. TI recommends connecting at least 6 decoupling capacitors as close to the device as possible.
A1, A2, A4, A6, A8, A10, A12, A14, A15, B2, B4, B6, B8, B10, B12, B14, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, D1, D2, D5, D7, D9, D11, D14, D15, E11, F1, F2, F5, F7, F9, F11, F14, F15, G2, G3, G4, G5, G6, G7, G8, G9, G10, G11, G12, G13, G14, H2, H4, H6, H8, H10, H12, H14, J1, J2, J4, J6, J8, J10, J12, J14, J15	GND	GND	GND	No	Ground reference.

3.4 Codesign Schematic Example

Figure 3-8, Figure 3-9, and Figure 3-10 show schematic diagrams for an example codesign which can be used with DS2x0DF810 retimers, DS280BR8x0 redrivers, and DS280MB810 redriver with crosspoint. A few component replacements are necessary to use each device with this codesign.

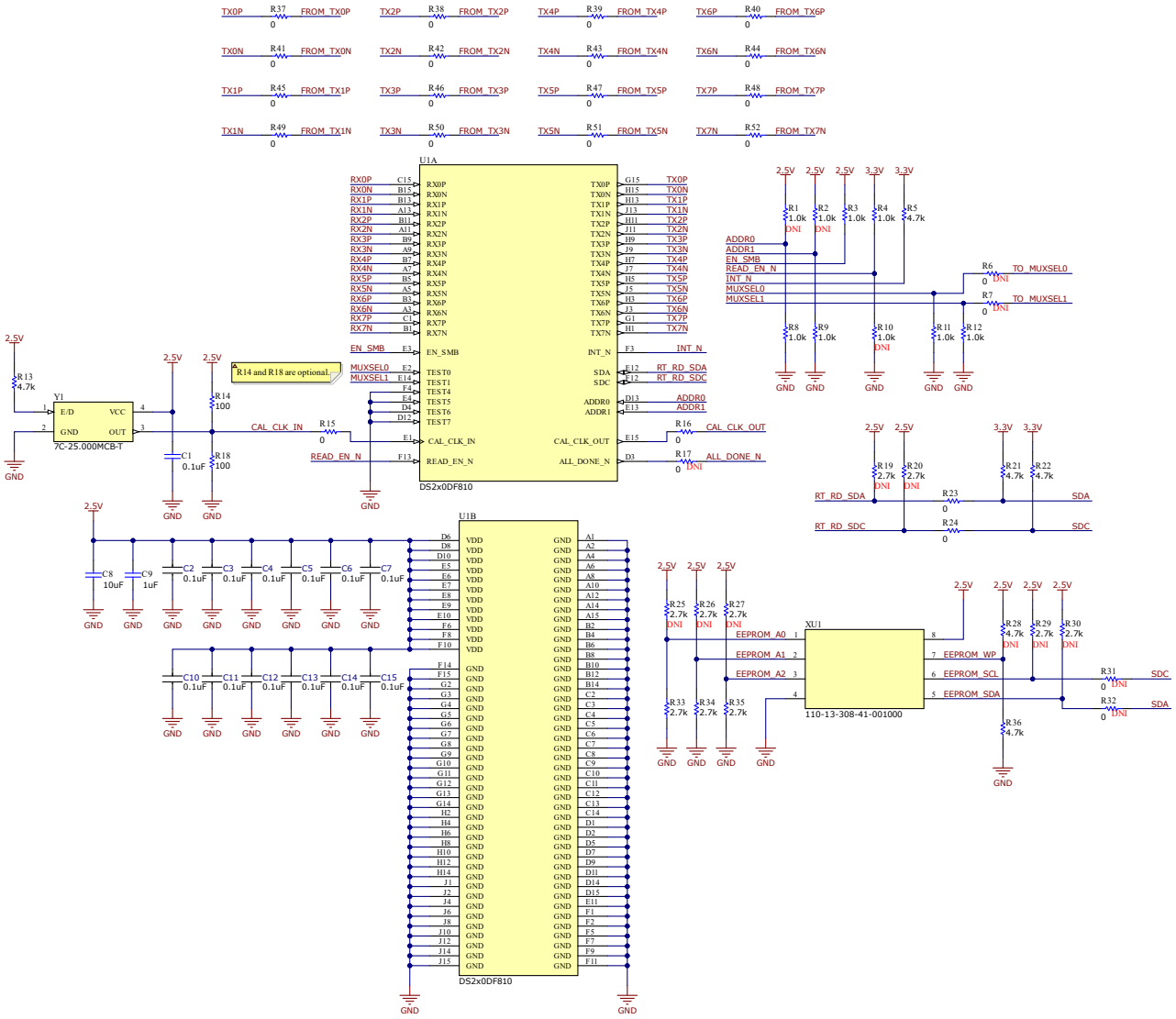

Figure 3-8. DS2x0DF810 Schematic Example

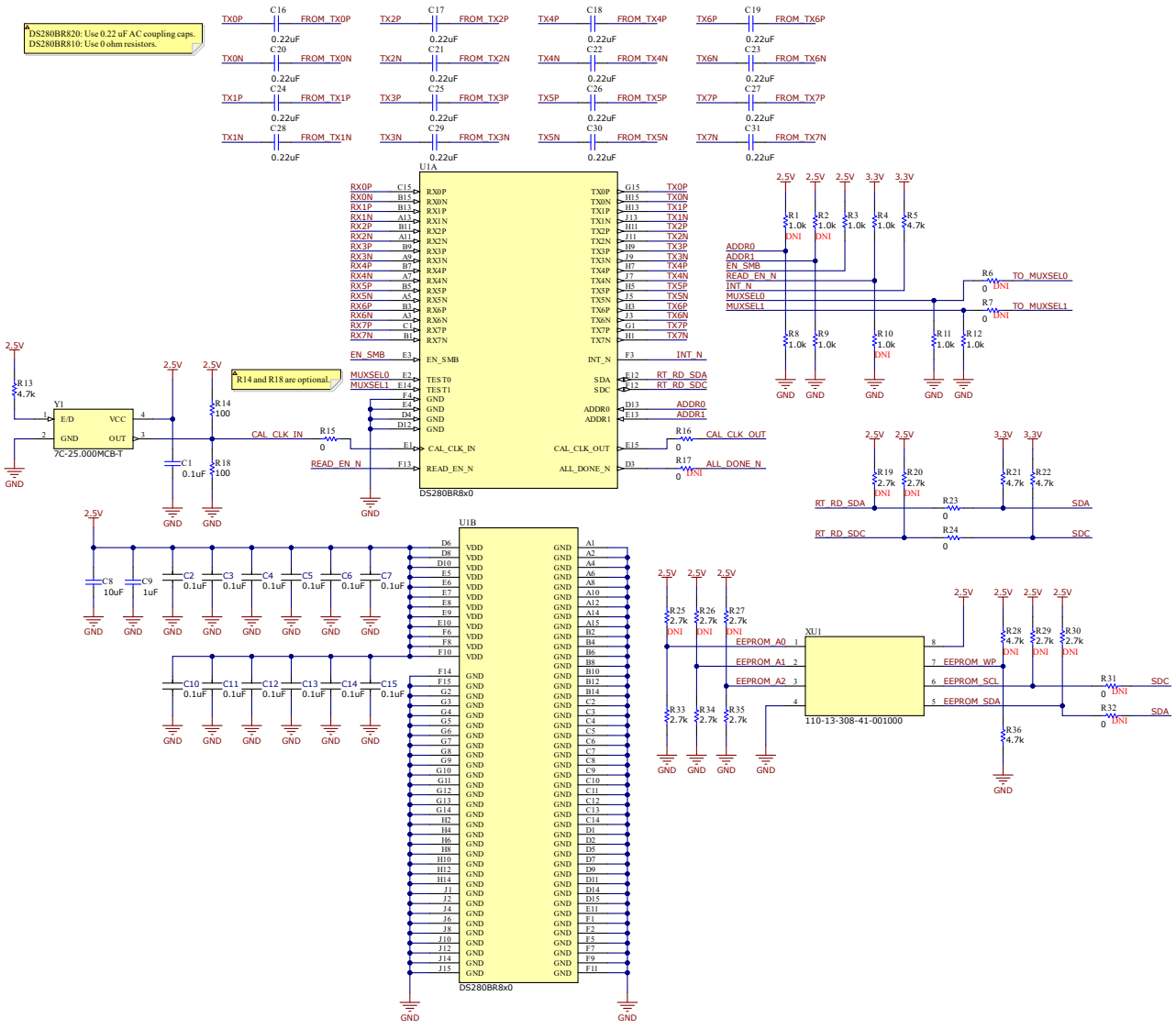

Figure 3-9. DS280BR8x0 Schematic Example

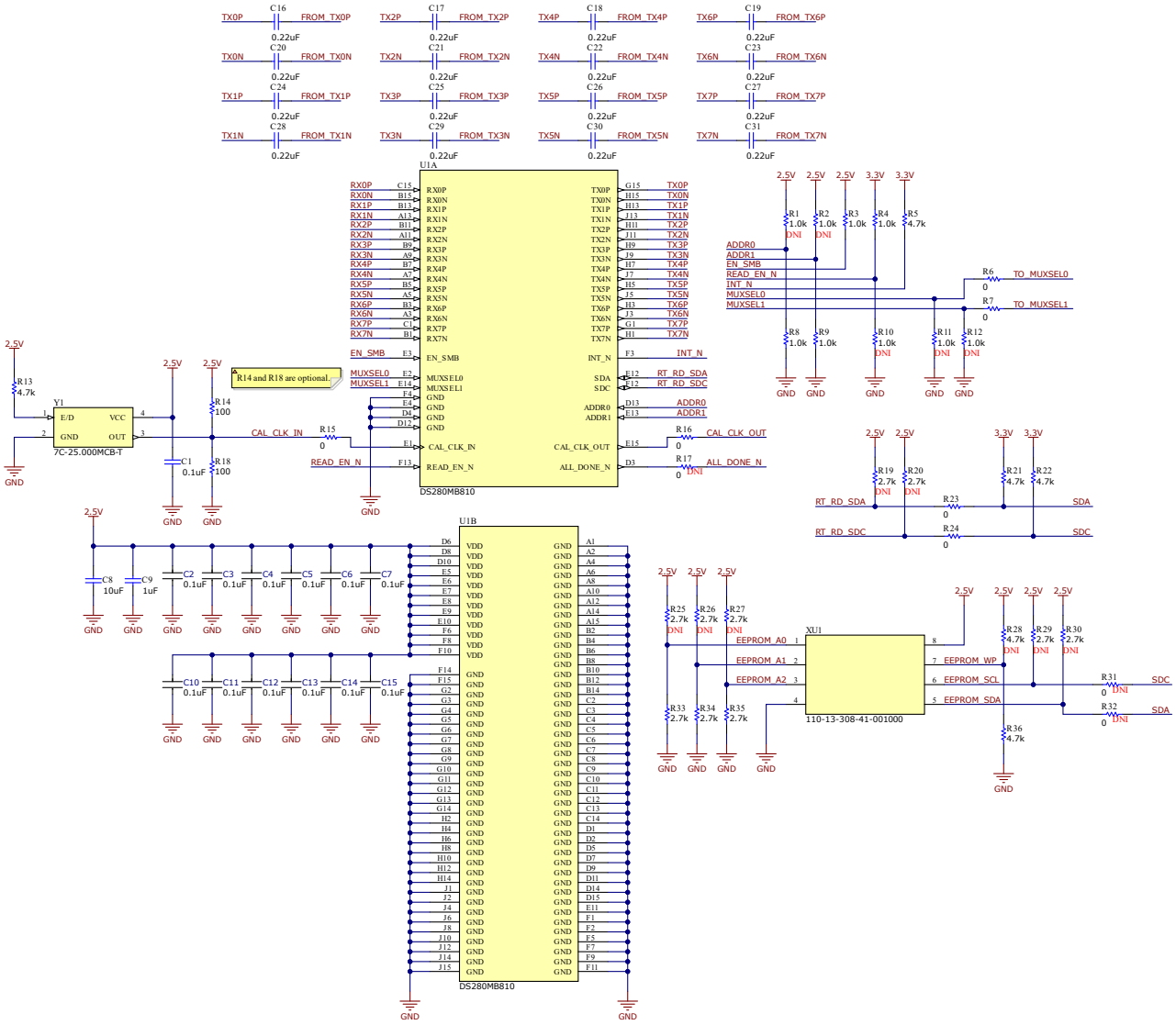

Figure 3-10. DS280MB810 Schematic Example

3.5 Notable Codesign Elements

3.5.1 AC Coupling

All 8-channel retimers and redrivers require AC coupling on high-speed inputs and outputs. AC coupling is integrated on-chip for all devices on the receiver side and some devices on the transmitter side.

DS250DF810, DS280DF810, and DS280BR810 include integrated AC coupling on the transmitter side. Therefore 0Ω resistors R37–R52 can be used on high-speed outputs.

DS280BR820 and DS280MB810 do not include integrated AC coupling on the transmitter side. Therefore R37–R52 need to be replaced with 220nF capacitors. These are labeled as C16–C31 in the codesign schematic examples.

3.5.2 Calibration Clock

DS2x0DF810 requires a 25MHz (±100PPM) 2.5V single-ended clock from external oscillator to be connected to pin E1 (CAL_CLK_IN). A 25MHz oscillator Y1 is included in the codesign schematic example. Pin E15 (CAL_CLK_OUT) outputs a 2.5V buffered replica of the calibration clock input for connecting multiple devices in a daisy-chained fashion.

DS280BR8x0 and DS280MB810 do not require an external calibration clock. Pin E1 (CAL_CLK_IN) can optionally support a 25MHz input clock. Pin E15 (CAL_CLK_OUT) outputs a 2.5V buffered replica of the calibration clock input.

There are two options regarding calibration clock connections to DS280BR8x0 and DS280MB810 within this codesign example.

1. Depopulate resistors R15 and R16 to disconnect the calibration clock input and output signals from the device.
2. Keep R15 and R16 populated to buffer the 25MHz reference clock signal. This option is most useful if the reference clock is connected to multiple devices in a daisy-chained fashion.

3.5.3 SMBus Address

Pins D13 (ADDR0) and E13 (ADDR1) are connected such that the 8-bit SMBus address for DS2x0DF810, DS280BR8x0, and DS280MB810 is 0x30 by default. Strap resistors R1, R2, R8, and R9 can be populated/depopulated with different values to select a different SMBus address. The four defined strap options are:

- 0: 1kΩ to GND
- R: 20kΩ to GND
- F: Float
- 1: 1kΩ to VDD

Table 3-3. SMBus Address Map

7-BIT TARGET ADDRESS	8-BIT WRITE ADDRESS	REQUIRED ADDRESS PIN STRAP VALUE	
		ADDR1	ADDR0
0x18	0x30	0	0
0x19	0x32	0	R
0x1A	0x34	0	F
0x1B	0x36	0	1
0x1C	0x38	R	0
0x1D	0x3A	R	R
0x1E	0x3C	R	F
0x1F	0x3E	R	1
0x20	0x40	F	0
0x21	0x42	F	R
0x22	0x44	F	F
0x23	0x46	F	1
0x24	0x48	1	0

Table 3-3. SMBus Address Map (continued)

7-BIT TARGET ADDRESS	8-BIT WRITE ADDRESS	REQUIRED ADDRESS PIN STRAP VALUE	
		ADDR1	ADDR0
0x25	0x4A	1	R
0x26	0x4C	1	F
0x27	0x4E	1	1

3.5.4 SMBus Controller Mode

Pin E3 (EN_SMB) is connected such that SMBus Target mode is selected for both DS2x0DF810, DS280BR8x0, and DS280MB810 by default. In SMBus Target mode, a controller accesses and modifies the retimer's or redriver's register configuration through the SMBus interface. In SMBus Controller mode, the retimer or redriver attempts to self-configure by reading the device settings stored in an external EEPROM.

DS2x0DF810, DS280BR8x0, and DS280MB810 can be reconfigured in SMBus Controller mode within this codesign example. The following design modifications need to be made.

1. Depopulate R3 to select SMBus Controller mode on the EN_SMB pin.
2. Depopulate R4 and populate R10 with a 1kΩ resistor. This pulls the READ_EN_N pin low to initiate EEPROM load.
3. Populate R17 with a 0Ω resistor to connect the ALL_DONE_N pin output. If multiple devices share a single EEPROM, then connect the ALL_DONE_N output of the first device to the READ_EN_N input of the next device to prevent multiple devices attempting to read the EEPROM at the same time.
4. Populate R31 and R32 with 0Ω resistors to connect the EEPROM SMBus interface to the retimer or redriver SDA and SDC pins.
5. Place an external EEPROM in dipsocket XU1. Modify resistor straps R25 – R30, R33 – R35 as necessary. Note that the EEPROM 8-bit address must be 0xA0 and capable of 400kHz operation at 2.5V or 3.3V supply.

3.5.5 SMBus Pull-Up Resistors

The SMBus interface uses open-drain clock and data inputs/outputs to enable device communication. The SDA and SDC lines each require a single 2kΩ to 5kΩ pull-up resistor. This codesign example offers multiple pull-up options.

- R21 and R22 are populated by default. These are 4.7kΩ pull-ups to 3.3V supply.
- R19 and R20 can be populated to use 2.7kΩ pull-ups to 2.5V supply near the retimer or redriver. These can be useful for debug purposes if the device SDA/SDC pins need to be disconnected from the main SMBus interface (by depopulating R23 and R24).
- R29 and R30 can be populated to use 2.7kΩ pull-ups to 2.5V supply near the external EEPROM. These can be useful for debug purposes if the EEPROM SDA/SDC pins need to be disconnected from the main SMBus interface (by depopulating R31 and R32).

3.5.6 Interrupt Output

DS2x0DF810 includes an interrupt output on pin F3 (INT_N) which is pulled low when an interrupt event occurs. This output is open-drain and requires a single 2kΩ to 5kΩ pull-up resistor. This codesign example includes a 4.7kΩ pull-up to 3.3V supply.

DS280BR8x0 and DS80MB810 do not include an interrupt output. Pin F3 (INT_N) is a no connect on package but can be connected to other devices' INT_N pins. This codesign example includes a 4.7k pull-up to 3.3V supply. No design provision is necessary to switch between retimer and redriver implementations.

3.5.7 Mux Select Inputs

DS280MB810 includes mux select inputs on pins E2 (MUXSEL0) and E14 (MUXSEL1). MUXSEL0 controls the crosspoint for channels 0–1 and 4–5, and MUXSEL1 controls the crosspoint for channels 2–3 and 6–7. The crosspoint can also be controlled entirely via SMBus register writes.

There are 2 options regarding mux select input connections to DS280MB810 within this codesign example.

1. Populate R6 and R7 with 0Ω resistors and depopulate R11 and R12. This allows an external device to control the crosspoint via LVCMOS voltage level inputs.

2. Populate R11 and R12 with 1kΩ resistors and depopulate R6 and R7. This option is most useful if the mux select inputs are unused.

DS2x0DF810 and DS280BR8x0 do not include mux select inputs. The crosspoint on DS2x0DF810 is controlled entirely via SMBus register writes. DS280BR8x0 does not include any crosspoint capability. On DS2x0DF810 and DS280BR8x0, pins E2 (TEST0) and E14 (TEST1) are reserved TI test pins which can be left floating, tied to GND, or connected to a 2.5V output. This codesign example includes 1kΩ pull-downs to GND when R11 and R12 are populated and R6 and R7 are depopulated.

4 Summary

TI's signal conditioning portfolio enables system designers the flexibility to implement a single socket supporting both redriver and retimer and characterize the performance. By leveraging information in this application note, designers can easily determine how to design a socket supporting both redriver and retimer. This allows engineers to minimize design risk while also maximizing signal conditioner price and power consumption.

5 References

- Texas Instruments, DS250DF410 product site
- Texas Instruments, DS560MB410 product site
- Texas Instruments, DS250DF810 product site
- Texas Instruments, DS280DF810 product site
- Texas Instruments, DS280BR810 product site
- Texas Instruments, DS280BR820 product site
- Texas Instruments, DS280MB810 product site

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