Application Brief

Level Shift No More: Support Low Voltage I/O Signals into a FPGA, Processor, or ASIC

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Background

Low voltage differential signaling (LVDS) interfaces are often internally integrated into data processing platforms such as field programmable gate arrays (FPGAs). The development of these platforms on smaller geometry CMOS processes has reduced voltage requirements for both the core supply and input/output (I/O) channels. These I/O requirements are defined by lower voltage standards designated by an *LV* (low voltage) prefix. Single-ended, 5V CMOS signals, for example, now come in lower voltage (LVCMOS) flavors, such as 3.3V, 2.5V, 1.8V, and 1.2V. Smaller geometry processes reach a limitation and cannot support the entire LVDS standard, requiring an external LVDS receiver solution. This application brief spotlights the DS90LVRA2-Q1, an external LVDS receiver solution that supports I/O voltages as low as 1.8V.

Point-to-Point LVDS Topology

LVDS is a differential physical (PHY) layer protocol that offers gigabits of data throughput using only milliwatts. A point-to-point LVDS application consists of an LVDS driver that sources a constant 3.5mA of drive current along a bus medium terminated by a 100-ohm resistor. The LVDS receiver determines a high or low data bit based on a positive or negative voltage swing across the bus termination of ±350mV. The LVDS driver translates LVCMOS or LVTTL single-ended inputs into an LVDS output. The LVDS receiver translates LVDS inputs into single-ended LVCMOS or LVTTL outputs.

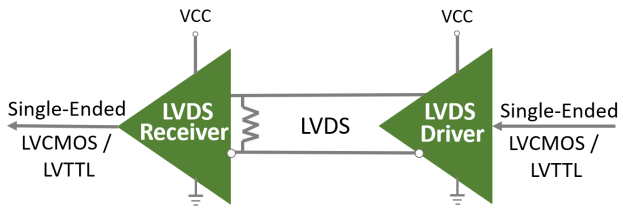

Figure 1. Point-to-Point LVDS Topology

Lower I/O Voltage Requirements

The development of smaller process technologies has reduced the core supply voltages for data capture platforms to 2.5V, 1.8V, and 1.2V. These platforms generally only send and receive signals that match the supply voltage. Most devices in the TI LVDS portfolio run at 3.3V and only accept and output 3.3V single-ended signals. This means that the I/O channels of these devices does not support the lower voltage signaling requirements these platforms require without the need for a level shifter. The TI application brief, *How to Support 1.8-V Signals Using a 3.3-V LVDS Driver/Receiver + Level-Shifter* details how this is achieved. The application note also provides practical tips and considerations for design implementation. The TI *Logic Guide* is another helpful resource to select the best level shifter for any application.

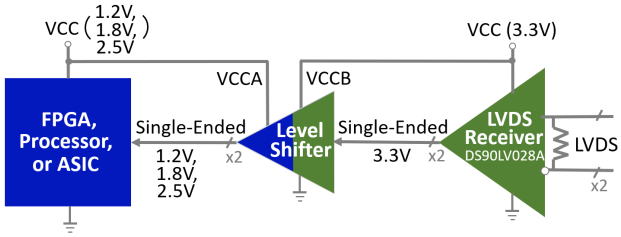

Figure 2. LVDS Receiver and Level Shifter to Support Low Voltage Signals

As an example, the DS90LV028A dual-channel 3.3V receiver supports up to two LVDS inputs and two single-ended 3.3V LVCMOS outputs. The outputs must be level shifted to meet the lower I/O voltage requirement for a low power processing platform. One option is implementing a dual-channel level-shifter, such as the SN74AVC2T45-Q1. Level shifters can limit receiver performance for metrics such as signaling rates and this must be considered in device selection.

Level Shift No More with TI LVDS Receivers

Level shifters increase design complexity and can limit receiver performance. The use of two devices, driver or receiver and a level shifter, plus associated discrete components take up more PCB area and requires the use of a 3.3V supply in the design.

For a more integrated solution, Texas Instruments offers the DS90LVRA2-Q1. This device is a dual-channel automotive grade LVDS receiver that operates at signaling rates up to 600Mbps. The DS90LVRA2-Q1 offers the flexibility to operate at 3.3V, 2.5V, and 1.8V to drive LVCMOS output signals to these voltage levels, thus eliminating the need for a separate level shifter device to meet lower voltage input signal specifications.

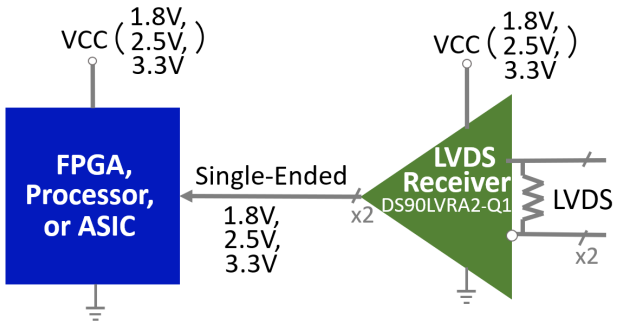

Figure 3. DS90LVRA2-Q1 Dual-Channel LVDS Receiver to Support Low Voltage Output Signals

The DS90LVRA2 is the non-automotive grade version of the DS90LVRA2-Q1. This device operates only as a 1.8V LVDS receiver with a 1.8V LVCMOS output.

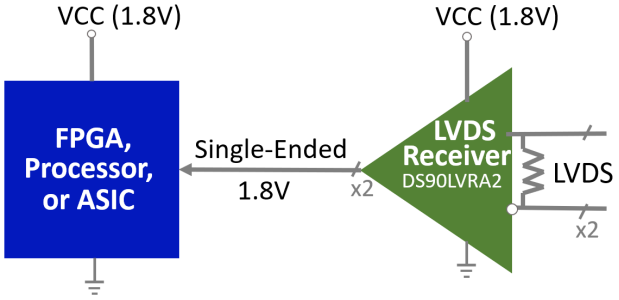

Figure 4. DS90LVRA2 Dual-Channel LVDS Receiver to Support 1.8V Output Signals

The SN65LVDS4 is a non-automotive grade, single-channel LVDS receiver. It operates at signaling rates up to 500Mbps. The device drives 3.3V LVTTL, 2.5V LVCMOS, 1.8V LVCMOS outputs based on the output drive voltage pin (VDD), eliminating the need for a separate level shifter device to meet lower voltage input signal specifications. However, the SN65LVDS4 requires two voltage supply pins (VCC and VDD), whereas the DS90LVRA2-Q1 and DS90LVRA2 offer the advantage of a single voltage supply pin.

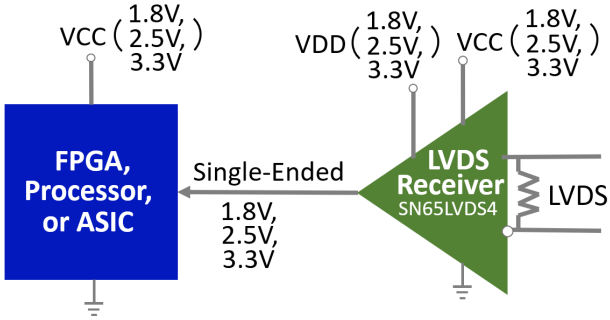

Figure 5. SN65LVDS4 Single-Channel LVDS Receiver to Support Low Voltage Output Signals

Lower Voltage Solutions for TI LVDS Drivers

The TI LVDS portfolio does not currently offer a lower voltage LVDS driver. The automotive-grade DS90LV027AQ-Q1 dual-channel 3.3V LVDS driver is the recommended pair for the DS90LVRA2-Q1. See the TI application brief, *How to Use a 3.3-V LVDS Buffer as a Low-Voltage LVDS Driver,* for applications requiring lower voltage input signals. A LVDS driver does not require a level shifter when a simple biasing network is implemented.

System Advantages of External LVDS Interfaces

1: Optimize FPGA Performance

FPGAs commonly have internally integrated programmable LVDS interfaces. Designing with an external LVDS receiver offloads the interface, meaning that FPGA power and performance are not sacrificed. This is highlighted in the TI application brief *Enabling LVDS Links for Low Power FPGAs, Processors, and ASIC Implementations*.

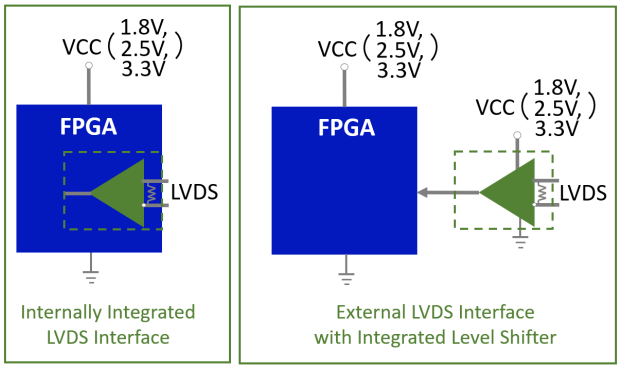

Figure 6. Optimize FPGA Performance by Offloading the LVDS Interface

2: Design Flexibility and Lower Cost FPGAs

Smaller geometry CMOS processes are a limiting factor in the feasibility of offering an internally integrated LVDS receiver and are unable to support entire common-mode voltage (VCM) range of the LVDS standard. The standard allows for a ±1-V common-mode ground shift, meaning that the VCM is as high as 2.2V. Additionally, system designs with the potential for large ground shifts further benefit from external LVDS interfaces that offer extended common-mode range voltages as high as 5V. FPGAs with integrated LVDS interfaces are typically more expensive. In some designs, an external LVDS interface offers system design flexibility and reduces complexity and cost.

3: Reduced Power Budget

Using lower power data capture platforms helps optimize power consumption, allowing for smaller systems that are cheaper, more reliable, and reduce thermal design complexity by reducing the need for fans or heat sinks. Application-specific integrated circuits (ASICs) are non-programmable logic devices with fixed logic sources, allowing for predictable power consumption, while modern FPGAs require three separate power supplies and the overall power consumption is design-dependent.

The TI application note, *Fast Forward Your FPGA Power Design with TI Designs,* highlights the use of power-management integrated circuits (PMICs) as integrated power solutions. This link provides a comprehensive overview of power solutions using Texas Instruments processors. The site also includes power solutions compatible with other popular processors and FPGAs, such as Altera and Xilinx.

Conclusion

Smaller geometry CMOS processes have reduced core and I/O voltage requirements and limited the feasibility of internally integrated LVDS receiving solutions in data capture platforms. The DS90LVRA2-Q1 dual-channel LVDS receiver is an external solution with integrated features that eliminate the need for a separate level shifting device for platforms requiring inputs as low as 1.8V. This solution increases design flexibility while reducing component count and supports the lower voltage signal requirements of many smaller geometry CMOS processes. The DS90LVRA2 dual-channel 1.8-V receiver and the SN65LVDS4 single-channel receiver offer similar benefits.

References

1. Texas Instruments, *How to Support 1.8-V Signals Using a 3.3-V LVDS Driver/Receiver and Level-Shifter*, Application Brief
2. Texas Instruments, *How to Use a 3.3-V LVDS Buffer as a Low-Voltage LVDS Driver*, Application Brief
3. Texas Instruments, *Enabling LVDS Links for Low Power FPGAs, Processors, and ASIC Implementations*, Application Brief
4. Texas Instruments, *Fast Forward Your FPGA Power Design with TI Designs*, Technical Article

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