Application Note

TDP2004 Configuration Guide

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ABSTRACT

This document includes how to configure and setup the TDP2004. This configuration guide needs to be used alongside the *TDP2004* data sheet, the TDP2004 Schematic Checklist, and the *TDP2004 EVM Users Guide* to make sure proper implementation.

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Trademarks

1 Introduction

The TDP2004 is a four-channel multi-rate linear repeater with integrated signal conditioning. The signal channels of the device operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE) and a linear output driver, which together compensate for a lossy transmission channel between the source transmitter and the final receiver.

2 Access Methods

For the TDP2004, there are five 5-level input pins: MODE, EQ0/ADDR0, EQ1/ADDR1, GAIN/SDA, and TEST/SCL.

These 5-level inputs use an external resistor to help set the five valid levels as shown in Table 2-1.

Table 2-1. TDP2004 5-Level Control Pin Settings

Level	Setting
L0	1kΩ to GND
L1	8.25kΩ to GND
L2	24.9kΩ to GND
L3	75kΩ to GND
L4	Floating

The TDP2004 can be configured in three different ways through the MODE pin:

Table 2-2. TDP2004 Mode Configuration

Level	Configuration
L0	Pin-strap mode
L1	SMBus/ I2C primary mode
L2	SMBus/ I2C secondary mode
L3 and L4	Reserved

Pin strap mode – The TDP2004 control configuration is done solely by strap pins.

SMBus/I2C Primary mode – The TDP2004 control configuration is automatically read from an external EEPROM.

SMBus/I2C Secondary mode – The TDP2004 control configuration is controlled through an external Serial Management Bus (SMBus/I2C)

2.1 Pin-Strap Mode

In pin strap mode, EQ0/ADDR0 and EQ1/ADDR1 set the receiver linear equalization (CTLE) boost for channels 0-3. The GAIN/SDA sets the flat gain (DC and AC) from the input to the output of the TDP2004 for channels 0-3. The TEST/SCL is the TI test mode and must be left floating. For detailed pin strap mode configuration, please refer to the *TDP2004 Schematic Checklist*, application note.

2.2 SMBus, I2C Primary Mode

In the SMBus, I2C Primary mode, GAIN/SDA is the 3.3V SMBUS/I2C data and TEST/SCL is the 3.3V SMBUS/I2C clock. Both require an external 1kΩ to 5kΩ pullup resistor per the SMBus, I2C interface standard.

The TDP2004 automatically reads the initial configuration setting from an external EEPROM (SMBus 8-bit address 0xA0) at power up. Multiple TDP2004 can be cascaded to read from single EEPROM. Tie the READ_EN_N pin of the first device low (GND) to automatically initiate EEPROM read at power up. DONEn of the first device can be fed into READ_EN_N of the next device with 4.7kΩ pullup resistors. Leave the DONEn pin of the final device floating, or connect the pin to a microcontroller input to monitor the completion of the final EEPROM read.

2.3 SMBus, I2C Secondary Mode

There are 16 unique SMBus secondary addresses that can be assigned to the device by placing external resistor straps on the EQ0 / ADDR0 and EQ1 / ADDR1 pins as provided in Table 2-2. When multiple TDP2004 devices are on the same SMBus interface bus, each device must be configured with a unique SMBus secondary address.

GAIN/SDA is the 3.3V SMBus, I2C data and TEST/SCL is the 3.3V SMBus, I2C clock. Both require an external 1kΩ to 5kΩ pullup resistor per the SMBus, I2C interface standard.

3 Register Mapping

The TDP2004 has two types of registers:

- **Shared Registers**: these registers can be accessed at any time and are used for device-level configuration, status read back, control, or to read back the device ID information.
- **Channel Registers**: these registers are used to control and configure specific features for each individual channel. All channels have the same register set and can be configured independent of each other or configured as a group through broadcast writes to Channels 0-3.

3.1 Shared Registers

Table 3-1. General Registers (Offset = 0xE2)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	rst_i2c_regs	R/W/SC	0x0	Device reset control: Reset all I^2C registers to default values (self-clearing).
5	rst_i2c_mas	R/W/SC	0x0	Reset I^2C Primary (self-clearing).
4-1	RESERVED	R	0x0	Reserved
0	frc_eeprm_rd	R/W/SC	0x0	Override MODE and READ_EN_N status to force manual EEPROM configuration load.

Table 3-2. EEPROM_Status Register (Offset = 0xE3)

Bit	Field	Type	Reset	Description
7	eecfg_cmplt	R	0x0	EEPROM load complete.
6	eecfg_fail	R	0x0	EEPROM load failed.
5	eecfg_atmpt_1	R	0x0	Number of attempts made to load EEPROM image.
4	eecfg_atmpt_0	R	0x0	
3	eecfg_cmplt	R	0x0	EEPROM load complete 2.
2	eecfg_fail	R	0x0	EEPROM load failed 2.
1	eecfg_atmpt_1	R	0x0	Number of attempts made to load EEPROM image 2.
0	eecfg_atmpt_0	R	0x0	

Table 3-3. DEVICE_ID0 Register (Offset = 0xF0)

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3	device_id0_3	R	0x0	Device ID0 [3:1]: 011
2	device_id0_2	R	0x1	
1	device_id0_1	R	0x1	
0	RESERVED	R	X	Reserved

Table 3-4. DEVICE_ID1 Register (Offset = 0xF1)

Bit	Field	Type	Reset	Description
7	device_id[7]	R	0x0	Device ID 0010 1001: TDP2004
6	device_id[6]	R	0x0	
5	device_id[5]	R	0x1	
4	device_id[4]	R	0x0	
3	device_id[3]	R	0x1	
2	device_id[2]	R	0x0	
1	device_id[1]	R	0x0	
0	device_id[0]	R	0x0	

3.2 Channel Registers

Table 3-5. EQ Gain Control Register (Channel Register Base + Offset = 0x01)

Bit	Field	Type	Reset	Description
7	eq_stage1_bypass	R/W	0x0	Enable EQ stage 1 bypass: 0: Bypass disabled 1: Bypass enabled
6	eq_stage1_3	R/W	0x0	EQBoost stage 1 control See Table 6-1 in the data sheet for details
5	eq_stage1_2	R/W	0x0	
4	eq_stage1_1	R/W	0x0	
3	eq_stage1_0	R/W	0x0	
2	eq_stage2_2	R/W	0x0	EQ Boost stage 2 control See Table 6-1 in the data sheet for details
1	eq_stage2_1	R/W	0x0	
0	eq_stage2_0	R/W	0x0	

Table 3-6. EQ Gain, Flat Gain Control Register (Channel Register Base + Offset = 0x03)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	eq_profile_3	R/W	0x0	EQ mid-frequency boost profile See Table 6-1 in the data sheet for details
5	eq_profile_2	R/W	0x0	
4	eq_profile_1	R/W	0x0	
3	eq_profile_0	R/W	0x0	
2	flat_gain_2	R/W	0x1	Flat gain select: See Table 6-2 in the data sheet for details
1	flat_gain_1	R/W	0x0	
0	flat_gain_0	R/W	0x1	

Table 3-7. TI Test Mode Control Register (Channel Register Base + Offset = 0x04)

Bit	Field	Type	Reset	Description
7-3, 1-0	RESERVED	R	0x0	Reserved
2	TI test mode	R/W	0x0	Set TI test mode: 0: test mode is enabled 1: test mode is disabled. Must be set to "1" for normal operation.

Table 3-8. PD Override Register (Channel Register Base + Offset = 0x05)

Bit	Field	Type	Reset	Description
7	device_en_override	R/W	0x0	Enable power down overrides through SMBus/I^2C 0: Manual override disabled 1: Manual override enabled

Table 3-8. PD Override Register (Channel Register Base + Offset = 0x05) (continued)

Bit	Field	Type	Reset	Description
6-0	device_en	R/W	0x111111	Manual power down of redriver various blocks of a channel – gated by device_en_override = 1 111111: All blocks in the channel are enabled 000000: All blocks in the channel are disabled

Table 3-9. Bias Register (Channel Register Base + Offset = 0x06)

Bit	Field	Type	Reset	Description
5-3	Bias current	R/W	0x100	Control bias current Set 001 for best performance
7,6,2-0	Reserved	R/W	0x00000	Reserved

4 RX Equalization Control Settings

The TDP2004 receivers feature a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. The receivers implement two stage linear equalizer for wide range of equalization capability. The equalizer stages also provide flexibility to make subtle modifications of mid-frequency boost for best EQ gain profile match with wide range of channel media characteristics. The EQ profile control feature is only available in SMBus/I^{2}C mode. In Pin mode the settings are optimized for FR4 traces.

Table 4-1 provides available equalization boost at 20Gbps (10GHz Nyquist frequency) through EQ control pins or SMBus/I^{2}C registers. In Pin Control mode EQ1 and EQ0 pins set equalization boost for channels 0-3. In I^{2}C mode individual channels can be independently programmed for EQ boost.

Table 4-1. Equalization Control Settings

EQUALIZATION SETTING							TYPICAL EQ BOOST (dB)
EQ INDEX	Pin mode		SMBus/I^{2}C Mode				at 10GHz
	EQ1	EQ0	eq_stage1_3:0	eq_stage2_2:0	eq_profile_3:0	eq_stage1_bypass	
0	L0	L0	0	0	0	1	4.0
1	L0	L1	1	0	0	1	5.0
2	L0	L2	3	0	0	1	7.0
5	L1	L0	0	0	1	0	8.0
6	L1	L1	1	0	1	0	9.0
7	L1	L2	2	0	1	0	9.5
8	L1	L3	3	0	3	0	10.0
9	L1	L4	4	0	3	0	11.0
10	L2	L0	5	1	7	0	12.0
11	L2	L1	6	1	7	0	12.5
12	L2	L2	8	1	7	0	13.5
13	L2	L3	10	1	7	0	14.5
14	L2	L4	10	2	15	0	15.0
15	L3	L0	11	3	15	0	15.5
16	L3	L1	12	4	15	0	16.5
17	L3	L2	13	5	15	0	17.0
18	L3	L3	14	6	15	0	18.0
19	L3	L4	15	7	15	0	19.0

5 Flat-Gain

The GAIN pin can be used to set the overall data-path flat gain (DC and AC) of the TDP2004when the device is in Pin mode. The pin GAIN sets the flat-gain for channels 0-3. In I^2C mode each channel can be independently set. Table 5-1 provides flat gain control configuration settings. For most systems the default setting of GAIN = L4 (float) is recommended that provides flat gain of 0dB.

The flat-gain and equalization of the TDP2004 must be set such that the output signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively.

Table 5-1. Flat Gain Configuration Settings

Pin mode GAIN	I^2C Modeflat_gain_2:0	Flat Gain
L0	0	–5.6dB
L1	1	–3.8dB
L2	3	–1.2dB
L4 (float)	5	0.6dB (default recommendation)
L3	7	+2.6dB

6 RX Equalization and Flat Gain Selection Matrix

Table 6-1. RX Equalization and Flat Gain Selection Matrix

CTLE Index	Flat Gian	Reg. Range Offset 0x01	Reg. Range Offset 0x03
0	-6dB	0x80	0x00
0	-4dB	0x80	0x01
0	-2dB	0x80	0x03
0	0dB (default)	0x80	0x05
0	2dB	0x80	0x07
1	-6dB	0x88	0x00
1	-4dB	0x88	0x01
1	-2dB	0x88	0x03
1	0dB (default)	0x88	0x05
1	2dB	0x88	0x07
2	-6dB	0x98	0x00
2	-4dB	0x98	0x01
2	-2dB	0x98	0x03
2	0dB (default)	0x98	0x05
2	2dB	0x98	0x07
Default	-6dB	0x00	0x00
Default	-4dB	0x00	0x01
Default	-2dB	0x00	0x03
Default	0dB (default)	0x00	0x05
Default	2dB	0x00	0x07
5	-6dB	0x00	0x08
5	-4dB	0x00	0x09
5	-2dB	0x00	0x0B
5	0dB (default)	0x00	0x0D
5	2dB	0x00	0x0F
6	-6dB	0x08	0x08
6	-4dB	0x08	0x09
6	-2dB	0x08	0x0B
6	0dB (default)	0x08	0x0D
6	2dB	0x08	0x0F
7	-6dB	0x10	0x08
7	-4dB	0x10	0x09
7	-2dB	0x10	0x0B
7	0dB 9default)	0x10	0x0D
7	2dB	0x10	0x0F
8	-6dB	0x18	0x18
8	-4dB	0x18	0x19
8	-2dB	0x18	0x1B

Table 6-1. RX Equalization and Flat Gain Selection Matrix (continued)

CTLE Index	Flat Gian	Reg. Range Offset 0x01	Reg. Range Offset 0x03
8	0dB (default)	0x18	0x1D
8	2dB	0x18	0x1F
9	-6dB	0x20	0x18
9	-4dB	0x20	0x19
9	-2dB	0x20	0x1B
9	0dB (default)	0x20	0x1D
9	2dB	0x20	0x1F
10	-6dB	0x29	0x38
10	-4dB	0x29	0x39
10	-2dB	0x29	0x3B
10	-2dB	0x29	0x3D
10	0dB (default)	0x29	0x3F
11	-6dB	0x31	0x38
11	-4dB	0x31	0x39
11	-2dB	0x31	0x3B
11	0dB (default)	0x31	0x3D
11	2dB	0x31	0x3F
12	-6dB	0x41	0x38
12	-4dB	0x41	0x39
12	-2dB	0x41	0x3B
12	0dB (default)	0x41	0x3D
12	2dB	0x41	0x3F
13	-6dB	0x51	0x38
13	-4dB	0x51	0x39
13	-2dB	0x51	0x3B
13	0dB (default)	0x51	0x3D
13	2dB	0x51	0x3F
14	-6dB	0x52	0x78
14	-4dB	0x52	0x79
14	-2dB	0x52	0x7B
14	0dB (default)	0x52	0x7D
14	2dB	0x52	0x7F
15	-6dB	0x5B	0x78
15	-4dB	0x5B	0x79
15	-2dB	0x5B	0x7B
15	0dB (default)	0x5B	0x7D
15	2dB	0x5B	0x7F
16	-6dB	0x64	0x78
16	-4dB	0x64	0x79
16	-2dB	0x64	0x7B

Table 6-1. RX Equalization and Flat Gain Selection Matrix (continued)

CTLE Index	Flat Gian	Reg. Range Offset 0x01	Reg. Range Offset 0x03
16	0dB (default)	0x64	0x7D
16	2dB	0x64	0x7F
17	-6dB	0x6D	0x78
17	-4dB	0x6D	0x79
17	-2dB	0x6D	0x7B
17	0dB (default)	0x6D	0x7D
17	2dB	0x6D	0x7F
18	-6dB	0x76	0x78
18	-4dB	0x76	0x79
18	-2dB	0x76	0x7B
18	0dB (default)	0x76	0x7D
18	2dB	0x76	0x7F
19	-6dB	0x7F	0x78
19	-4dB	0x7F	0x79
19	-2dB	0x7F	0x7B
19	0dB (default)	0x7F	0x7D
19	2dB	0x7F	0x7F

7 TDP2004 Programming Example

In the following examples, assume that SMBus secondary address 0x18 is used for Device 0 (Channels 0-3) and SMBus secondary address 0x1A is used for Device 1 (Channels 0-3). Example code using TotalPhase Aardvark I2C controller

7.1 PD Control Through Register Programming

Broadcast write to Device 0 and Device 1 Bank 0 registers at Channel register 0x85 (Channel base register 0x80 + PD Override register 0ffset 0x05) with a value of 0x80 to **power down** all channels.

- <I2c_srite addr= "0x18" count = "0" radix"16">85 80</i2c write>
- <I2c_srite addr= "0x1A" count = "0" radix"16">85 80</i2c write>

Broadcast write to Device 0 and Device 1 Bank 0 registers at Channel register 0x85 (Channel base register 0x80 + PD Override register 0ffset 0x05) with a value of 0x7F to **power on** all channels.

- <I2c_srite addr= "0x18" count = "0" radix"16">85 7F</i2c write>
- <I2c_srite addr= "0x1A" count = "0" radix"16">85 7F</i2c write>

7.2 Broadcast Channel CTLE Index or Flat Gain Selection Through Register Programming (CTLE Index 2, Flat Gain 0dB)

To select CTLE index 2 with Flat Gain of 0dB on all channels:

Broadcast write to Device 0 and Device 1 Bank 0 registers at Channel register 0x81 (Channel base register 0x80 + EQ Control register 0ffset 0x01) with a value of 0x98.Broadcast write to Device 0 and Device 1 Bank 0 registers at Channel register 0x83 (Channel base register 0x80 + EQ/Gain Control register 0ffset 0x03) with a value of 0x05

- <I2c_srite addr= "0x18" count = "0" radix"16">81 98</i2c write>
- <I2c_srite addr= "0x18" count = "0" radix"16">83 05</i2c write>
- <I2c_srite addr= "0x1A" count = "0" radix"16">81 98</i2c write>
- <I2c_srite addr= "0x1A" count = "0" radix"16">83 05</i2c write>

7.3 Individual Channel CTLE Index or Flat Gain Selection Through Register Programming (CTLE Index 2, Flat Gain 0dB)

To select CTLE Index 2 with Flat Gain of 0dB on a single channel (Channel 0):

Write to Channel 0 register on Device 0 Bank 0 and Device 1 Bank 0 registers at Channel register 0x01 (Channel 0 base register 0x00 + EQ Control register 0ffset 0x01) with a value of 0x98. – Write to Channel 0 register on Device 0 Bank 0 and Device 1 Bank 0 registers at Channel register 0x03 (Channel 0 base register 0x00 + EQ/Gain Control register 0ffset 0x03) with a value of 0x05

- <I2c_srite addr= "0x18" count = "0" radix"16">01 98</i2c write>
- <I2c_srite addr= "0x18" count = "0" radix"16">03 05</i2c write>
- <I2c_srite addr= "0x1A" count = "0" radix"16">01 98</i2c write>
- <I2c_srite addr= "0x1A" count = "0" radix"16">03 05</i2c write>

8 Summary

This configuration guide provides the tools needed to setup and configure the TDP2004 in your system. Please refer to this documentation alongside the *TDP2004 Four-Channel 20Gbps DisplayPort 2.1 Linear Redriver*, data sheet, TDP2004 Schematic Checklist, and the *DS320PR410 Programming Guide.* for further information.

9 References

- Texas Instruments, *TDP2004 Schematic Checklist*, application note.
- Texas Instruments: *TDP2004 Four-Channel 20Gbps DisplayPort 2.1 Linear Redriver*, data sheet.
- Texas Instruments: *DS320PR410 Programming Guide.*

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