Application Note

DP83869 Troubleshooting Guide

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ABSTRACT

DP83869HM is a robust, fully-featured gigabit physical layer (PHY) transceiver. *Understanding different modes of operation in DP83869* describes each mode of the DP83869HM in greater detail. This application note was created to help troubleshoot the DP83869HM in a design and to show what to look at in the event that the PHY is not working as intended.

Table of Contents

1 DP83869 Application Overview 2
2 Troubleshooting the Application 3
2.1 Configuring Correct Operational Mode 3
2.2 Schematic and Layout Checklist 3
2.3 Component Checklist 4
2.4 Peripheral Pin Checks 5
2.5 Built-In Self Test with Various Loopback Modes 9
2.6 Debugging MAC Interface 10
3 Operational Mode Clarification 15
3.1 Bridge Modes 15
3.2 Fiber Configuration 16
4 Tools and References 17
4.1 DP83869HM Register Access 17
4.2 Extended Register Access 18
4.3 Software and Driver Debug on Linux 20
5 Summary 21
6 References 22

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1 DP83869 Application Overview

The DP83869HM device is a robust, fully-featured gigabit physical layer (PHY) transceiver with integrated PMD sublayers that supports 10BASE-Te, 100BASE-TX, and 1000BASE-T Ethernet protocols. The DP83869 also supports 1000BASE-X and 100BASE-FX fiber protocols.

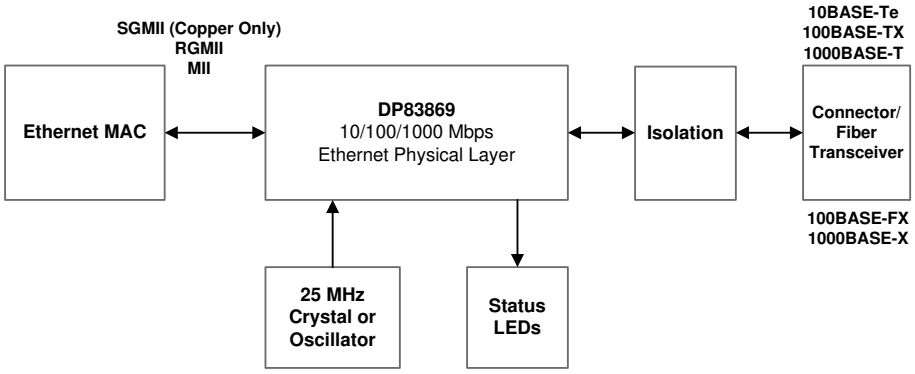

Figure 1-1. Standard Ethernet System Block Diagram

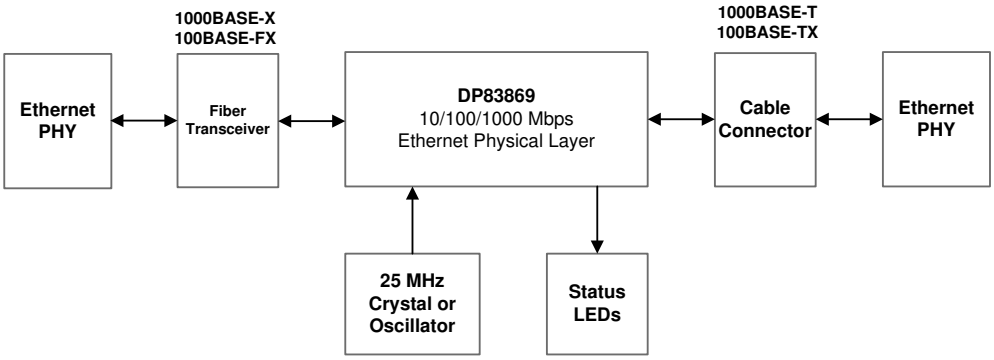

Figure 1-2. Media Convertor System Block Diagram

2 Troubleshooting the Application

The following sections approach the debug from a high level, attempting to start with application characteristics that have a broad impact and then zeroing in on more focused aspects of the design.

2.1 Configuring Correct Operational Mode

The operational mode of the DP83869HM is configured through the OPMODE[0], OPMODE[1], and OPMODE[2] straps. A brief summary of each OPMODE configuration is provided in Table 2-1. More information can be found in the *Programming* section of the data sheet.

To verify DP83869HM's operational mode, register 0x6E can be read to confirm. If register 0x6E does not match your intended hardware straps configuration, something in the system is causing the PHY to strap into the incorrect mode. Make sure lines for GPIO_1, RX_D3, and RX_D2 (pins responsible for OPMODE[0..2] respectively) are silent during PHY boot up.

Register 0x6E is read-only, meaning the Operational Mode cannot be changed by writing to this register. Software configuration of the DP83869HM is possible through register 0x1DF which allows writes to configure the OPMODE. Some operational modes require more register writes than just register 0x1DF, this information is provided in the *Register Configuration for Operational Modes* Section in the data sheet.

Note

Registers 0x6E and 0x1DF are extended registers and cannot be accessed directly. Please reference Section 4.2.

Table 2-1. Functional Mode Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	OPMODE[2]	OPMODE[1]	OPMODE[0]	FUNCTIONAL MODES
JTAG_TDO/ GPIO_1	OPMODE[0]	22	0	0	0	0	RGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				0	0	1	RGMII to 1000Base-X
RX_D3	OPMODE[1]	36	0	0	1	0	RGMII to 100Base-FX
				0	1	1	RGMII-SGMII Bridge Mode
RX_D2	OPMODE[2]	35	0	1	0	0	1000Base-T to 1000Base-X
				1	0	1	100Base-Tx to 100Base-FX
				1	1	0	SGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				1	1	1	JTAG for boundary scan

2.2 Schematic and Layout Checklist

Reference schematic and layout recommendations checklists that can be found on the product page:

DP83869HM Product Page

2.3 Component Checklist

Magnetics:

The following guidelines are the main specifications to reference for compatible magnetics:

Table 2-2. Magnetic Electrical Specification

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turns Ratio	±2% Tolerance	1:1	-
Insertion Loss	1-100 MHz	-1	dB
Return Loss	1-30 MHz	-16	dB
	30-60 MHz	-12	dB
	60-80 MHz	-10	dB
Differential to Common Mode Rejection	1-50 MHz	-30	dB
	60-150 MHz	-20	dB
Crosstalk	30 MHz	-35	dB
	60 MHz	-30	dB
Open Circuit Inductance	8-mA DC Bias	350	µH
Isolation	HPOT	1500	Vrms

- Turns Ratio
  - Ideally 2% but 3% is tolerable
- Insertion Loss
  - As close to 0 dB as possible
- Return Loss
  - At or smaller magnitude than specified in Table 2-2
    - If specification gives -16 dB typical, finding a component with -16 dB, -17 dB is recommended.

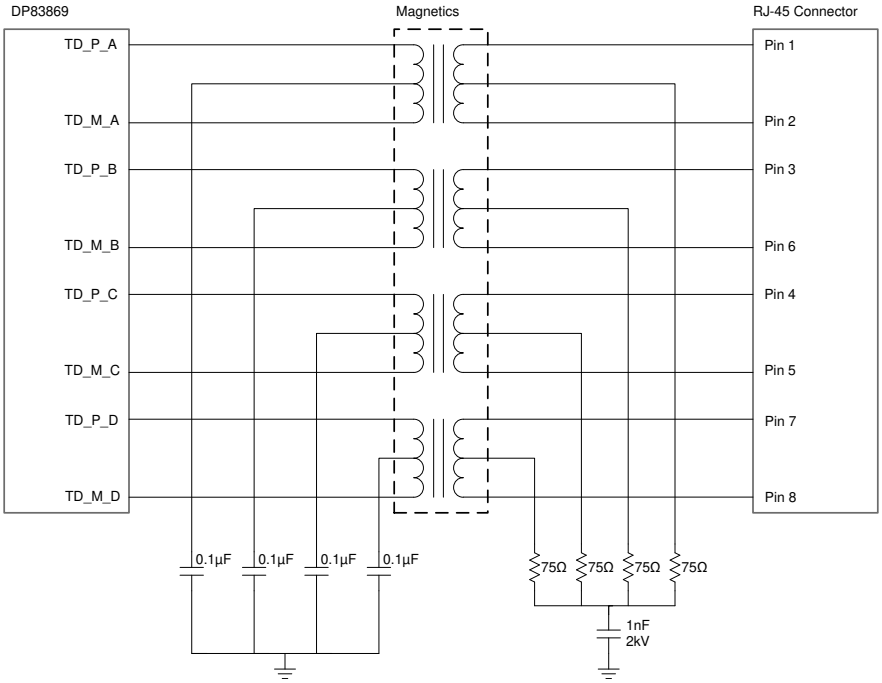

Figure 2-1. PHY to RJ45 and Magnetics

- Each center tap on the side connected to the PHY must be isolated from one another and connected to ground by a decoupling capacitor (0.1 µF recommended).
- Pulse Electronics part, HX5008FNL is recommended for a discrete magnetics solution.

Crystal or Oscillator

The following guidelines are the main specifications to reference for compatible crystals and oscillators:

Table 2-3. 25-MHz Crystal Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Including operational temperature, aging, and other factors			±100	ppm
Load Capacitance		15		40	pF
ESR				50	ohm

Table 2-4. 25-MHz Oscillator Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational temperature, 1 year aging			±100	ppm
Rise and Fall Time	20% - 80%			5	ns
Symmetry	Duty cycle	40%		60%	

2.4 Peripheral Pin Checks

The following section details the expected values of various peripheral output pins of the PHY during operation. Measure and compare the noted pin outputs to verify PHY operation.

2.4.1 Power Supplies

The power supplies are the first key item to check. Power up the device and perform DC measurement of the supplies as close to the pin as possible. Confirm that each measurement is within the limits defined in the *Recommended Operating Conditions* section of the data sheet.

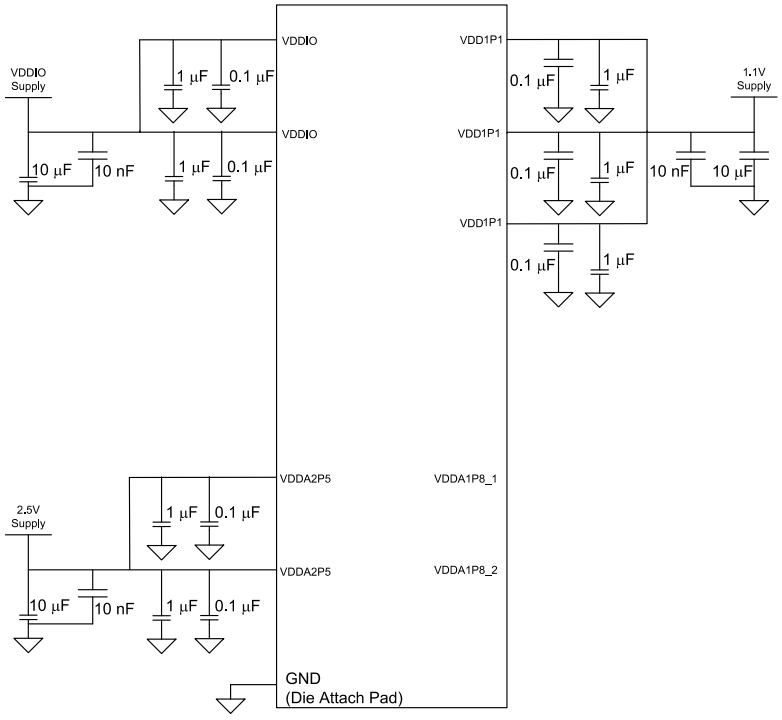

Figure 2-2. Two-Supply Configuration

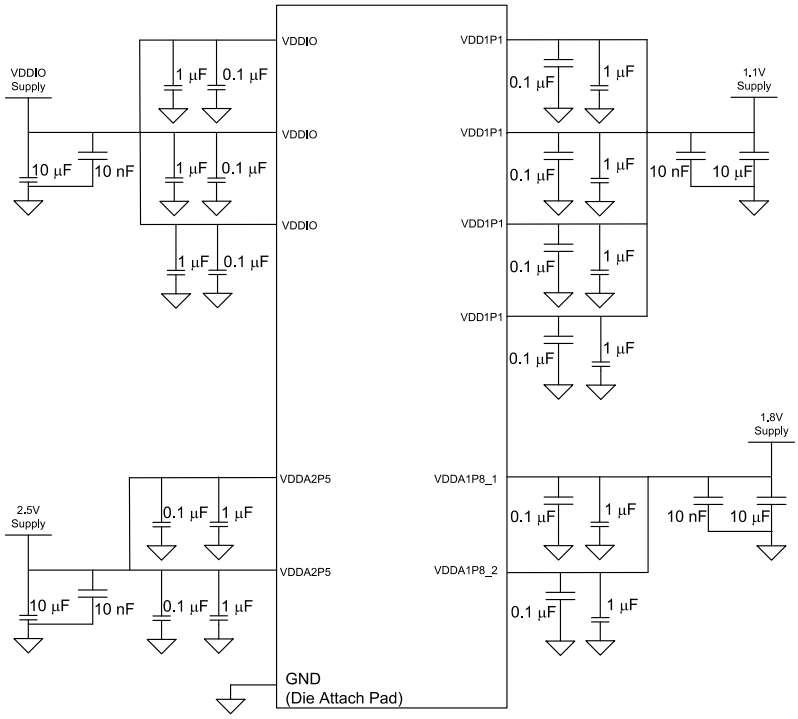

Figure 2-3. Three-Supply Configuration

The DP83869 supports the two configurations for power supplies as shown in Figure 2-2 and Figure 2-3.

When operating in the three supply configuration, our recommendation is to power all supplies together. If powering all supplies simultaneously is not possible, then power VDD1P1 and VDD2P5 first with VDDIO and VDD1P8 following within 50 ms. Place 1-µF and 0.1-µF decoupling capacitors as close as possible to component VDD pins, placing the 0.1-µF capacitor closest to the pin.

When operating in the two supply configuration, leave both VDDA1P8 pins disconnected and power all supplies together. If powering all supplies simultaneously is not possible, then power VDDA2P5 and VDD1P1 first with VDDIO following within 50 ms. Place 1-µF and 0.1-µF decoupling capacitors as close as possible to component VDD pins, placing the 0.1-µF capacitor closest to the pin.

2.4.2 RBIAS Voltage and Resistance

The RBIAS resistor is used to develop the internal bias currents and voltages in the PHY. The resistor is specified for 1% tolerance so that the PHY can meet the strictest IEEE 802.3 specifications.

Measure the DC value of the voltage across the RBIAS resistor and confirm that the voltage is 1 V.

Power down the board and verify that the RBIAS resistor value is 11 kΩ ±1%.

2.4.3 Probe the XI Clock

Verify the frequency and signal integrity. For link integrity the clock must be 25 MHz ±50 ppm. If using a crystal as the clock source, probe the CLK_OUT signal. Probing the crystal can change the capacitive loading therefore changing the operational frequency. The default signal on CLK_OUT is a buffered version of the XI reference and provides a representative measurement.

2.4.4 Probe the RESET_N Signal

The reset input is active low. Confirm that the controller is not driving the RESET_N signal low; otherwise, the device is held in reset and can not respond.

2.4.5 Probe the Strap Pins During Initialization

In some cases, other devices on the board (for example, the MAC) pull or drive these pins unexpectedly. Confirm that these signals are in the range of the target voltages described in the data sheet. Measurements can be made during power up and after power up when the RESET_N signal is asserted.

For further confirmation, the strap values can be read from the registers. The values are available in register 0x006E (STRAP_STS).

Note

Register 0x6E is an extended register and cannot be accessed directly. Please reference Section 4.2.

2.4.6 Probe the Serial Management Interface Signals (MDC, MDIO)

MDIO requires a 2.2 kΩ pull-up to the I/O supply when undriven. Probe MDIO to confirm the default voltage. Attempt to read the registers. Probe the MDC/MDIO signals during read and write operations, referencing the expected waveforms below:

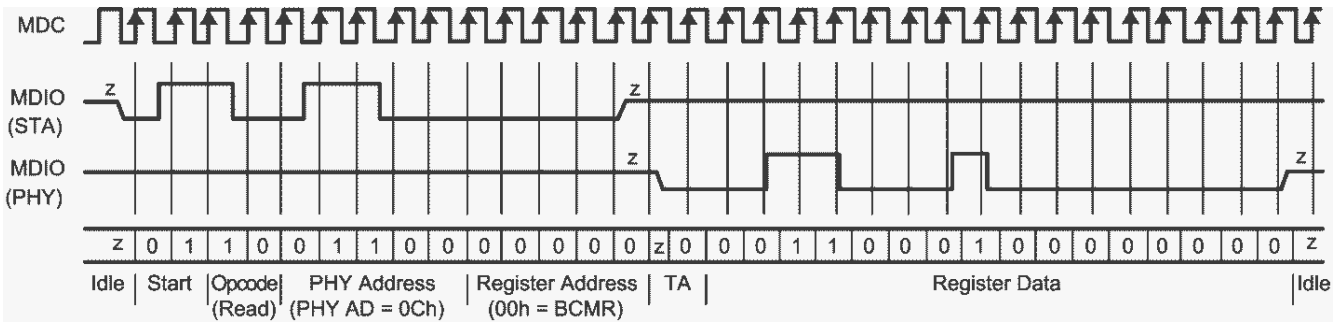

Figure 2-4. Typical MDC/MDIO Read Operation

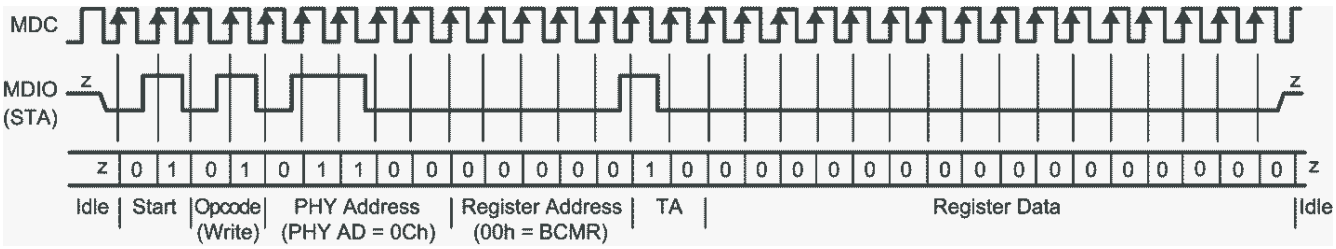

Figure 2-5. Typical MDC/MDIO Write Operation

2.4.7 Probe the MDI Signals

The DP83869 has four differential pairs to send data:

- TD_P_A | TD_M_A
- TD_P_B | TD_M_B
- TD_P_C | TD_M_C
- TD_P_D | TD_M_D

In OpMode: 000, RGMII to Copper, probing a channel allows you to see the link pulse which confirms the PHY is on and is attempting to link.

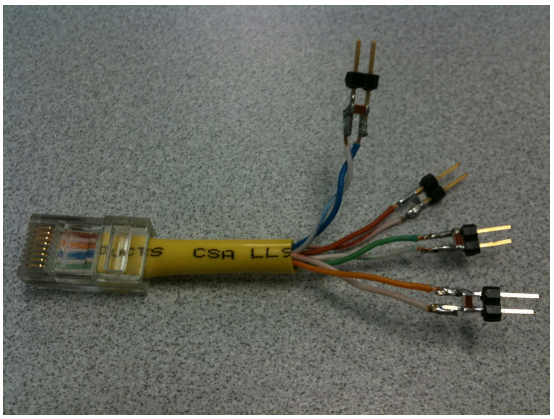

Figure 2-6. 100 Ohm Terminated Cable for MDI Signal Measurement

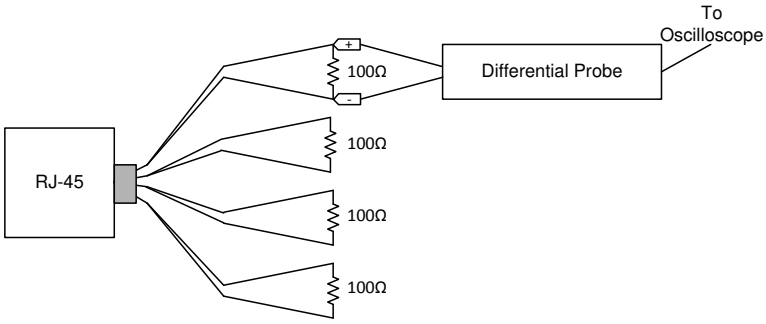

Figure 2-7. Connection Diagram for 1000M Terminated Cable

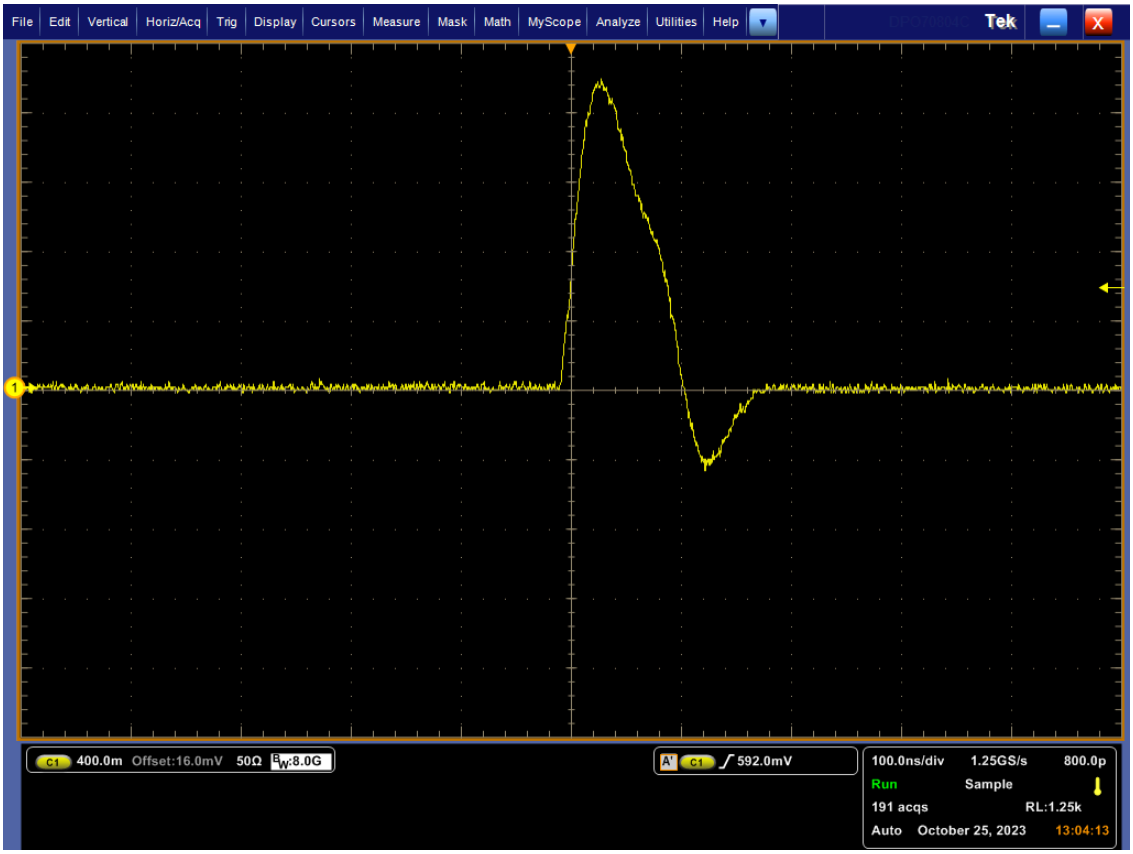

Figure 2-8. Link Pulse Waveform

2.5 Built-In Self Test with Various Loopback Modes

There are several options for loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the digital and analog data paths. Generally, the DP83869HM can be configured to one of the near-end loopback modes or to the far-end (reverse) loopback. The *Loopback Mode* section in the data sheet provides additional details on loopbacks and how to configure them.

The availability of Loopback depends on the operational mode of the PHY. The Link Status in these loopback modes is also effected by the operational mode. Table 2-5 lists out the exceptions where Loopbacks are not available.

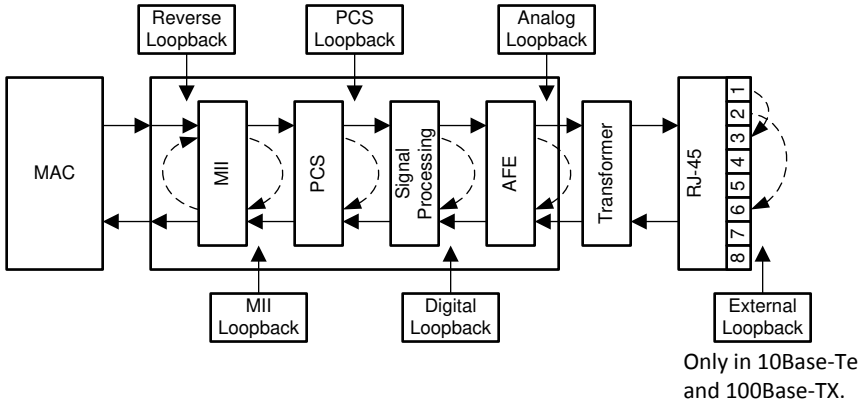

Figure 2-9. Loopbacks

Table 2-5. Loopback Availability Exception

OP MODE	LOOPBACK	EXCEPTION
Copper	PCS	10M
Fiber	MII	100M
	PCS	100M
	Analog	100M, 1000M
SGMII to RGMII	PCS	10M, 100M, 1000M
	Digital	10M, 100M, 1000M
	Analog	10M, 100M, 1000M
	External	10M, 100M, 1000M
RGMII to SGMII	PCS	10M, 100M, 1000M
	External	10M, 100M, 1000M
Media Convertor	MII	100M, 1000M
	Analog	100M on Fiber Interface
	External	100M on Fiber Interface
		100M, 1000M on Copper Interface

2.6 Debugging MAC Interface

2.6.1 RGMII

Reference the waveforms in this section to verify the expected MAC data and clock signals for RGMII in shift and align modes. To capture data and clock signals, measure close to the receiver end. Note the following requirements for selecting the correct delay mode:

Table 2-6. Selecting the Correct RGMII Delay Mode

If MAC's Configuration is:	Required PHY Configuration
RGMII Align Mode on TX side	RGMII Shift Mode on TX side
RGMII Align Mode on RX side	RGMII Shift Mode on RX side
RGMII Shift Mode on TX side	RGMII Align Mode on TX side
RGMII Shift Mode on RX side	RGMII Align Mode on RX side

RX_D[3:0] Data Aligned with RX_CLK

For the PHY set in RX align mode in 10/100Mbps, probe the clock and data signals on the MAC end and compare to the reference waveforms shown below.

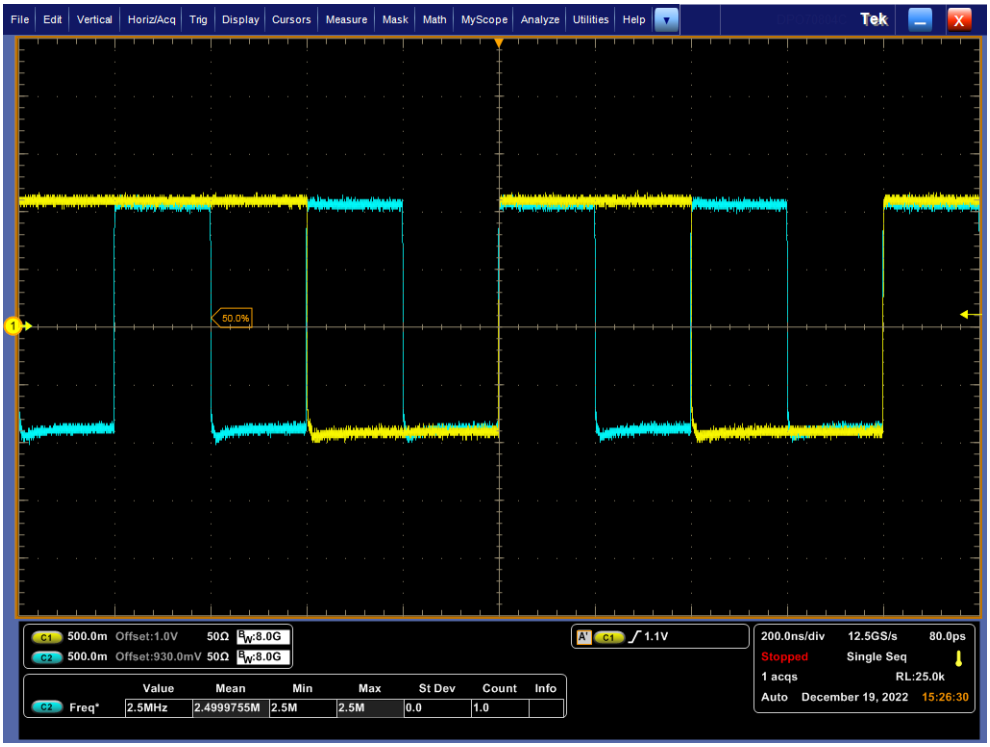

Figure 2-10. 10Mbps Data Aligned With RX_CLK

Verify the frequency of the clock (C2) as 2.5 MHz and the data (C1) being sampled at the rising edge of the clock.

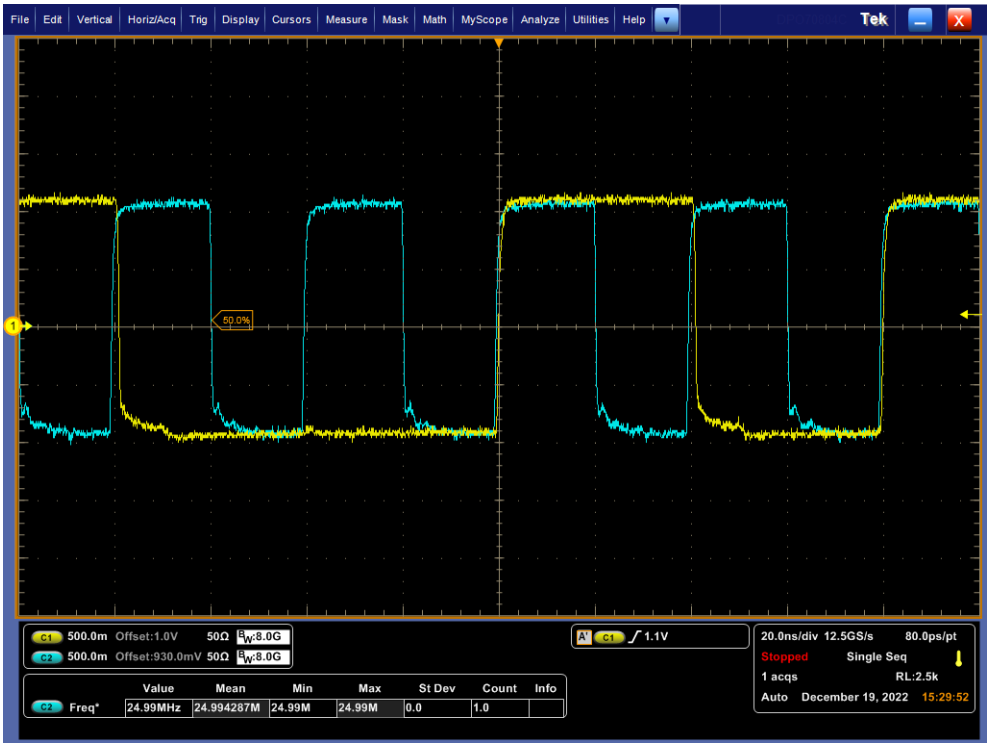

Figure 2-11. 100Mbps Data Aligned With RX_CLK

Verify the frequency of the clock (C2) as 25 MHz and the data (C1) being sampled at the rising edge of the clock.

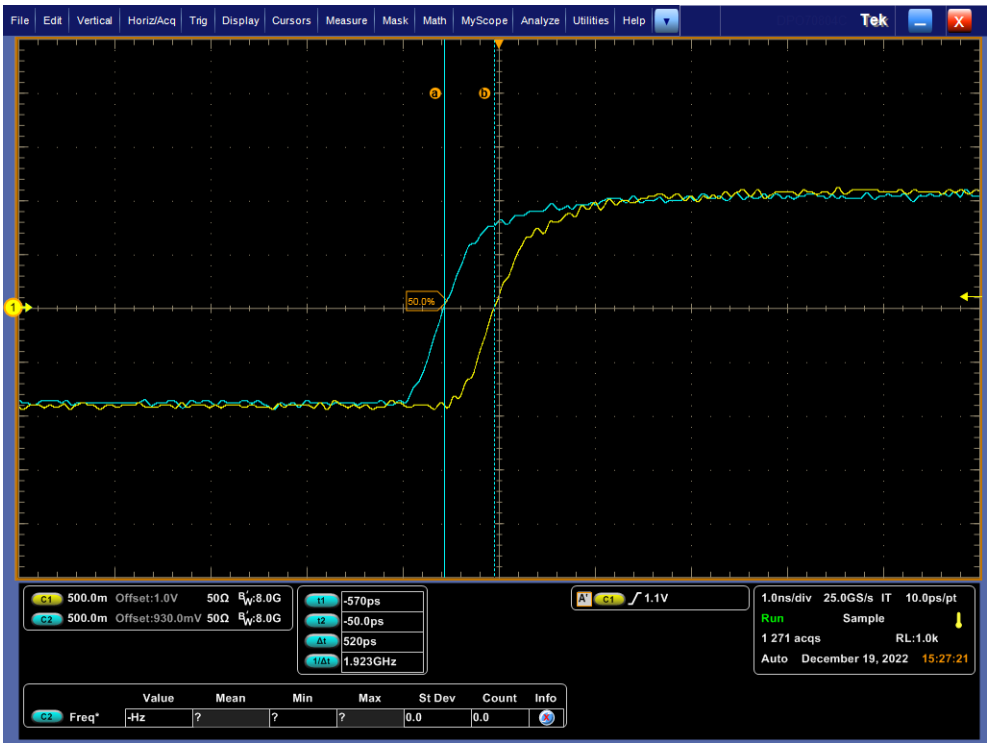

Figure 2-12. 10Mbps Data and Clock Delay in Align Mode

Verify the delay between clock and data is <500ps in align mode.

RX_D[3:0] Data and RX_CLK in Shift Mode

For the PHY set in RX shift mode (0x32) in 10/100Mbps, probe the clock and data signals on the MAC end and compare to the following reference waveforms.

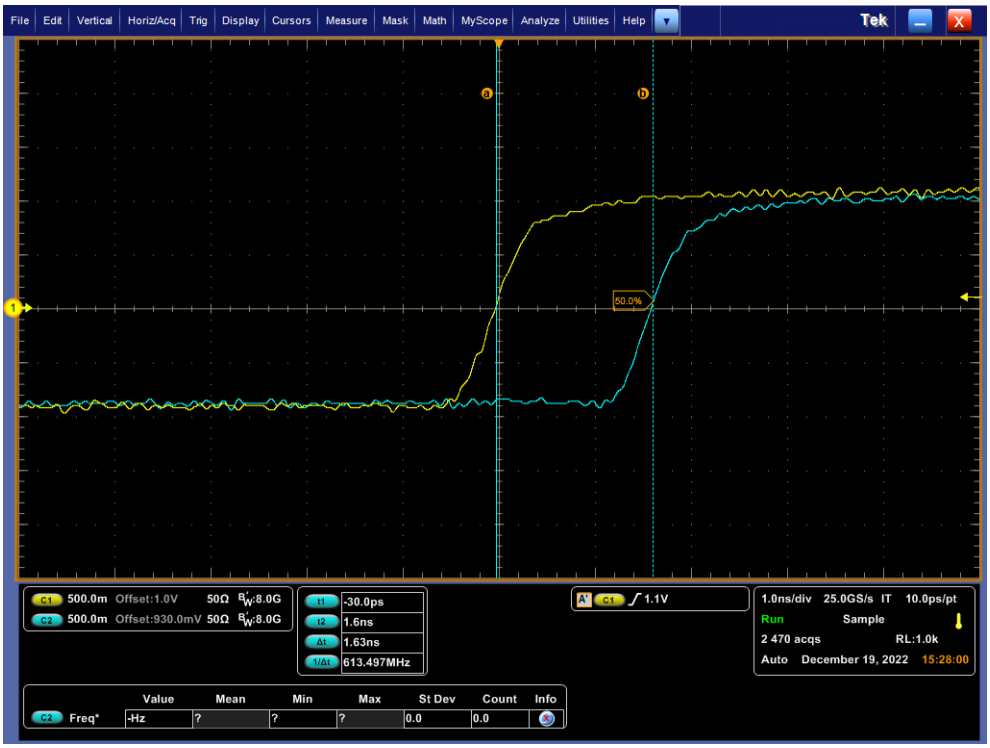

Figure 2-13. 10Mbps Data and RX_CLK in Shift Mode (4ns Programmed Delay)

Verify the delay between clock and data is >1ns in shift mode. The programmed delay is relative to the clock's initial position in aligned mode. Measuring the difference in the clock's position before and after setting shift mode yields a value closer to the programmed delay.

TX_D[3:0] and TX_CLK in Shift and Align Mode

With the PHY set in TX shift or align mode, probe the data and clock signals on the PHY end and verify the timing requirements below are met:

PARAMETER		MIN	NOM	MAX	UNIT
T_{skewT}	Data to Clock output Skew (at Transmitter)	–500	0	500	ps
T_{skewR}	Data to Clock input Skew (at Receiver)	1	1.8	2.6	ns
T_{setupT}	Data to Clock output Setup (at Transmitter – internal delay)	1.2	2		ns
T_{holdT}	Clock to Data output Hold (at Transmitter – internal delay)	1.2	2		ns
T_{setupR}	Data to Clock input Setup (at Reciever – internal delay)	1	2		ns
T_{holdR}	Clock to Data input Hold (at Receiver – internal delay)	1	2		ns
T_{cyc}	Clock Cycle Duration	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit	45	50	55%	
Duty_T	Duty Cycle for 10/100T	40	50	60%	
T_R	Rise Time (20% to 80%)			0.75	ns
T_F	Fall Time (20% to 80%)			0.75	ns

2.6.2 SGMII

The Serial Gigabit Media Independent Interface (SGMII) provides a means of conveying network data and port speed between a 100/1000 PHY and a MAC with significantly less signal pins (4 or 6 pins) than required for GMII (24 pins) or RGMII (12 pins). The SGMII interface uses 1.25-Gbps LVDS differential signaling which has the added benefit of reducing EMI emissions relative to GMII or RGMII.

The SGMII interface includes Auto-Negotiation capability. Auto-Negotiation provides a mechanism for control information to be exchanged between the PHY and the MAC. This allows the interface to be automatically configured based on the media speed mode resolution on the MDI side. SGMII Auto-Negotiation is the default mode of the operation but can be disabled by writing register 0x14[7] = 0.

The SGMII Output spec included in the data sheet states an Output Differential Voltage which refers to the Peak-to-Peak, SO_P - SO_N. This means that the SO_P and SO_N signals are roughly ±0.55 V each.

Table 2-7. SGMII Output Spec

SGMII Output		Min	Typ	Max	Unit
Output Differential Voltage	SO_P and SO_N, AC Coupled	0.95	1.00	1.05	V

All SGMII connections must be AC-coupled through a 0.1-µF capacitor.

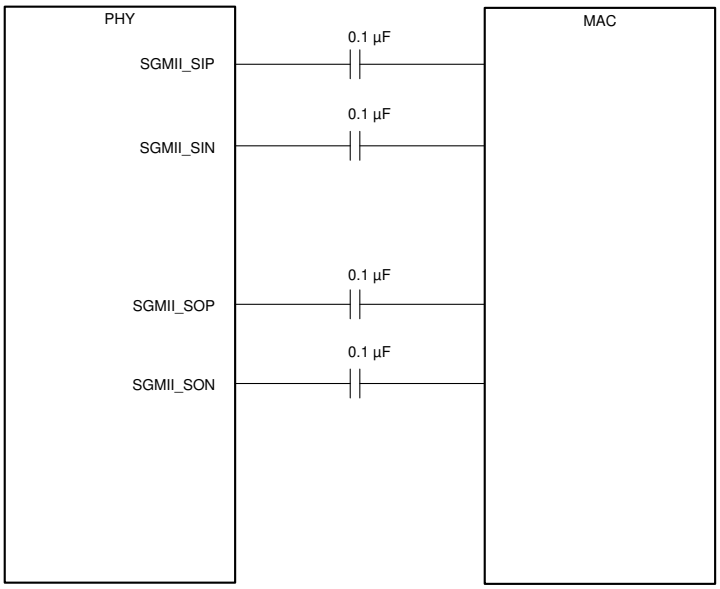

Figure 2-14. SGMII 4-Wire Connections

3 Operational Mode Clarification

While the data sheet offers sufficient information, this section is a condensed version to help understand how to properly use and configure these modes.

3.1 Bridge Modes

The DP83869HM supports two types of Bridge Modes to translate data between two MAC interface types. The two types are:

- RGMII-to-SGMII mode
- SGMII-to-RGMII mode

The naming convention implies MAC-to-PHY and the functionality of the DP83869HM changes depending on which mode is selected. More information can be found in the *Bridge Modes* section of the data sheet.

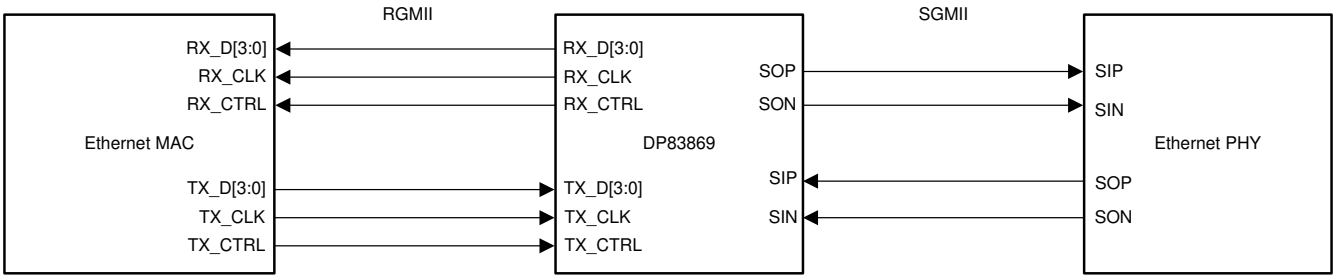

Figure 3-1. DP83869HM RGMII-to-SGMII Bridge

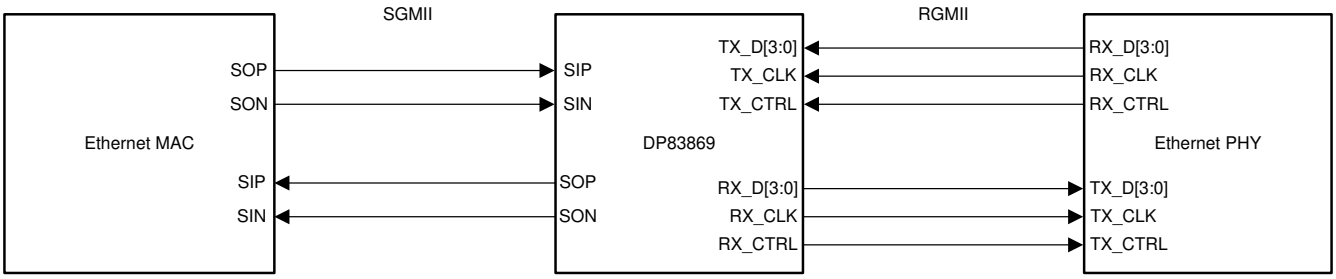

Figure 3-2. DP83869HM SGMII-to-RGMII Bridge

3.2 Fiber Configuration

DP83869HM is capable of 100Base-FX and 1000Base-X fiber communication. When using fiber, speed is not determined by auto-negotiation. Both sides of the link must be configured to the same operating speed. The pins used for fiber are also the same pins used for SGMII: SIP/SIN and SOP/SON. The DP83869HM must be set to either *SGMII to Copper* or *RGMII/MII to fiber*. A SGMII to fiber connection is not possible.

Table 3-1. Differential SGMII or Fiber Data Pins Description

Pin		I/O	Type	Description
NO.	Name			
14	SON	O	Analog	Differential SGMII or Fiber Data Output: This signal carries data from the PHY to the MAC, fiber transceiver, or link partner in SGMII and fiber modes. This pin is AC-coupled to the distant device through a 0.1-µF capacitor. This pin provides LVDS signals. Additional components can be required for the optical transceiver.
15	SOP	O	Analog	
16	SIP	I	Analog	Differential SGMII or Fiber Data Input: This signal carries data from the MAC, fiber transceiver, or link partner, to the PHY in SGMII and fiber modes. This pin is AC-coupled to the distant device through a 0.1-µF capacitor. This pin accepts LVDS signals. Additional components can be required for the optical transceiver.
17	SIN	I	Analog	

3.2.1 Fiber Registers

DP83869HM has several fiber related registers, this section is intended to summarize a few of their functionalities and show how to debug. Link status can always be checked in register 0x01, but register 0xC01 checks Fiber link.

Table 3-2. Register 0xC01 Behavior

Mode	Register 0xC01 behavior
RGMII to Fiber	Behaves the same as register 0x01, meaning there is no added benefit of reading register 0xC01
Media Convertor Mode	**Case 1:** Copper link is down but Fiber link is up Register 0x01 indicates link is down (copper side), but register 0xC01 shows link is up (fiber side). This is helpful for being able to debug which cable is at fault. **Case 2:** Copper link is up but Fiber link is down Register 0x01 indicates link is down. If register 0xC01 says link is down, register 0x01 is also down.

Case 2 in Table 3-2 does not give full confidence in which link is down. The Fiber Interrupt Status Register (0xC19) can be used to isolate where the fault is. In Case 2, 0xC19[9] (Fiber Far End Fault) and 0xC19[4] (Link Status Change) can flag. In Case 1, only 0xC19[4] can flag.

4 Tools and References

The following chapter contains additional tools and references relevant for debugs.

4.1 DP83869HM Register Access

If register access is not readily available in the application, USB-2-MDIO GUI is available from TI and can be used with an MSP430™ Launchpad, purchasable through the TI eStore. The GUI supports reading and writing registers, running script files, and can be used with the DP83869HM and the other devices in TI's Ethernet portfolio. USB-2-MDIO User's Guide and GUI are available for download.

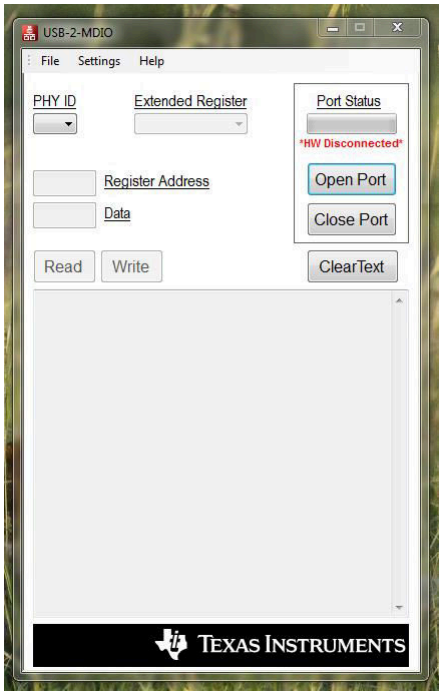

Figure 4-1. USB-2-MDIO GUI

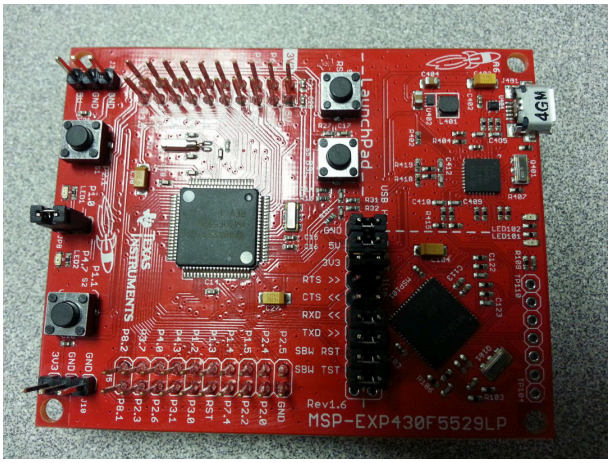

Figure 4-2. MSP430 LaunchPad

Below is an example script that can also be found in the USB-2-MDIO GUI in the Help menu:

```
// This is how you make a comment. All scripts must start with 'begin'
begin
// To read a register, all you need to do is put down the 4 digit
// HEX value of the registers (from 0000 to FFFF)
// Example to read registers 0001, 000A, and 0017
0001
000A
0017
// To write a register, all you need to do is put down the 4 digit
// HEX value of the register (from 0000 to FFFF) followed by the
// HEX you desire to configure the register to (from 0000 to FFFF)
// Example to write 2100 to register 0000 and
// Example to write 0110 to register 0016
0000 2100
0016 0110
// You must end the script by adding 'end' once you are finished
end
```

The Serial Management Interface defined by IEEE 802.3 is a single master bus. The MDC clock is generated by the bus master, typically an Ethernet MAC. To use the USB-2-MDIO GUI, connections must be made directly between the MSP430 Launchpad and the DP83867 MDIO and MDC pins. Specifically, pins 4.1 to MDC, 4.2 to MDIO, and any GND to the ground of the PHY allows the MSP to read and write the PHY's registers by USB-2-MDIO.

4.2 Extended Register Access

The DP83869HM's Serial Management Interface (SMI) function supports read or write access to the extended register set using registers REGCR (0x0D) and ADDAR (0x0E) and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah Draft for clause 22 for accessing the clause 45 extended register set.

The standard register set, MDIO registers 0 to 31, is accessed using the normal direct-MDIO access or the indirect method, except for register REGCR (0x0D) and ADDAR (0x0E), which is accessed only using the normal MDIO transaction. The SMI function ignores indirect accesses to these registers.

REGCR (0x0D) is the MDIO Manageable MMD access control. In general, register REGCR(4:0) is the device address DEVAD that directs any accesses of ADDAR (0x0E) register to the appropriate MMD.

The PHY'S supports one MMD device address. The vendor-specific device address DEVAD[4:0] = 11111 is used for general MMD register accesses.

All accesses through registers REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVAD are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10), and data with post increment on writes only (11).

Table 4-1. REGCR DEVAD Functions

REGCR[15:14]	Function
00	Accesses to register ADDAR modify the extended register 'set address' register. This address register must always be initialized to access any of the registers within the extended register set.
01	Accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
10	Access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
11	Access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write accesses only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR. The descriptions use the device address for general MMD register accesses (DEVAD[4:0] = 11111).

4.2.1 Read (No Post Increment) Operation

To read a register in the extended register set:

Instruction	Example: Read 0x0170
1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x001F
2. Write the desired register address to register ADDAR.	Write register 0x0E to value 0x0170
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x401F
4. Read the content of the desired extended register set register to register ADDAR.	Read register 0x0E

Subsequent reads from register ADDAR (step 4) continue reading the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

4.2.2 Write (No Post Increment) Operation

To write a register in the extended register set:

Instruction	Example: Set reg 0x0170 = 0C50
1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR (0x0D).	Write register 0x0D to value 0x001F
2. Write the desired register address to register ADDAR (0x0E).	Write register 0x0E to value 0x0170
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x401F
4. Write the content of the desired extended register set register to register ADDAR.	Write register 0x0E to value 0x0C50

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

4.3 Software and Driver Debug on Linux

The two essential components required for the PHY to function on a Linux system are the device tree and driver file, for which the DP83869HM drivers can be found here. Below is a sample format of what a device tree looks like. This can be found on any open source kernal under the following path: root/Documentation/devicetree/bindings/net/ti.

```
#include <dt-bindings/net/ti-dp83869.h>
   mdio0 {
     #address-cells = <1>;
     #size-cells = <0>;
     ethphy0: ethernet-phy@0 {
       reg = <0>;
       tx-fifo-depth = <DP83869_PHYCR_FIFO_DEPTH_4_B_NIB>;
       rx-fifo-depth = <DP83869_PHYCR_FIFO_DEPTH_4_B_NIB>;
       ti,op-mode = <DP83869_RGMII_COPPER_ETHERNET>;
       ti,max-output-impedance;
       ti,clk-output-sel = <DP83869_CLK_O_SEL_CHN_A_RCLK>;
       rx-internal-delay-ps = <2000>;
       tx-internal-delay-ps = <2000>;
     };
   };
```

4.3.1 Common Terminal Outputs

The following section is intended to provide common terminal commands that can be used to debug driver related issues.

```
$ dmesg | grep "mdio"
```

One of the possible outputs is as follows:

```
$ mdio_bus xxx.ethernet-x: MDIO device at address 8 is missing
```

This message indicates that the PHY is not found on the MDIO bus, which can be caused by several issues. The most common one being a missing or incorrect device tree, but can also be due to a non-functional PHY or a bad SMI connection.

Once the PHY can be detected on the MDIO bus, another common error message is as follows:

```
$ Generic PHY xxx.ethernet-x: attached PHY driver [Generic PHY]
```

This message indicates that the driver file for the corresponding PHY is not loaded correctly or not present at all, and Linux loaded in a generic driver that most likely won't work with the PHY. In that case, verify that the driver successfully compiled, was added when building Linux, and that the driver matches with the model of PHY used.

Finally, a message like this can display:

```
am65-cpsw-nuss 8000000.ethernet eth1: PHY [mdio_mux-0.1:03] driver [TI DP83869] (irq=POLL)
```

This message shows that the PHY has the correct driver loaded and is detected successfully. Run *ifconfig* to verify the network interface is present. Example *ifconfig* output when the PHYs are successfully recognized as network adapters:

```
root@am64xx-evm:~# ifconfig
eth0: flags=4099<UP,BROADCAST,MULTICAST>  mtu 1500
        ether 34:08:e1:80:b5:f8  txqueuelen 1000  (Ethernet)
        RX packets 0  bytes 0 (0.0 B)
        RX errors 0  dropped 0  overruns 0  frame 0
        TX packets 0  bytes 0 (0.0 B)
        TX errors 0  dropped 0 overruns 0  carrier 0  collisions 0

eth1: flags=4099<UP,BROADCAST,MULTICAST>  mtu 1500
        ether 70:ff:76:1e:9e:a6  txqueuelen 1000  (Ethernet)
        RX packets 0  bytes 0 (0.0 B)
        RX errors 0  dropped 0  overruns 0  frame 0
        TX packets 0  bytes 0 (0.0 B)
        TX errors 0  dropped 0 overruns 0  carrier 0  collisions 0

lo: flags=73<UP,LOOPBACK,RUNNING>  mtu 65536
        inet 127.0.0.1  netmask 255.0.0.0
        loop  txqueuelen 1000  (Local Loopback)
        RX packets 90  bytes 6824 (6.6 KiB)
        RX errors 0  dropped 0  overruns 0  frame 0
        TX packets 90  bytes 6824 (6.6 KiB)
        TX errors 0  dropped 0 overruns 0  carrier 0  collisions 0
```

5 Summary

This application note provides a suggested flow for evaluating a new application and confirming the expected functionality. The step-by-step recommendations helps ease board bring-up and initial evaluation of DP83869HM designs.

6 References

- Texas Instruments, DP83869HM product page.
- Texas Instruments,*DP83869HM High Immunity 10/100/1000 Ethernet Physical Layer Transceiver With Copper and Fiber Interface* data sheet.
- Texas Instruments, Understanding the different modes of operation in DP83869HM application report.

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