Application Note

EMC/EMI Compliant Design for Single Pair Ethernet

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ABSTRACT

This application note provides guidance for good schematic and layout practices for passing EMI and EMC tests. The publication focuses on the often neglected aspects of power supply and clocking schemes. A special focus is also set on the requirements for singe pair Ethernet (SPE) with adding power over data lines (PoDL) on top, as this has additional requirements on the ripple voltage caused by the power supply on the data line.

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1 Introduction

Whenever designing a system, certain rules can be applied to create a system not emitting electromagnetic interference, but also to be robust against external emissions. This document summarizes good practices that can be kept in mind during schematic as well as layout design. The main focus point here is on single pair Ethernet, but some rules are also valid for standard Ethernet as well.

2 Power Supply

A very important aspect when looking at EMI is the power supply. The goal is to minimize noise on every supply rail for two reasons, noise can interfere with your circuit and causes ICs to not work properly, possibly even receiving brown outs, but also your supply line can bring the noise to the environment either by radiating (radiated emissions) or through wires (conducted emissions).

When looking at a typical block diagram of the power tree of a system, we can separate into the internal supply rails, for example all voltages going to processors, Ethernet Phys and everything that powers the system from external supply inputs. In Figure 2-1 these are the 24 V PoDL and 24 V Aux.

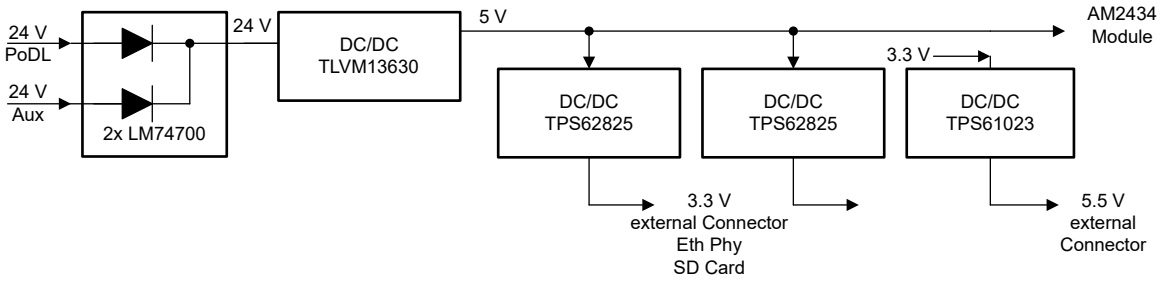

Figure 2-1. Power Supply Block Diagram

2.1 Internal Supply Rails

Internal supply rails are generated by local switching or linear regulators from higher voltages. The example shown here starts from external 24 V, generates an intermediate 5 V rail and finally 3.3 V and 1.8 V rails for different subsystems using switching regulators.

This document does not focus on how to design a switching regulator, keep in mind general rules about current loops and check the data sheets. Also the document does not cover the basics for linear regulators.

When implementing a supply for an Ethernet PHY, stick to the guidelines given in the data sheet, in terms of capacitors and filtering on the supply rails. Typically you want to have two to three capacitors with different capacitance per supply pin as well as some bulk capacitance. On top of this, the recommendation is to have the option for some low pass filtering. Figure 2-2 shows a set of capacitors per pin and with R77 and R78 the option for filtering is given. Multiple capacitors with different capacitance and sizes are used to get a low impedance over a wide frequency range. There also different physical sizes from 0402 (for very high frequencies also 0201 or smaller) up to 0805 can help.

During (pre-)compliance tests you can see if there is a need to add additional filtering, for example, by using ferrite beads. If there is noise visible, correlating to frequencies used inside the device, or you can measure a lot of HF current going through this resistor (a near field probe can help), it can help to add a ferrite bead to keep this noise away from the power planes.

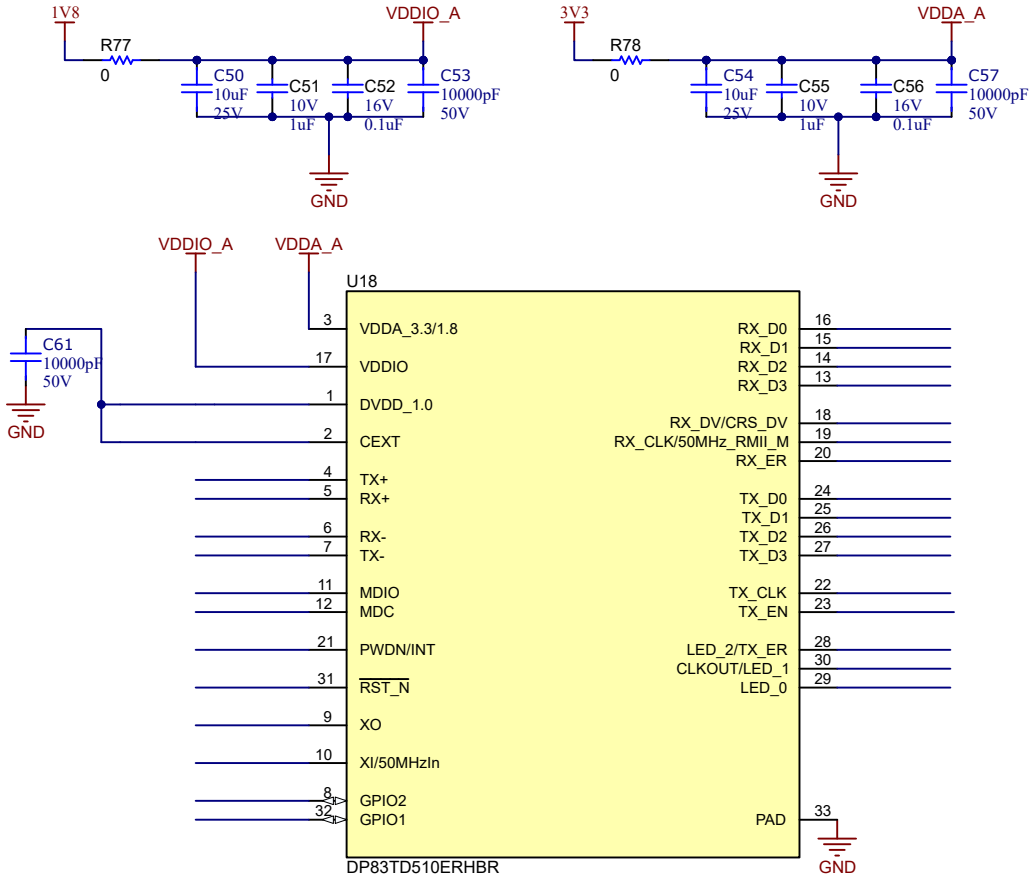

Figure 2-2. Power Supply Schematic

In terms of layout, there is an importance to have the components in the correct order and connected with wide and short traces. Every trace has parasitic elements, especially resistance, and inductance can be bad in this case. As a rule of thumb a trace of 1 cm has 10 nH of inductance. This does not sound much, but when looking at the impedance at 100 MHz, we have about 6 Ω, which is already significant. So a capacitor connected through a long and thin trace is useless for higher frequencies.

Also, the impedance of capacitors changes over frequency, as real capacitors have parasitics and do not behave like ideal capacitors. Typically, small capacitance are better designed for filtering high frequencies than high capacitance. Also, the physical size makes a difference, the smaller the better for high frequency, as the series inductance is lower. Also, stay away from through hole parts or electrolytic caps for filtering in this case.

Figure 2-3 shows the layout for this implementation, the trace from the pin is as short as possible and going to a bank of capacitors with increasing values. This bank is connected at the very end through a ferrite bead to the supply plane. Also think about the return path, every current going into a supply pins needs to go back somehow. This path also needs to provide a low impedance path to the same source. The typical approach of having a solid GND plane is a good design, when you also connect the return path of the IC and of the caps in a solid way. This means to have a set of vias as close as possible. Here you are limited by the manufacturing capabilities you want to pay for. Stay away from pads, so the vias and the pad are separated by the solder mask otherwise you can have problems when manufacturing the board. If you really want to have the vias in the pads, talk to your manufacturer upfront about this.

In some cases it can be necessary to have the capacitor on the other side of the PCB directly below the IC. This is also a good approach, but again, the via adds some inductance, a 0.2 mm vias in a 1.6 mm PCB has about 1 nH, so similar to 1 mm PCB trace.

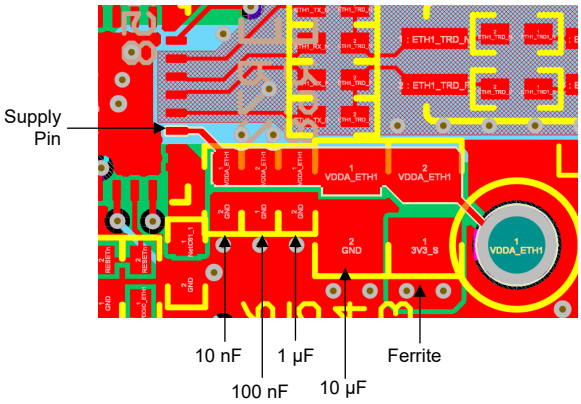

Figure 2-3. Power Supply Layout

2.2 External Supply Lines

Somehow you will always need to feed power to your system, this means you have a cable going to your system. Now, if you have noise generated from your system on this cable, it will start radiating. So the goal is to keep this line as clean as possible. Typically you see on this line all the noise generated by the first DC/DC, in the example above the 24 V to 5 V buck regulator plus some noise (typically higher frequency) that will find the way to the input.

Typically the noise you see here has some lower frequency components from the DC/DC such as the switching frequency plus harmonics, as well as high frequency components. The low frequency parts can be typically eliminated effectively with a Pi filter, L3, C42 and C44 in the example in Figure 2-4. Here, you need to be a bit careful to not build a resonant tank that makes things worse, so a lossy aluminum capacitor (with significant ESR) is a good choice. Power Stage Designer offers a filter designer, that can help here. (POWERSTAGE-DESIGNER)

The high frequency components can ignore this filter and use the parasitic capacitance of this inductor to pass through the filter. Therefore it is useful to add a ferrite bead in addition, this can reduce the noise in the two and three digit MHz range.

Lastly, there can also be some common mode noise, you cannot eliminate this way, but an additional common mode choke directly at the input connector can reduce this.

If all these measures are really needed to pass EMI conformance tests is hard to judge upfront, but better place them on the first PCB, if it is not needed, you can remove them in the final product. With a current clamp you can measure whether the noise you see on the lines is a common or differential mode noise.

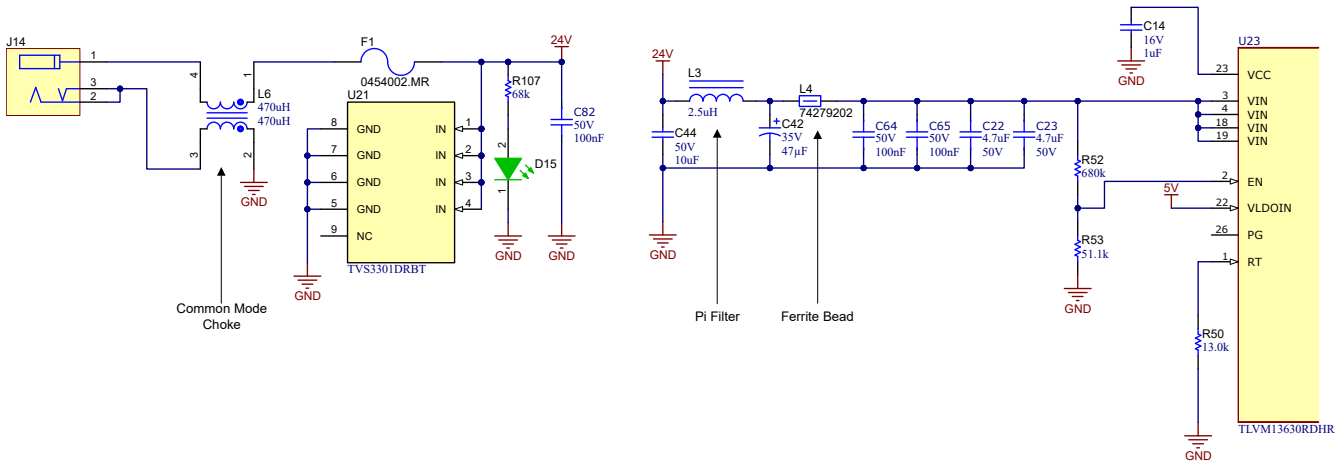

Figure 2-4. External Power Supply

For the layout of such a filter the layout can be simplified into three stages, the high frequency filter, the low frequency filter and the common mode noise filter.

For the high frequency filter, a ferrite bead, similar rules apply as for the internal supply rails. You want to keep the noise where it is generated and not have it travel everywhere. This is done as before, by placing a ferrite bead close to the noise source. Figure 2-5 shows how this is implemented in the layout.

A buck converter always generates more noise on the input side than on the output side, whereas with a boost converter it is the other way round, due to the topology LC combination. So the buck converter needs to have a filter, it draws fast rising currents from its input capacitor, that is already filtering a lot, especially the lower frequencies but it is not able to do much at higher frequencies. Looking at the frequency domain, the noise consists of the switching frequency, all the harmonics and noise caused by parasitic capacitances and inductances. As the rise times are designed to be as fast as possible (to reduce switching losses) the harmonics can go up to three digits MHz. As example a buck converter with 1 MHz switching frequency has a rise time in the single digit nano second range, resulting in several 100 MHz of noise spectrum. The input capacitor of 4.7 µF already has more than 100 mΩ impedance at this frequency, as the parasitic series inductance takes over. The ferrite bead can do a good job in keeping this away from your power line.

Besides that, of course you need to continue to use the general design rules for a DC/DC converter, otherwise the ferrite bead cannot save you.

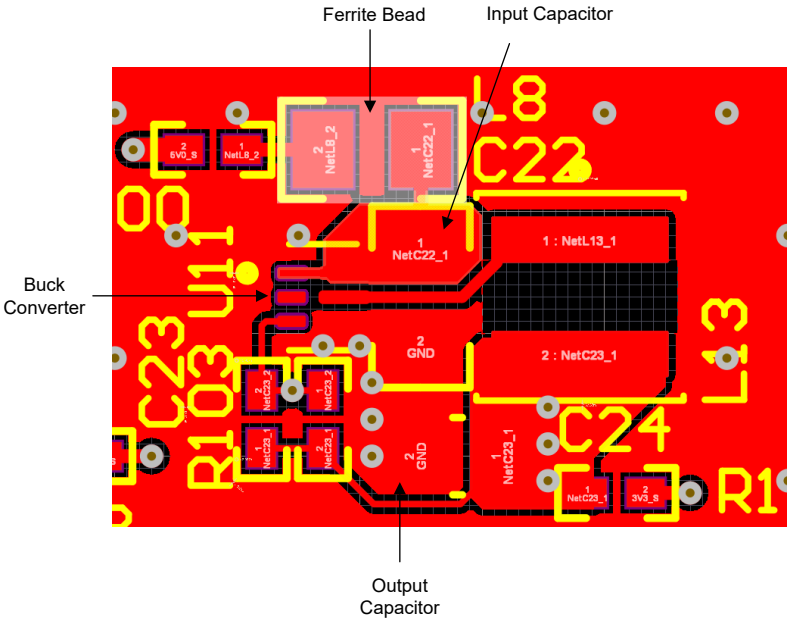

Figure 2-5. DC/DC Filter Layout

Second step, the previous mentioned filter has eliminated a lot of the high frequency noise, but the fundamental switching frequency and some harmonics are still left on the line. Here the Pi filter as shown in the schematic can help. The placement is not that critical anymore, as we are taking about lower frequencies. In Figure 2-6, the filter is shown, try to minimize capacitive coupling from the input to the output and connect capacitors in a way the current has to pass them.

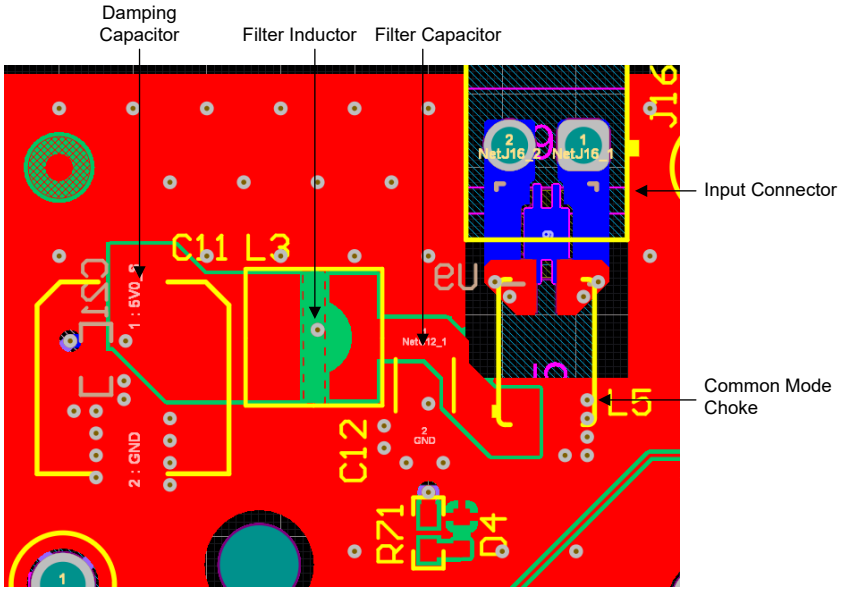

Figure 2-6. Pi Filter Layout

Also shown in Figure 2-6, is the common mode choke. A common mode choke should reduce all common mode noise, meaning all noise that is the same on both supply lines. This is typically higher frequency noise that couples in a capacitive way into supply planes and from there to the supply traces. As this originates for example the ground plane, it is necessary to cut out this plane where the common mode choke is located and the traces to the connector are. Otherwise the effect of the common mode choke can be reduced.

Table 2-1 is a quick checklist to verify a schematic and layout.

Table 2-1. Schematic and Layout Checklist

	Schematic	Layout
At least one capacitor per supply pin on IC (for example, Ethernet PHY)?		
Option for ferrite bead close to IC (for example, Ethernet PHY)?		
Traces from IC to capacitor as short as possible?	N/A	
Capacitors on IC in correct order?	N/A	
Ferrite bead on the correct place?	N/A	
Power supply with ferrite bead at input of buck regulator?		
Ferrite bead close to input capacitor of buck regulator?	N/A	
PI Filter at input of power supply?		
Common mode choke at input connector?		
Common mode choke without GND plane underneath?	N/A	

2.3 Requirements for PoDL

Some systems not only have one power source, but can be powered either from a local power supply or from a combination of data and power line, such power over data lines. Here are some additional rules that can apply to prevent interference from the power supply into the data signal.

The IEEE standards 802.3bu and 802.3cg specify the requirements in terms of ripple voltage at certain frequencies for the different types for PD and PSE. Looking at a type E powered device, there is specified, in IEEE 802.3bu table 104-7 item 3a, a allowed ripple voltage of 0.1 Vpp in the range of 1 kHz to 10 MHz. Item 3b specifies for the same range 0.01 Vpp.

Item 3a and 3b specify different methods for measuring the voltage at the PD. Both have in common to power the device through a DC bias network and measure the ripple voltage through a differential probe. This differential probe is specified to have a specific impedance and transfer function. The two plots $H_1(f)$ and Z(f) Figure 2-7 and Figure 2-8 show the impedance of this differential probe over frequency, as well as the transfer function in the given frequency range for 803.3cg, type E.

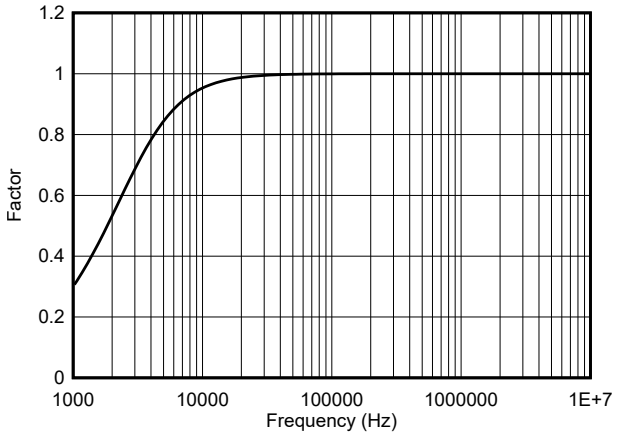

Figure 2-7. $H_1(f)$ as Given by IEEE802.3cg

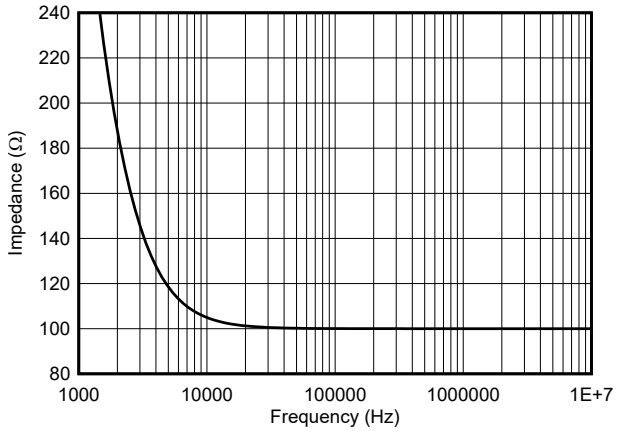

Figure 2-8. Z(f) as given by IEEE802.3cg

The voltage measured with this probe must not exceed 0.1 Vpp in 1 kHz to 10 MHz range, otherwise the voltage can impact the data transmission.

Moreover, also a post processing transfer function $H_2(f)$ is given. The measurement must be scaled with this and must not exceed 0.01 Vpp in the given frequency range.

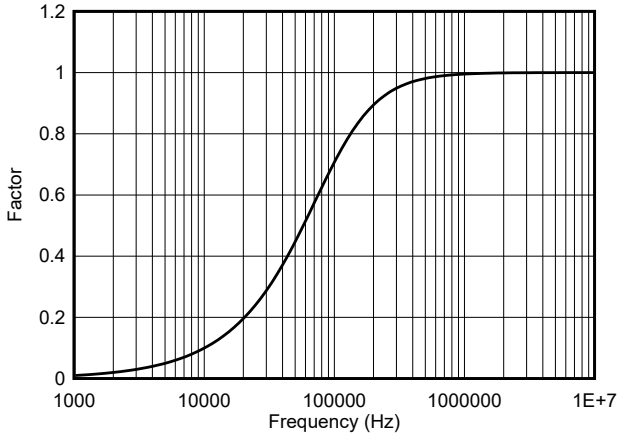

Figure 2-9. $H_2(f)$

This results in a maximum ripple voltage as shown in Figure 2-10.

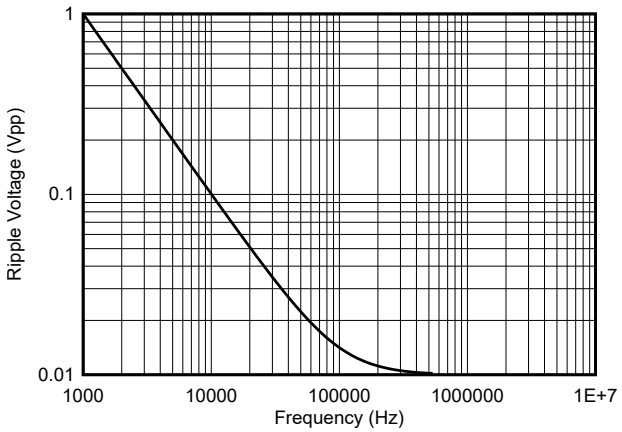

Figure 2-10. Maximum Ripple Voltage

The system must not exceed these voltage limits and the filtering has to be done properly.

2.4 Clocking

Clocking the different components of the interface system needs to be considered, for investigation communication system is built around processor with a MAC layer and a PHY layer, each part is an individual hardware and needs to be provided with an external crystal or oscillator. This leads to the typical use of either of the following two options.

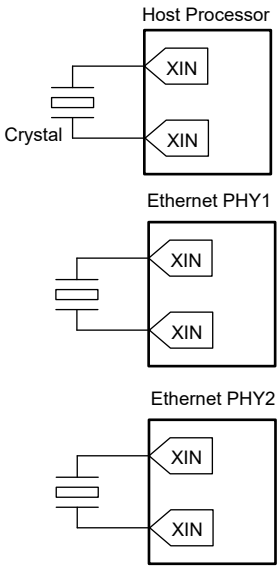

Figure 2-11. Topology 1

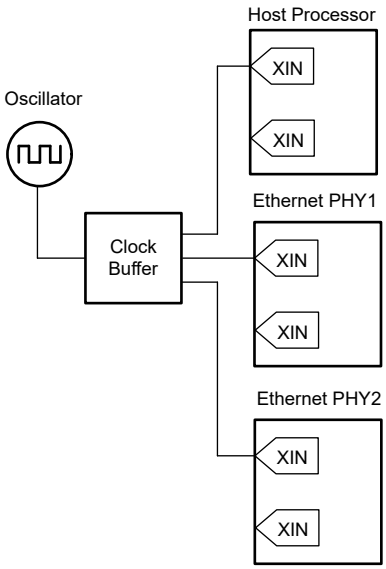

Figure 2-12. Topology 2

Pending the chosen topology, there is an importance to consider how to implement those to be robust for EMC and radiate less EMI.

2.4.1 Topology 1

Using a crystal to clock the IC's, it is important to read the crystal data sheet and the IC's data sheet to confirm that the two parts are able to work together. With that being done, a typical crystal connection can look like the following.

R**2** and R**3** is the series termination of the crystal and R**1** is the parallel termination of the crystal, these resistors can be added to the circuit but can also be removed to achieve smaller traces. However, the use of those resistors can be mandated from the IC data sheet.

The C1 and C2 capacitors are important to use C0G/NP0 capacitors for proper performance on system level.

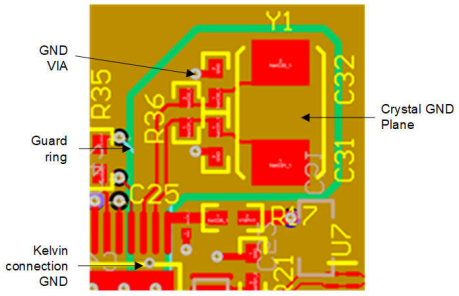

Figure 2-13. Clock Layout - Option 1

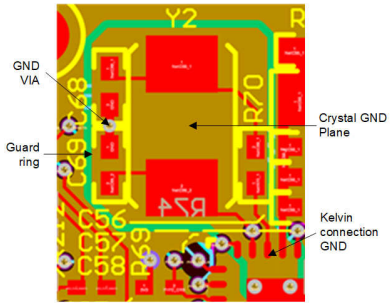

Figure 2-14. Clock Layout - Option 2

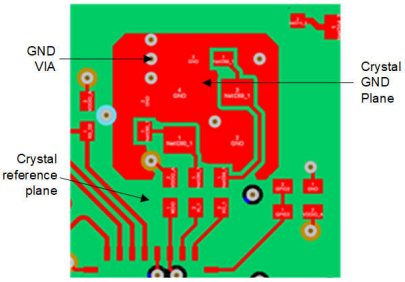

Figure 2-15. Clock Layout - Option 3

As shown in the layout examples, the suggestion is to have the crystal ground connected on an island, keeping noise away from the system ground. However there is an importance to keep this crystal ground kelvin connected to the system ground to make sure this island ground is not susceptible to high-frequency ringing.

2.4.2 Topology 2

Using an oscillator or a clock buffer as a clock source typically means that the connection used is a single ended signal. This means that the driver and receiver of the clock signal IC needs to have a defined impedance on the used port. Here typically for the oscillator and clock buffers the driver impedance for a CMOS output this is typically 50 Ω. With this in mind it is now important to also look at the impedance of the receiver circuit of the clock buffer or IC clocked. This input circuit is typically high impedance circuit, this means a series termination on the clock trace at the clock input circuit is good practice to ensure the trace is proper terminated.

With the potential long trace, it should be defined for the PCB to ensure that the PCB trace is 50 Ω impedance matched, this will reduce the ringing effects.

Here of cause also the trace length needed to implement the circuit also have effects on if it makes sense to add the additional termination. This termination of single ended signals have some typical methods which can be shown in Figure 2-16 and Figure 2-17.

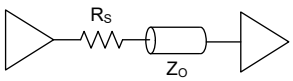

Figure 2-16. Series Termination

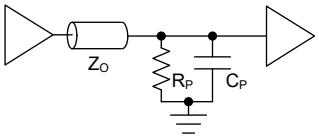

Figure 2-17. Parallel Termination

Figure 2-18 is an example of how to terminate the 50 Ω trace to the high impedance input using both Series and Parallel termination.

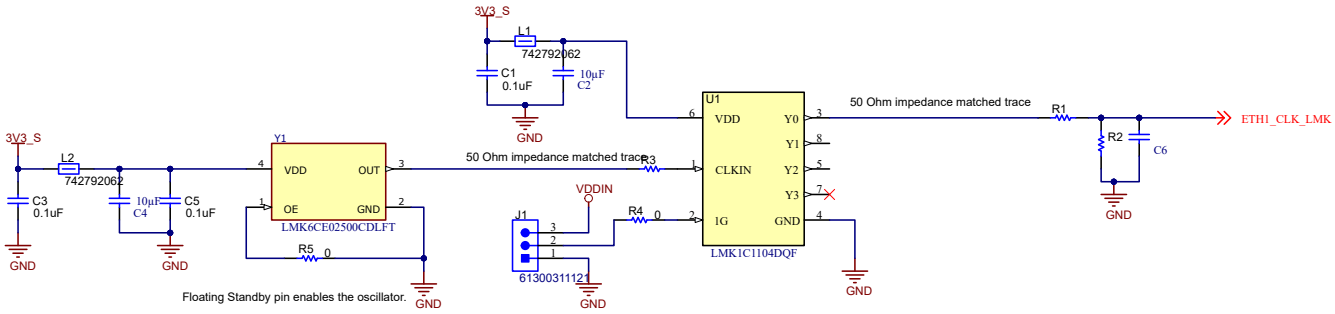

Figure 2-18. Oscillator with Clock Distribution Connection to IC

Another point to remember here is to ensure that the voltage levels from the clock buffer fits the input voltage levels of the PHY and MAC device used, it is can also add the need to divide down the voltage level from the buffer. This can be done either capacitive or resistive voltage divider. On Figure 2-18, placement of the resistors and capacitors are placed as they should be placed in the PCB.

One topic here to remember is that the typical values used for this circuit can be around the following values:

- R1 and R3 around 22 Ω to 47 Ω pending PCB design.
- R2 can be around 22 Ω to 47 Ω pending PCB design.
- C6 around 1 pF to 10 pF pending PCB design and frequency used, due to the filter effect needed there is an importance to use C0G/NP0 type of capacitors.

There values can then be refined using measurements in EMI lab to define the best choice.

3 Summary

When designing a system, keep the good rules for EMI and EMC in mind. The aspects mentioned in this document do not cover everything, but give a good starting point of often neglected aspects, such as power supply and clocking. Also focusing on the requirements for singe pair Ethernet (SPE) and the allowed ripple caused by adding power over data lines (PoDL) on top.

4 References

- IEEE802.3cg.
- IEEE802.3bu.
- Texas Instruments, *Power Stage Designer*.

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