Application Note

PCI Express Compliance Testing with the DS320PR810

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ABSTRACT

This application note describes the results of compliance and electrical testing with DS320PR810 (PCI Express Gen 5.0 8-channel Linear Redriver) and high-level redriver tuning guidance.. The intended audience for this document includes hardware engineers using DS320PR810 in their design. Please note that the procedures and testing results highlighted in this document also apply to the SN75LVPE5412 (PCI Express Gen 5.0 4-channel Linear Redriver with Integrated 1:2 Demux) and SN75LVPE5421 (PCI Express Gen 5.0 4-channel Linear Redriver with Integrated 2:1 Mux).

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Trademarks

1 Introduction

PCI Express compliance and interoperability testing is offered by the PCI Special Interest Group (PCI-SIG). The Compliance Workshop Program offers standardized device electrical and system testing for PCI Express systems, peripherals, and components. The program provides component and system manufacturers the opportunity to test new Intellectual Property (IP) for electrical performance and compatibility with other PCI Express products. Texas Instruments uses the PCI-SIG workshops to perform standardized PCIe tests which ultimately lead to inclusion on the PCI-SIG Integrators List. Products referenced on the Integrators List meet PCIe requirements and will provide a robust solution. The PCI-SIG compliance program is made up of several mandatory test procedures as well as an interoperability program.

The goal of this application note is to review the process and provide an understanding of the PCI-SIG Compliance Program, especially in the way that compliance testing relates to linear redrivers.

1.1 Add-in-Card (AIC) Form Factor

To participate in system and electrical testing, the redrivers were designed onto an AIC which can also accommodate a standard PCIe endpoint which is compliant to the PCIe standard. This endpoint acts as the redrivers *test partner*; the *test partner* is used to transmit compliant PCIe Tx presets, perform loopback, and inter operate with Host system components. The redriver and the AIC to which the redriver is mounted must be designed to allow any and all normal PCIe link configuration and activity. This design includes some of the following items:

- Receiver Detection
- PCIe Reset
- PCIe Speed Changes
- Equalization Link Training

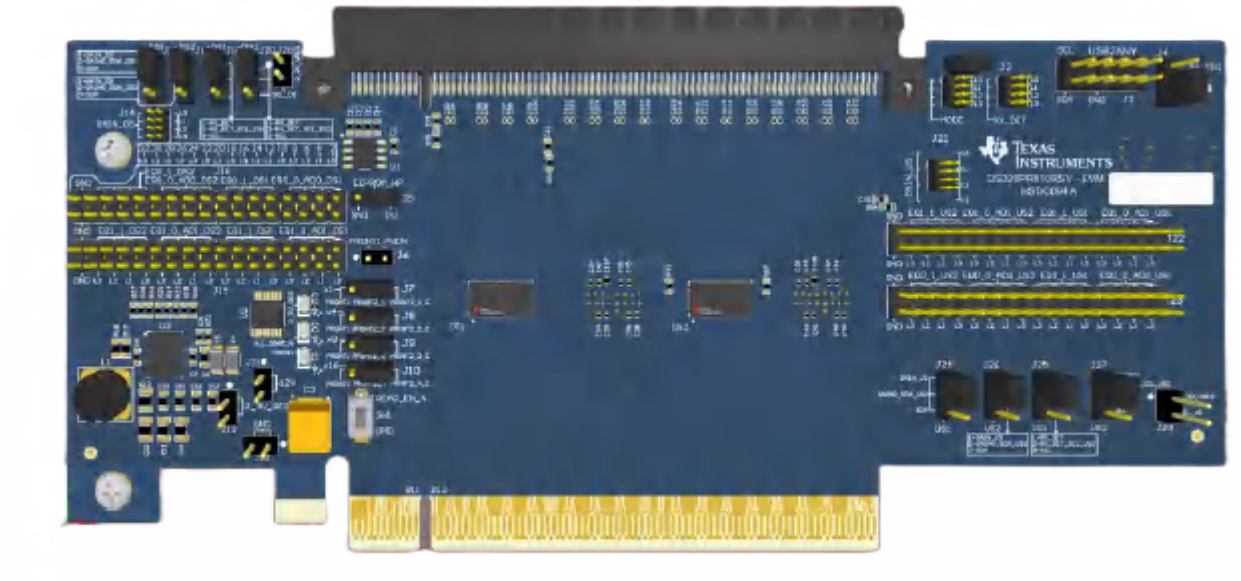

Figure 1-1. DS320PR810 Riser Card EVM

2 Compliance Tests

There are several test types that define PCI Express AIC component compliance testing.

1. **Configuration**: This test exercises the configuration space registers of the device under test. In the case of a redriver AIC the test partner is providing the PCIe specific information. Its purpose is to check for compliance with the PCI specification for configuration space registers. The test software accesses the AIC and issues configuration read and write requests and checks for the correct response. The test program also performs functional stress tests to ensure the end-point can retrain and relink in an acceptable amount of time. It also tests to make sure the AIC can properly handle hundreds of cycles of link-up/link-down and all registers are operational. While the redriver is a silent partner in this test, it is important that the redriver does not compromise any functional performance when inserted into the PCIe link.
2. **Electrical**: PCI Express Electrical Testing was developed to help verify electrical compliance to the PCI Express Base Specification(s). PCI Express Electrical Testing is a series of transmitter and receiver tests used to evaluate PCI Express Host and PCI Express AIC products. Testing on a redriver AIC and the endpoint *test partner* is done using a compliance baseboard (CBB) available from the PCI-SIG. The CBB provides the physical means to connect the AIC to high-speed test equipment for measurement and analysis.
3. **Protocol**: Link and Transaction Protocol testing to ensure AIC compliance to specification requirements.
4. **Interoperability**: For interoperability test sessions the test procedure will tend to vary by device function. For linear redrivers which do not have any endpoint function, the procedure is tied to the partner device. As an example, a PCIe SSD could be used to transfer files and data. The PCI-SIG recognizes that participants may bring designs that are not fully compliant or have unknown or undisclosed bugs. For this reason, to pass the interoperability tests, vendors must only demonstrate a success rate of 80%.

Once a device has passed 100% of the PCI-SIG mandatory tests and 80% interoperability, the device is eligible to be on the Integrators List. The Integrators List is proof a product has passed all the PCI-SIG tests and has demonstrated interoperability with others. This status implies that the device is viable for use in PCIe systems.

2.1 Workshop Test Results

Table 2-1 summarizes the PCI-SIG workshop interoperability results using the DS320PR810 AIC.

Table 2-1. Workshop Testing Summary

Test Number	Test Group	Vendor	Test Description	Test Results
1	Gen-5	Teledyne	AIC TX/PLL Gold Endpoint Tester	Pass
2	System	Microchip	Interoperability with Gen-5 root complex (x16)	Pass
3	Gen-5	Keysight	AIC link equalization	Pass
4	System	Alibaba	Interoperability with Gen-5 root complex (x16)	Pass
5	Gen-3	Teledyne	AIC link equalization	Pass
6	System	Cadence	Interoperability with Gen-5 root complex (x8)	Pass
7	Gen-4	Tektronix	AIC link equalization	Pass
8	Gen-5	Keysight	AIC TX PLL	Pass
9	System	Broadcom	Interoperability with Gen-5 root complex (x16)	Pass
10	Gen-5	Viavi	Gen-5 lane margining, link transaction	Pass
11	System	Xilinx	Interoperability with Gen-5 root complex (x8)	Pass
12	Gen-5	PCI-SIG Golden Config.	Configuration tests	Pass

2.2 Electrical Testing Results

Some of the most relevant testing is done with compliance software to measure at-speed electrical and eye performance. Table 2-2 and Table 2-3 shows system eye opening measurements after passing through the linear redriver.

Table 2-2. Eye Width Measurements at BER Gen5

Equalization	Measured Value (ps)	Test Result	Margin (ps)	Low Limit (ps)
P0 Gen5	15.350	Pass	4.725	10.625
P01 Gen5	15.831	Pass	5.206	10.625
P02 Gen5	14.521	Pass	3.896	10.625
P03 Gen5	14.770	Pass	4.145	10.625
P04 Gen5	12.306	Pass	1.681	10.625
P05 Gen5	17.315	Pass	6.690	10.625
P06 Gen5	17.509	Pass	6.884	10.625
P07 Gen5	17.655	Pass	7.030	10.625
P08 Gen5	18.012	Pass	7.387	10.625
P09 Gen5	18.311	Pass	7.686	10.625

Table 2-3. Eye Height Measurements at BER Gen5

Equalization	Measured Value (mV)	Test Result	Margin (mV)	Low Limit (mV)
P0 Gen5	32.167	Pass	10.167	22
P01 Gen5	30.724	Pass	8.724	22
P02 Gen5	31.913	Pass	9.913	22
P03 Gen5	33.157	Pass	11.157	22
P04 Gen5	34.383	Pass	12.383	22
P05 Gen5	41.763	Pass	19.763	22
P06 Gen5	41.198	Pass	19.198	22
P07 Gen5	32.055	Pass	10.055	22
P08 Gen5	35.180	Pass	13.180	22
P09 Gen5	41.540	Pass	19.540	22

Another test which highlights linear redriver performance is the Tx Preset testing. This test uses the redriver *test partner* to generate each of the PCIe Tx presets P0 – P10. The ideal and measured values with the redriver are shown in Table 2-4. The performance of the redriver is based on its own linearity and the Tx performance of the *test partner*. Ideally the redriver will exactly emulate the *test partner* performance.

Table 2-4. Tx Preset Summary

Preset	Ideal Preshoot (dB)	Ideal De-Emphasis (dB)	Redriver Preshoot (dB)	Redriver De-Emphasis (dB)
P0	0	-6	0.00	-6.85
P1	0	-3.5	0.00	-4.15
P2	0	-4.4	0.00	-4.64
P3	0	-2.5	0.00	-2.83
P4	0	0	0.00	0.00
P5	1.9	0	1.81	0.00
P6	2.5	0	2.25	0.00
P7	3.5	-6	3.23	-6.46
P8	3.5	-3.5	3.28	-4.45
P9	3.5	0	3.04	0.00
P10	0	-10	0.00	-10.51

The Preset test is performed on a very low frequency portion of the compliance waveform. The test is run at such a low frequency to minimize PCB and cabling losses in the system. The lines use data from Presets P7 – P10 which form the perimeter of the Tx equalization space, other Presets use lower values of Preshoot and De-emphasis.

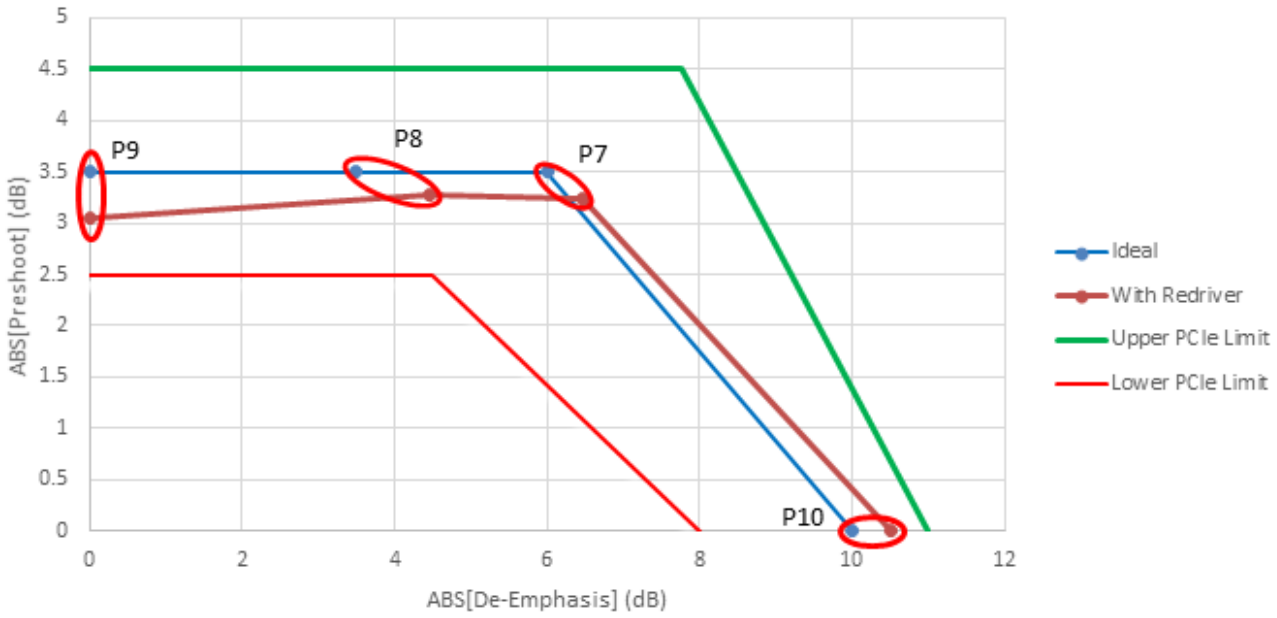

Figure 2-1. Graphical Representation of Tx Equalization

3 Electrical Performance

Why is redriver linearity and bandwidth so important?

PCI Express along with most modern communication standards uses the concept of link training and adaptive signal conditioning. Although the specifics and algorithms will vary, all incorporate methods that allow receivers (Rx) to feedback or recommend finite impulse response (FIR) coefficient changes to the transmit (Tx) device. Working through this process enables the system Rx/Tx pair to arrive at a total channel solution for signal compensation without external intervention. For the linear redriver to work robustly in an autonomous link training environment, it must maintain and preserve the linearity of the channel while providing sufficient high frequency gain to effectively turn a long channel into a shorter, less lossy channel. The linear equalizer must possess sufficient bandwidth and dynamic range to accomplish this task without distorting the original signal. Hence, maintaining linearity of the redriver across different EQ Indices and DC Gain is very important.

The redriver allows for tuning both the Continuous Time Linear Equalizer (CTLE), or EQ Index, and DC Gain of the transmitted signal. This section outlines the effects of both of these parameters on the time domain and eye diagram of the transmitted signal from the linear redriver.

For reference, the settings outlined in Table 3-1 were used in sections 3.1, 3.2, 3.3, and 3.4. For further information regarding other redriver EQ Index settings, please reference the DS320PR810 data sheet.

Table 3-1. EQ Index Summary

EQ Index	Typical EQ Boost (dB) at 16 GHz
0	4.0
Default	10.0
10	15.0
15	19.0

3.1 Effects of EQ Index on Time Domain Signal

Ideally, there would be no difference between the waveform at the signal generator and after the redriver. Using a time domain overlay helps to paint a clear image of linear equalization at work. Examples of varying EQ Indices at 16GHz show the effect of equalization on the time domain signals in Figure 3-1. Note that DC Gain = 0dB for this figure.

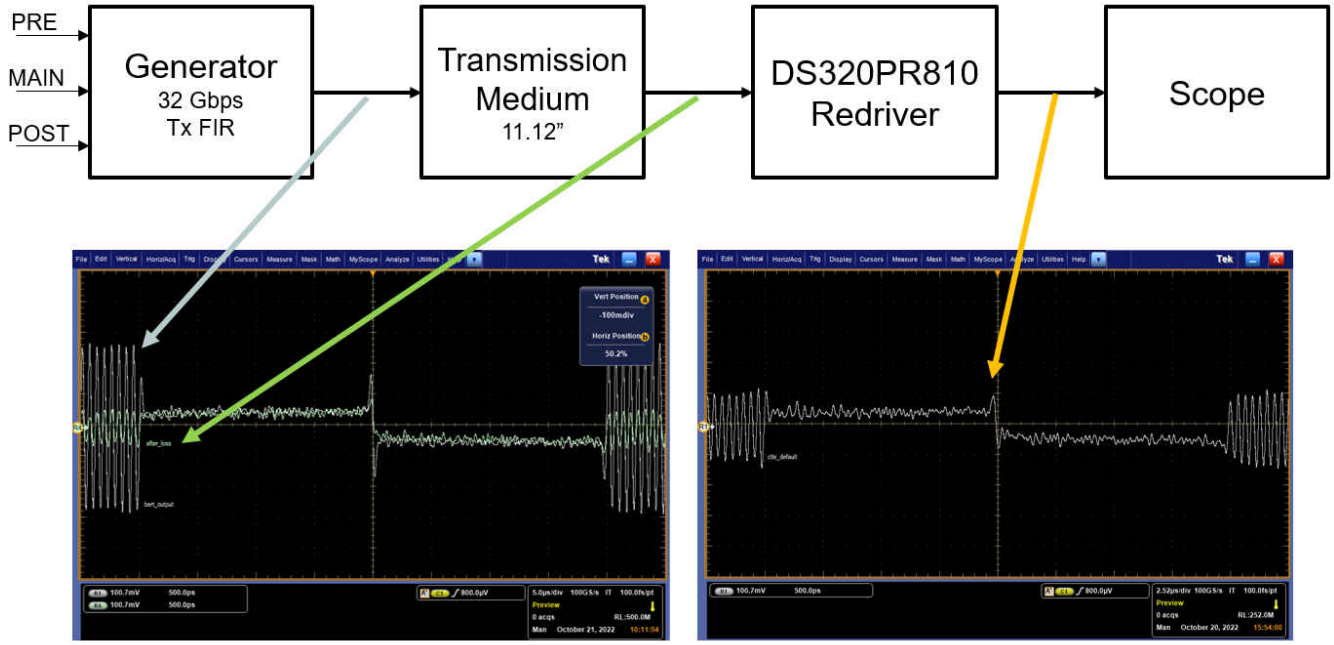

Figure 3-1. Time Domain Signal After Generator, Loss Trace, and Redriver

As shown in Figure 3-1, the time domain signal levels after the generator and after the redriver differ with an EQ Index of *Default* selected on the redriver. The following examples show the comparisons of time domain signals at the output of the redriver for EQ Indices of 0, Default, 10, and 15.

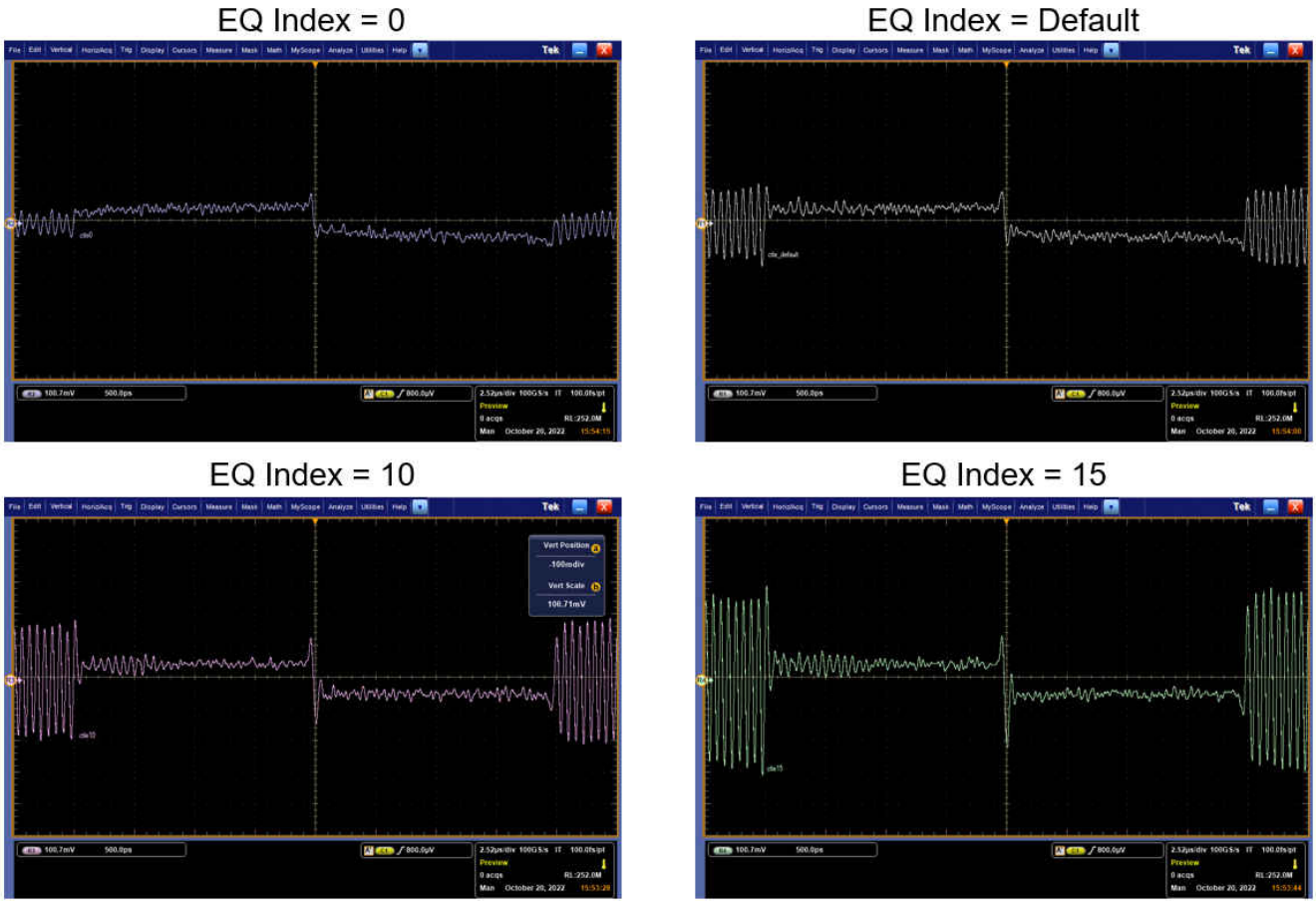

Figure 3-2. Time Domain Signal Comparison of EQ Index 0, Default, 10, 15

As shown in Figure 3-2, the amplitude of high-frequency components in the time domain signal are amplified as the EQ Index is increased. It is important to note that too large of an increase in the amplitude of the high frequency component of the time domain signal may not indicate the ideal eye opening at the output of the redriver. This process is highlighted in the following section.

3.2 Effects of EQ Index on the Eye Diagram

To further understand the importance of linearity when adjusting the EQ Index, the eye diagrams for each index are displayed in Figure 3-3.

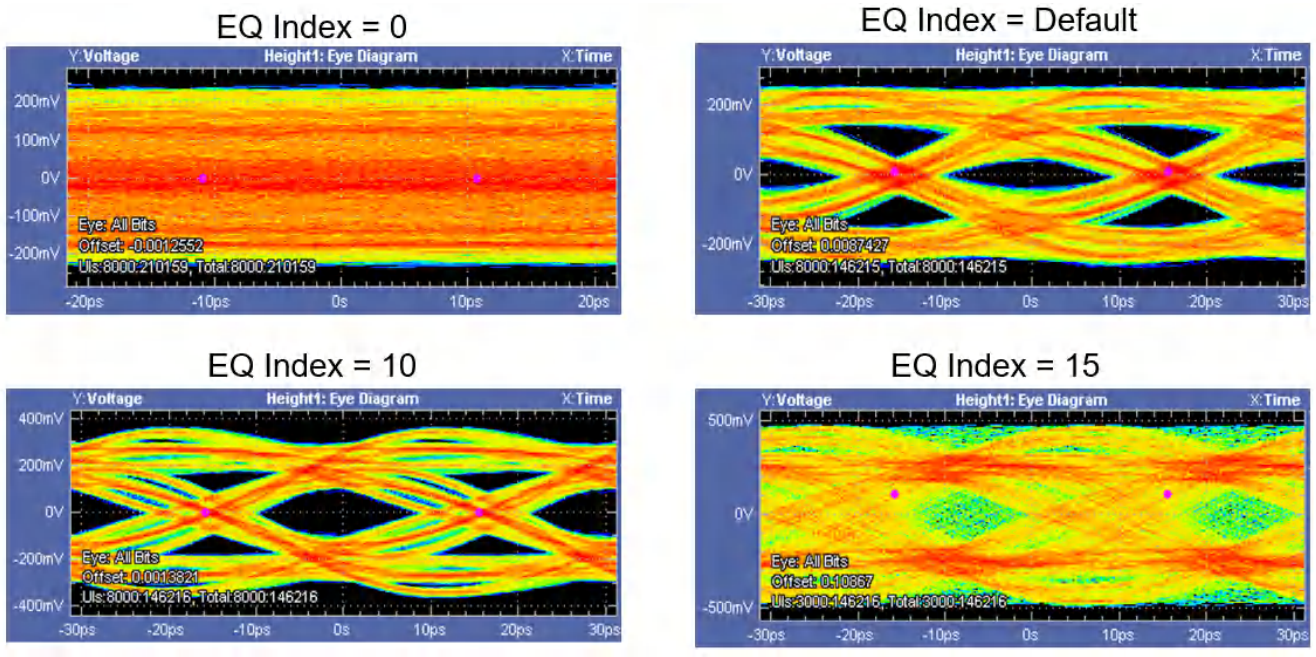

Figure 3-3. Redriver Output Eye Diagram vs. Different EQ Index Settings

The eye diagrams comparing the output of the redriver at different EQ Indices highlight the importance of the redriver's linearity. At the EQ Index 0, it can be observed that the signal is very under equalized, as there is no eye opening at all. At the default EQ Index, it can be observed that the signal is still slightly under equalized, as the eye opening is larger but not completely open. However, it is important to mention that if a short trace lies between the output of the redriver and the end point receiver, it is preferred to operate with the redriver under equalizing. This allows a higher linearity in the signal, while allowing the root complex and endpoint to do FIR training and optimization. At EQ Index 10, the eye opening is much larger and the voltage level of the signal has also increased. While it may appear that the eye is over equalized, there is good eye opening. In a system where a long trace lies between the redriver output and endpoint, then EQ Index of 10 is preferred. This is because the additional de-emphasis in the signal would help to compensate for this long trace. At EQ Index 15, the eye completely closes again even with a higher signal voltage level, indicating that the channel was over equalized. Thus, it can be determined that an ideal EQ Index lies between [5, 15); this range of EQ indices can be narrowed down with further testing. Table 3-2 shows the vertical eye opening (VEO) and horizontal eye opening (HEO) values, along with the jitter profile after the redriver for each EQ Index in the tests performed.

Note that the ideal eye was captured with an EQ Index in the range of [5,15). In the previous section, the amplitude of the high frequency time domain component increased with each increase of the EQ Index; however, not every increase of the EQ Index produced an improved eye diagram. While the amplitude of the time domain signal at the output of the redriver was larger at EQ Index 15, the better eye opening was produced at EQ Index 10.

Table 3-2. EQ Index Variation Eye Measurements

EQ Index	VEO (mV)	HEO (ps)	TJ (ps)	RJ (ps)	DJ (ps)
0	0	0	77.651	3.778	24.507
Default	70.265	10.908	20.343	0.577	12.228
10	178.54	13.830	17.420	0.407	11.696
15	0	0	37.410	0.346	32.545

3.3 Effects of DC Gain on Time Domain Signal

The redriver output is also affected by the DC Gain applied to the signal; these effects on the time domain signal can be observed in Figure 3-4. Note that the EQ Index selected for these tests is the *Default* setting.

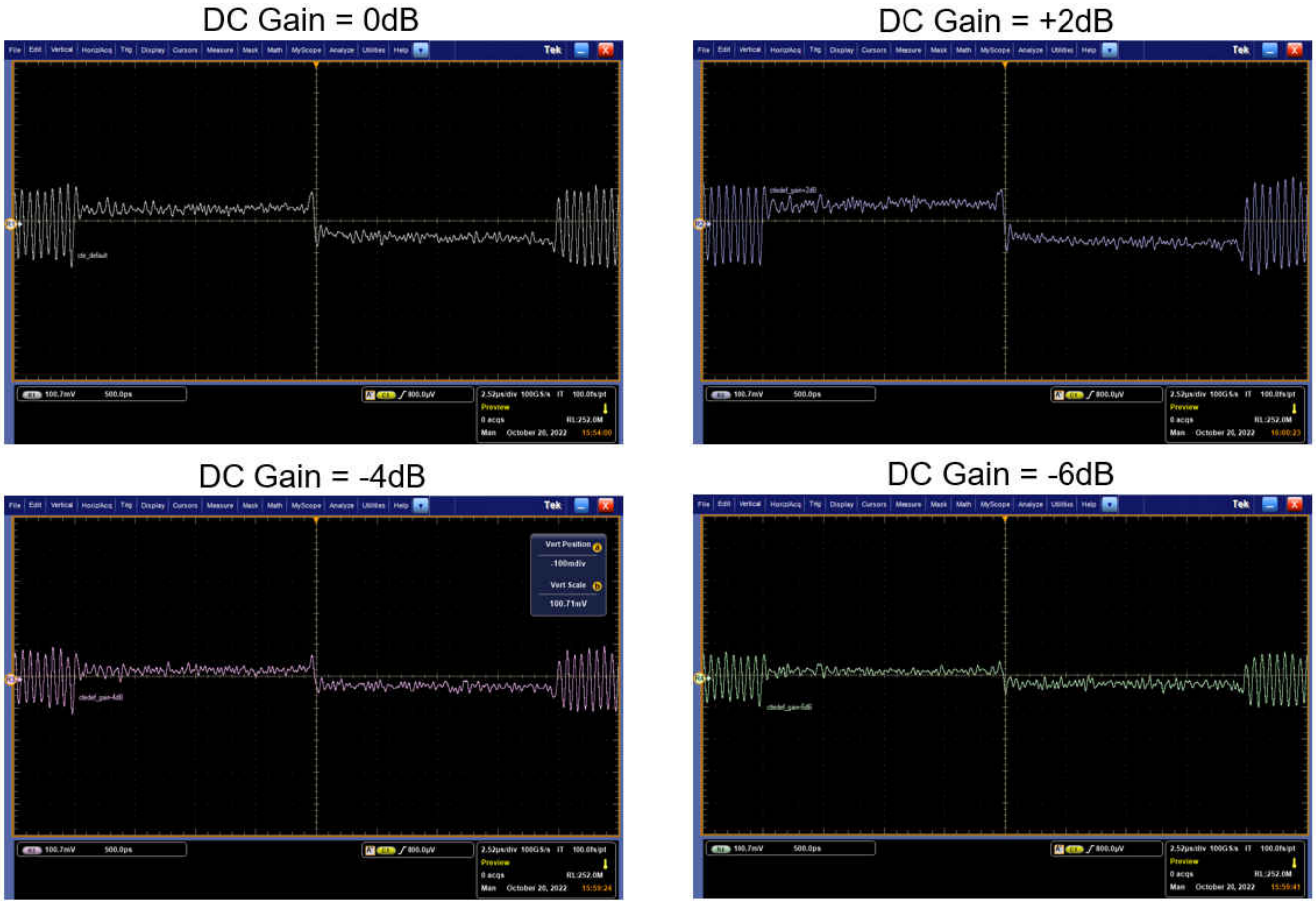

Figure 3-4. Time Domain Signal Comparison of DC Gain

As seen in Figure 3-4, adjusting the DC Gain mainly impacts the low frequency components of the time domain signal, either increasing the DC voltage level (at +2dB) or decreasing the DC voltage level (-4dB and -6dB). Notice that the high frequency components of the signal are minimally affected by adjusting DC Gain, and that amplitude of the long string of zeros or ones is reduced as gain approaches the -6dB DC Gain setting.

3.4 Effects of DC Gain on the Eye Diagram

The effect of DC Gain adjustment can again be seen in Figure 3-5, which shows the eye diagrams for each DC Gain level tested after the redriver.

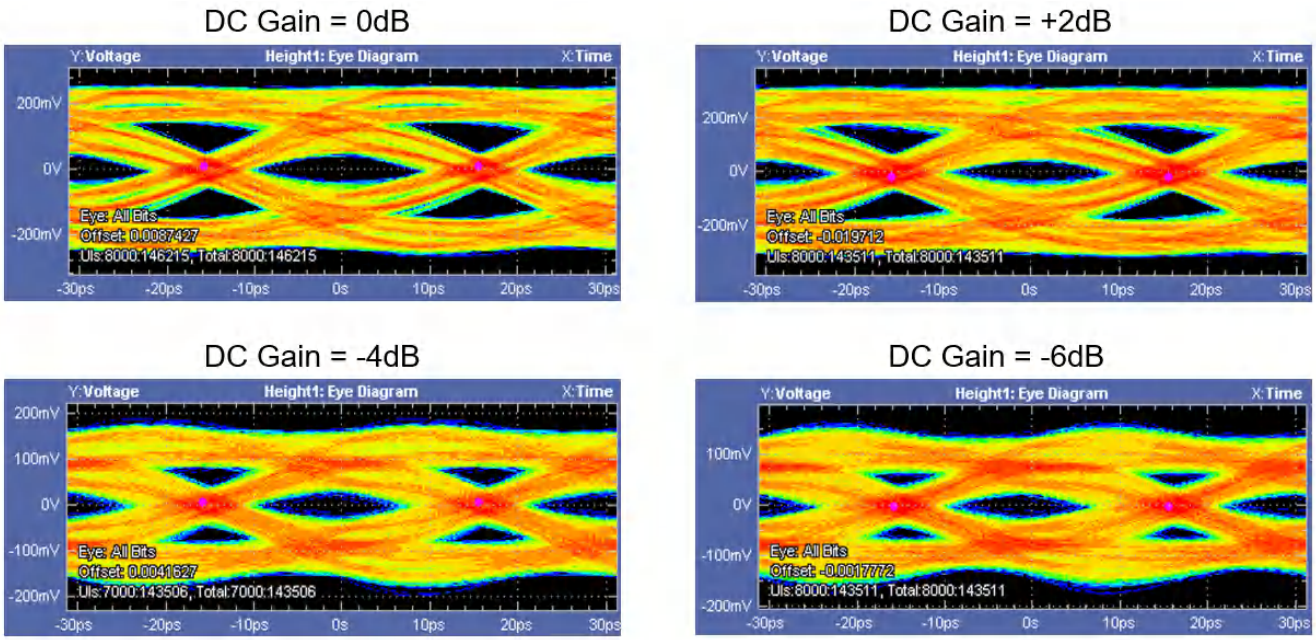

Figure 3-5. Redriver Output Eye Diagram vs. Different DC Gain Settings

As DC Gain is adjusted, variations in eye shape and opening can be seen. Note that adjusting DC Gain affects the eye height (VEO) of each eye diagram, but this adjustment does not greatly impact the eye width (HEO) of each eye diagram.

Comparing each eye diagram against the 0dB result, the following can be observed. At +2dB DC Gain, the DC level (outer eye) increased, but the eye height (VEO) was reduced. At -4dB DC Gain, the DC level and eye height were both reduced. Eye width (HEO) was slightly reduced as well, but in some cases it is observed that negative DC Gain settings marginally improve eye width. Finally, at -6dB DC Gain, the DC level is further reduced and eye width is reduced as well. Again note that in some cases, this may marginally improve eye width. In summary, it can be observed that optimum eye opening occurs when 0dB DC Gain is used, confirming the data sheet recommendation of using 0dB DC Gain.

Ideally, a channel that is equalized with the correct EQ Index and DC Gain value allows a channel signal to be replicated, giving the PCIe receiver a strong push to optimize the link based on what it perceives to be a relatively short low-loss application. This will result in a consistent training result optimized to the PCIe receiver strengths and characteristics.

4 Compliance Setting Fine Tuning

The most common failure with a redriver at compliance testing is the Tx Preset testing. As shown in Section 3, using a linear redriver alters the calculated Preshoot and De-Emphasis values by up to 1 dB. If the system *test partner* is already close to the PCIe limit for this specification, adding an improperly tuned redriver may result in a marginal failure. Similarly, adding a well equalized redriver to an endpoint that is marginal or fails the preset test can help the endpoint to pass the preset test. To properly tune the redriver, it is important to understand the core electrical concepts that impact the redriver's performance, as described in Section 3.

To understand the redriver's potential impact in a system, tuning typically begins with an equalization value (EQ Index) of 0 and a DC Gain of 0dB. The EQ Index can be increased one step at a time while using an eye opening monitoring tool to analyze the impact of higher equalization settings on system performance.

5 Summary

This application note presents data to show linear redrivers are very effective at compensating for PCIe channel attenuation without distorting received waveform characteristics. The application note also highlights the independence of DC Gain and EQ settings on linear redriver output waveform characteristics.

6 References

- Texas Instruments, DS320PR810 Eight-Channel Linear Redriver for PCIe 5.0, CXL 1.1 data sheet

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