Application Note

DP83TC812, DP83TC813: System Implementation of Open Alliance TC10 Sleep/Wake-up

ABSTRACT

Automotive ethernet networks need a sleep mode of operation where the PHY is inactive and waiting for a few triggers in the system. The whole network should be able to transition out of sleep upon receiving those triggers without any manual intervention. Ultra-low power consumption is a must in this sleep mode of operation to reduce battery discharge. Open Alliance defines TC10 sleep/wake-up specification to tackle these challenges.

TI's DP83TC812, DP83TC813 are the next generation 100M Automotive Ethernet PHYs that are fully compliant with the TC10 specification. This application note provides information related to TC10 and how to effectively use the sleep/wake-up feature of DP83TC812/3 in the system.

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Trademarks

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1 Introduction

DP83TC812/3 is 100BASE-T1 Ethernet PHY with TC-10 power saving feature with the following features.

- Open Alliance TC10 compliant
- 8µA (Typical, 27 °C), 18µA (Maximum, 125 °C) sleep current
- Wake forwarding feature for Ethernet network wake-up
- Open Alliance TC1 Interoperability and EMC compliant
  - EMC immunity Class-IV compliant for UTP
  - SAE J2962-3 EMC compliant

1.1 System Block Diagram

This block diagram shows the system level integration of DP83TC812/3 to support the TC10 sleep/wake-up feature.

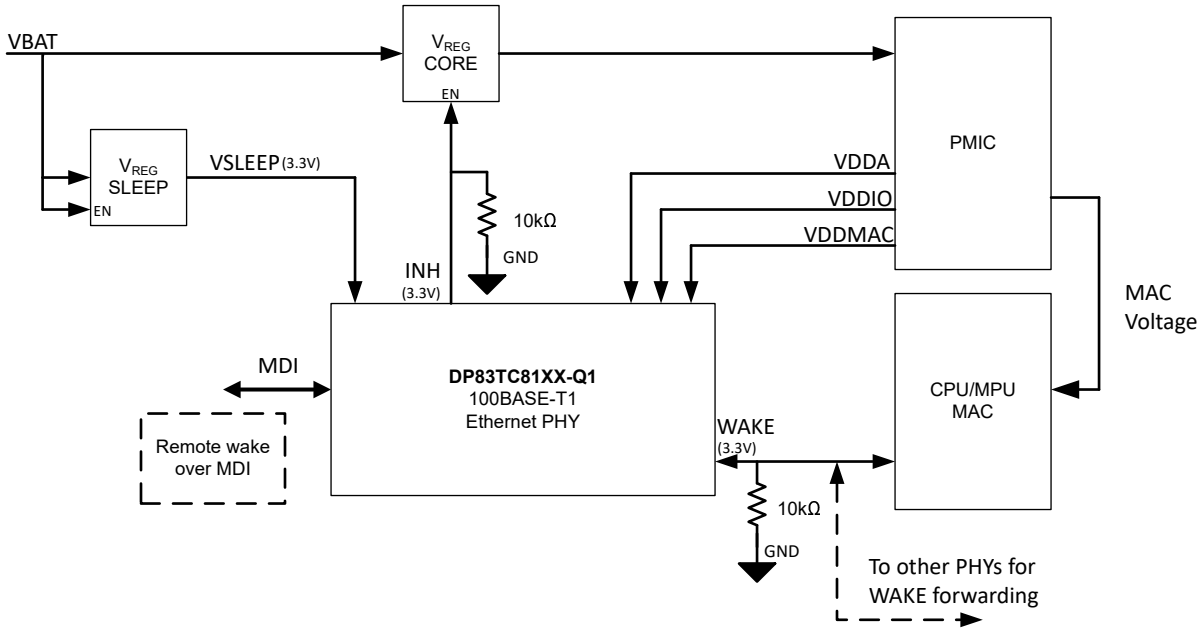

Figure 1-1. System Block Diagram

1.2 Terminology

This section explains the terminology used in this document.

- **WUP** – Wake Up Pulses (Differential Signal sent on MDI from one PHY to another to wake-up)
- **WUR** – Wake Up Request (Differential Signal sent on MDI during active link to re-initiate Wake Forwarding)
- **LPS** – (In context of LPS symbols) Low Power Sleep symbols sent during sleep negotiation
- **INH** – Inhibit Power Shut Down
- **VBAT** – Battery Voltage Supply
- **PMIC** – Power Management IC

2 TC10 Pin Descriptions

The following pins are used by the DP83TC812/3 for TC10 functionality

Table 2-1. Pin Descriptions

Pin No.	Name	Type	Function
7 (DP83TC812) 15 (DP83TC813)	VSLEEP	Supply	3.3 V power supply input derived from VBAT
8 (DP83TC812) 16 (DP83TC813)	WAKE	I/O	Bidirectional I/O pin used for • Local Wake Input • Wake Forwarding Output
10 (DP83TC812) 17 (DP83TC813)	INH	Output	Indication Output for Sleep Mode • High - Functional./Wake-up Mode • Hi-Z - Sleep Mode

VSLEEP

The VSLEEP pin needs a 3.3 V power supply input. The supply is derived from a low power LDO directly from VBAT (usually 12 V to 48 V). During sleep mode, to have the lowest power consumption, it is recommended that the VSLEEP is only supply which is on.

The following table shows the characteristics of this power supply pin.

Table 2-2. VSLEEP Supply Requirements

S.No.	Parameter	Description	Units	Min	Typ	Max
1	VSLEEP Voltage	Supply voltage operation limits	V	2.97	3.3	3.63
2	VSLEEP Ramp time	Ramp time (0-100%) of the supply	ms	Refer to Data Sheet		
3	Current consumption – Sleep mode	Current consumption from VSLEEP in sleep mode (INH = 0)	µA		7	18
4	Current consumption – Functional mode	Current consumption from VSLEEP in functional mode (INH = 1)	mA			4

The following image shows the recommended de-coupling network for the VSLEEP supply

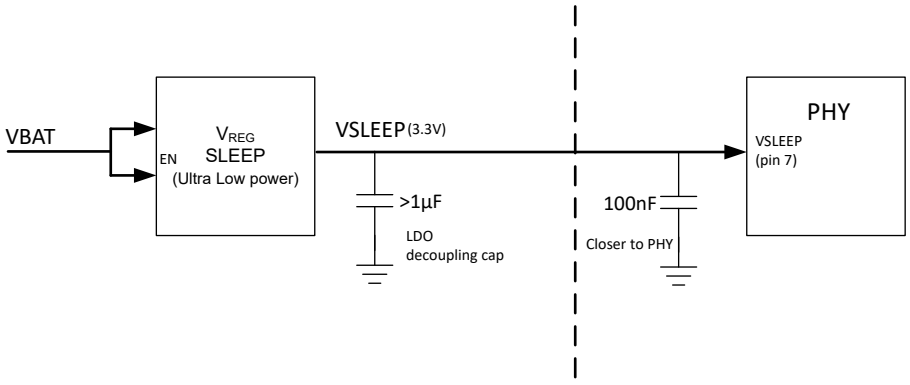

Figure 2-1. VSLEEP Supply Network

WAKE

WAKE is a bidirectional input pin used for local wake as input and wake forwarding as output. This pin can be controlled by the MAC/controller for local wake. Open drain (high polarity) is recommended from the MAC/controller.

A pulse of width >40 µs on this pin wakes up the PHY. For wake-forwarding, the pin drives the pin high for some time and transitions back to input mode emulating open drain drive.

Since the pin uses open drain configuration, a strong external pull down resistance (10 kΩ) can be used.

The following table shows the requirements of the WAKE pin

Table 2-3. WAKE Requirements and Characteristics

S.No.	Parameter	Description	Units	Min	Typ	Max
1	VIH	Minimum voltage beyond which the input buffer detects high	V	2		
2	VIL	Minimum voltage below which the input buffer detects low	V			0.8
3	R pull-down	Pull-down resistance on the pin internal to the PHY	kΩ		455	
4	VOH	Output high voltage (@ I = 2 mA)	V	2.4		

INH

INH is an open drain (high polarity) output pin which indicates whether the device is in sleep mode.

When the device is in sleep mode, the driver is turned off (Hi-Z). A pull down resistance external to the PHY can be used (10 kΩ recommended) which pulls down the INH pin down to 0 V.

When the device is out of sleep, INH transitions to high.

Table 2-4. INH Characteristics

S.No.	Parameter	Description	Units	Min	Typ	Max
1	VOH	Output Voltage (@ I = 2 mA)	V	2.4		

3 Primary Functions of the PHY

The following section describes in detail the primary functions of the ethernet PHY (DP83TC812/3) in supporting TC10.

3.1 Transition from Sleep to Wake-up mode

3.1.1 Local Wake Detection

To wake-up the PHY locally (local wake), a pulse of width greater than 40 µs is required to be forced on the WAKE pin. The detection circuit inside the PHY on the WAKE pin rejects any pulse of width less than 10 µs and detects any pulse greater than 40 µs reliably. The core power supplies (VDDA, VDDIO/VDDMAC) are not needed for the PHY for local wake detection.

After the wake-up, PHY transitions from sleep to wake-up mode and pulls INH to high.

For local wake, it is assumed that some portion of the system is already active and the PHY is in TC10 sleep. As an example, the system might have a microcontroller in active mode to control the WAKE pin of the PHY. When the MCU wants to wake up the PHY from TC10 sleep, it raises the WAKE pin to 3.3 V to send a wake pulse.

3.1.2 WUP Transmission and Reception

To wake-up the link partner remotely, the PHY needs to send a defined sequence of PAM3 symbols for 1 ms+/-0.3 ms. WUP transmission is done after a local wake-up without any manual intervention provided the device is strapped to autonomous mode and the pin RESET is not asserted. If the device is strapped to managed mode or if the device is in RESET state, WUP is transmitted only after the device transitions to normal mode.

During the sleep mode, to wake-up the PHY from sleep, remote link partner transmits WUP. The PHY detects the WUP and transitions from the sleep mode to functional mode. The core power supplies (VDDA, VDDIO/VDDMAC) are not needed for the PHY for WUP detection. The incoming WUP signal must be compliant to 100Base-T1 PMA signal PSD mask defined in IEEE802.3.

3.2 Wake Forwarding

Wake forwarding is a way to wake-up other PHYs connected to the same WAKE line, when one of the PHYs have woken up remotely. When PHY wakes-up from sleep on the reception of WUP (remote wake-up), the PHY transmits a pulse of width greater than 40µs on the WAKE line to wake-up other PHYs connected to the same wake-line without any manual intervention.

Wake forwarding can also be done by a PHY during active link upon reception of special WUR symbols. WUR can be initiated on one the PHYs by programming ***reg<0x018C> = 0x0080***. The link partner PHY forwards WAKE pulse of width 40µs upon reception of those WUR symbols.

Note

Programming ***0x018C = 0x0080*** without the link-up will make the PHY initiate WUR immediately after the link is up.

3.3 Transition to Sleep - Sleep Negotiation

Sleep negotiation can be initiated from one of the two PHYs connected through link-up. Post the initiation, both of these PHYs go through negotiation and smoothly transition to sleep.

The sleep negotiation can be initiated (local sleep req) by programming ***reg<0x018C> = 0x0002*** on any of the PHYs.

Note

Sleep can only be initiated when there is active link between the PHYs. Programming ***0x018C = 0x0002*** without the link-up will make the PHY initiate sleep immediately after the link is up.

The states the PHYs go through in the negotiation are explained in detail below.

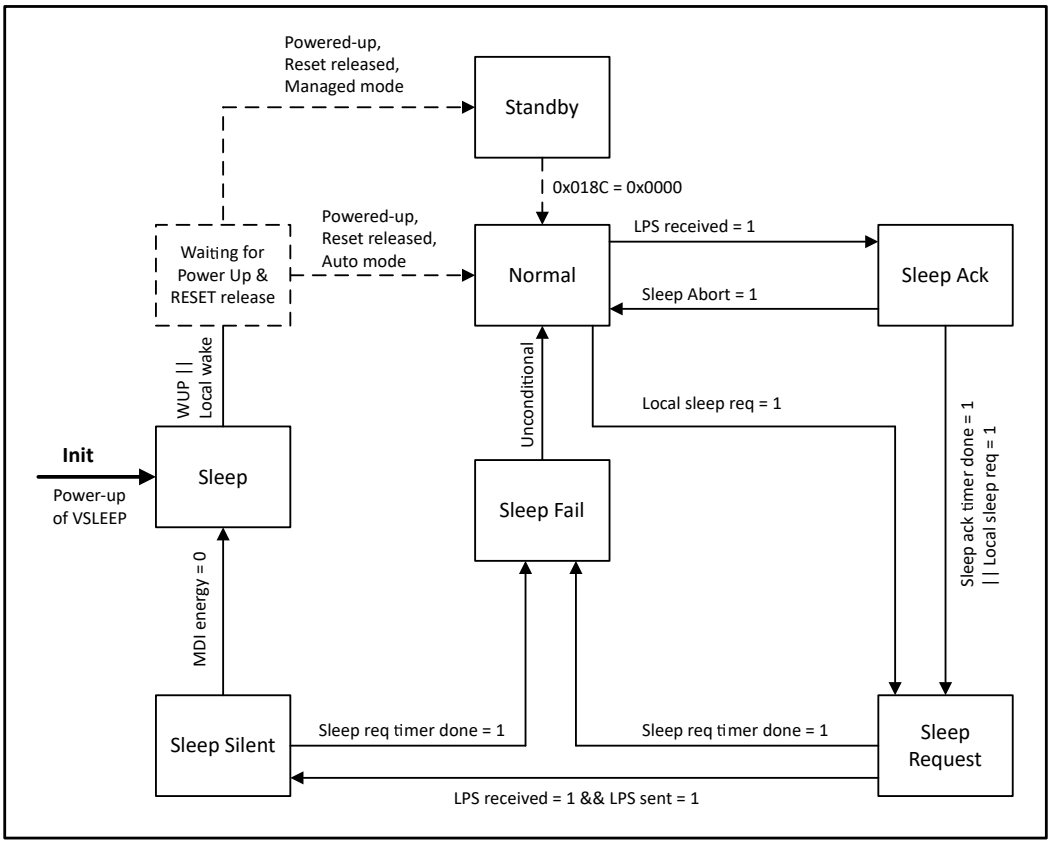

Figure 3-1. Sleep State Diagram

The MAC/controller intervention is only needed to initiate the sleep and abort the Sleep. All other state transitions happen though interaction between both the PHYs and need no external intervention and are explained below for information purpose only.

3.3.1 Sleep Ack

When a PHY receives LPS symbols from its link partner, it transitions from Normal state (linked-up state) to Sleep ACK state.

During this transition, a timer of 8 ms (sleep_ack_timer) is initialized and an interrupt is raised to indicate the MAC that the link partner is requesting sleep. The interrupt (LPS_int) is enabled by default (***reg<0x0018>[0]=1***).

The MAC can choose to abort the sleep by

- Programming ***reg<0x001B> = 0x0001*** (or)
- Drive a high pulse on LED_1 to abort the sleep (This feature is disabled by default and has to be enabled prior to sleep negotiation by programming ***reg<0x001B> = 0x0002***)

The PHY transitions back to Normal state if the MAC aborts the sleep. In case, the MAC chooses not to abort sleep before sleep_ack_timer lapses, the PHY transitions to Sleep Request state.

3.3.2 Sleep Request

The PHY which initiated the sleep (locally initiated), transitions from Normal to Sleep Request state. When the PHY transitions to Sleep Request, a timer of 16 ms (sleep_req_timer) is initialized and LPS symbols are transmitted (at least 64 bits). The PHY then waits for the link partner to send back the LPS symbols. After LPS symbols are received back from the link partner, the PHY transitions to Sleep Silent state. In case the LPS symbols aren't received before sleep_req_timer lapses, the PHY transitions to Sleep Fail state.

The PHY for which sleep is initiated remotely, the PHY transitions from Normal to Sleep ACK to Sleep Request provided the MAC chose not to abort the sleep. When the PHY transitions to Sleep Request, a timer of 16 ms (sleep_req_timer) is initialized and LPS symbols are transmitted (at least 64 bits). After LPS symbols are transmitted, the PHY transitions to Sleep Silent state.

3.3.3 Sleep Silent

The PHY transitions to Sleep Silent from the Sleep Request state and waits for the line to go silent. If the line goes silent, the PHY transition from Sleep Silent to the Sleep state. In case the PHY doesn't go silent before sleep_req_timer lapses (16 ms timer initialized when the PHY moved to Sleep Request state).

3.3.4 Sleep Fail

The PHY transitions to Sleep Fail if LPS symbols are not received before sleep_req_timer lapses or if the line is not silent before sleep_req_timer lapses, the PHY transitions to Sleep Fail state. When the PHY goes through this state, sleep fail interrupt flag (0x0018[13]) is set. Indication of this flag on INT_N pin can enabled through 0x0018[5].

After this transition, the PHY unconditionally transitions to Normal state.

3.3.5 Sleep

The PHY transitions to Sleep state after the negotiation is successful. In the Sleep mode, the INH transitions from High to Low. It is recommended to cutoff the core power supplies (VDDA, VDDIO/VDDMAC) to get the lowest current consumption.

In this Sleep state, the PHY waits for local wake or remote wake to eventually transition to Normal state.

After the first power-up, the PHY comes up in this sleep state until activity is observed on WAKE pin or MDI lines.

Note

In this sleep state, all the pins controlled by MAC/controller shouldn't be driven and to be left in a Hi-Z state. The pins must be made Hi-Z before the core power supplies are cutoff. 25 MHz clock on XI is not needed by the PHY and shouldn't be driven in the sleep mode. Crystal oscillator present on XI, XO pins internal to the PHY is also disabled in sleep mode.

3.3.6 Normal State

The PHY transitions to normal state (or standby state) from the sleep state upon reception of valid local wake pulse or WUP. After the transition to normal state, it is expected to program the initialization settings again to achieve a valid link-up.

3.3.7 Other Transitions

Apart from the state transitions in the 'Sleep State Diagram', there are some custom state transitions implemented in DP83TC812/3 for different application use-cases. The following sections explain these transitions in detail.

3.3.7.1 Forced Sleep

PHY can be placed into sleep by itself by bypassing the sleep negotiation by programming ***reg<0x0444> = 0x000C***.

For this forced sleep to work, WAKE should be driven low and MDI lines should be silent. Else, the PHY can transition to functional state immediately after the sleep is forced.

3.3.7.2 Activity during Sleep Negotiation

During Sleep Negotiation, if there is activity (i.e., packet reception) from link-partner, PHY transitions to Sleep Fail state. This transition is implemeted to drop the sleep negotiation as there is activity going on.

This feature is enabled by default and can be disabled by programming 0x018B[11] = 0. When this feature is disabled, MAC must handle the case if activity is observed during sleep negotiation.

3.3.7.3 Link Down during Sleep Negotiation

DP83TC812/3 has a few transitions implemented to handle link-down during sleep negotiation.

When link goes down when the PHY is in Sleep Request state, the PHY transitions to Sleep Fail state and then to Normal state. Sleep fail interrupt flag is set during this condition as the PHY goes through Sleep Fail state.

When link goes down when the PHY is in Sleep Ack state, the PHY directly transitions to Normal state and tries to link-up again. Sleep fail interrupt flag is not set during this condition.

3.3.7.4 Sleep Silent to Standby

Some systems might need PHY transitioning to Standby state after completing sleep negoitiation. DP83TC812/3 offers this feature which is disabled by default and can be enabled by programming 0x018B[1] = 0.

If this transition in needed, it has to be enabled before the start of sleep negotiation. Upon completion of the sleep negotiation, the PHY transitions to Standby state instead of Sleep state. INH doesn't transition to low in this case. It has to be noted that the exit from the standby state and transition to normal state is only by programming 0x018C register.

4 Relevant Registers

This section explains the relevant register fields used in TC10 implementation. Other fields sharing the same register address and are not relevant to TC10 are excluded from this section. The complete register list is available in the data sheet.

Table 4-1. Register Description

Register Name	Register Address	Bit	Field Name	Access Type	Default Value	Description
TC10_ABORT_REG	0x001B	0	cfg_sleep_abort	R/W	0x0	Sleep Abort 1b = Abort sleep when the PHY is in Sleep Ack state
		1	cfg_tc10_abort_gpio_en	R/W	0x0	Use LED_1 pin to abort sleep (CLKOUT if RX_D3 strap is set to high) 1b = Use LED_1 pin to abort sleep (drive high for abort)
LPS_CFG2	0x018B	1	cfg_lps_sleep_en	R/W	0x1	Transition to sleep mode after Sleep negotiation: 0b = Transition to Standby mode 1b = Transition to Sleep mode
		6	cfg_auto_mode_en	R/W	0x01	Autonomous Mode enable (Default value dependent on Strap): 0b = Manual Mode 1b = Autonomous Mode Note: This bit is auto cleared after link-up.
		8	cfg_tc10_dis_bond_pad_bypass	R/W	0x0	TC10 State Machine Disable: 0b = Enable 1b = Disable
		11	cfg_stop_sleep_neg_on_activity	R/W	0x1	Stop Sleep Negotiation on Activity: 0b = Continue Sleep Negotiation even if activity (packet transfer) is present 1b = Stop Sleep Negotiation on Activity
		12	cfg_stop_sleep_neg_on_no_send_n	R/W	0x1	Stop Sleep Negotiation on link-down: 1b = Stop Sleep Negotiation when link is down in Sleep Ack or Sleep Request states
LPS_CFG3	0x018C	7:0	cfg_lps_pwr_mode	RH/W1S	0x0	One hot enable for each LPS state: Bit 0: Set to 1 for Normal Mode Bit 1: Set to 1 for enabling local_sleep_req Bit 4: Set to 1 for Standby Mode Bit 7: Set to 1 to enable WUR
A2D_REG_68	0x0444	0	wake_fwd_force_control	R/W	0x0	WAKE Output Value Force Control: 1b = Force Control Enable. Output value is set by 0x0444[1]
		1	wake_fwd_force_val	R/W	0x0	WAKE Output Force Value: 0b = Force low on WAKE pin if 0x0444[0] = 1 1b = Force high on WAKE pin if 0x0444[0] = 1
		2	goto_sleep_force_control	R/W	0x0	Sleep Mode Force Control: Set to 1 along with 0x0444[3] to force sleep mode
		3	goto_sleep_force_val	R/W	0x0	Sleep Mode Force Value: Set to 1 along with 0x0444[2] to force sleep mode

5 Power Supply Recommendation

5.1 Core Supply Network Recommendation

DP83TC812/3 doesn't have any restrictions with respect to supply sequencing of VSLEEP, VDDA, VDDIO/ VDDMAC. The sleep functionality in the PHY will be active immediately after the VLSEEP supply ramp is complete. The core functionality of the PHY will be active 10 ms after the last core power supply ramp is complete or after the device transitions from sleep to functional state whichever happens later.

In a system which needs the lowest current consumption in sleep mode, it is recommended to cut off the core supplies.

The image below shows some of the configurations of supply networks.

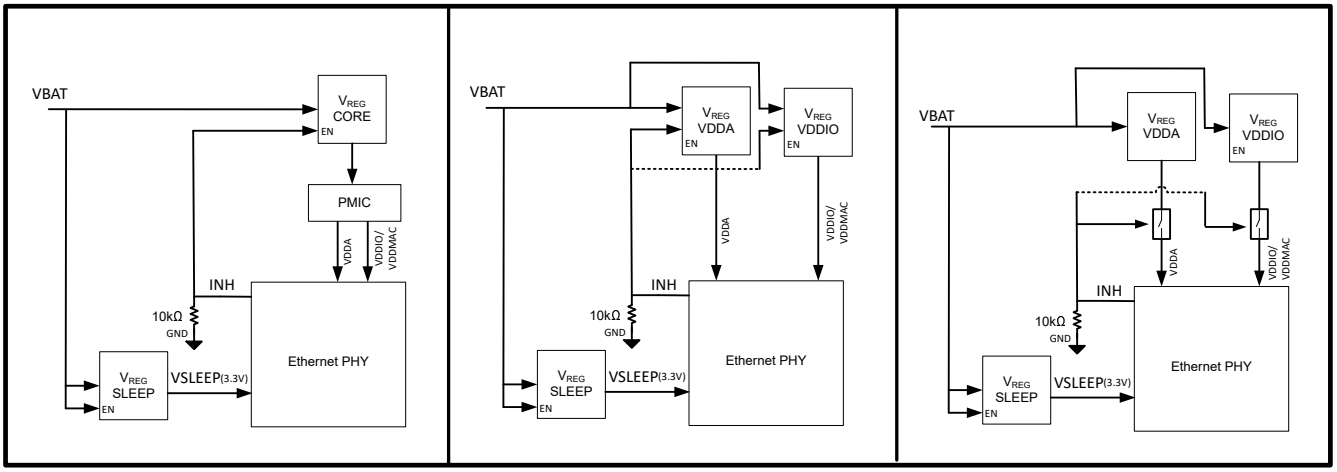

Figure 5-1. Core Supply Networks

The PHY doesn't malfunction even if the supplies are not cutoff. But, the current consumption of the PHY from the core supplies will be high. The table below shows the current comparison in sleep mode when supplies are cut off and when the supplies are intact.

Table 5-1. Current Consumption Comparison

S.No	Supply	Units	Current Consumption (Max)	
			Supplies Cut-off	Supplies Intact
1	VSLEEP	mA	0.018	0.018
2	VDDA	mA	0	50
3	VDDIO/VDDMAC (3.3 V)	mA	0	23
4	Total Current	mA	0.018	73

5.2 Networks with Shared Core Supplies

Many power supply networks share the PMIC between different PHYs available on the same PCB board to reduce the number of components and the board area.

In this case, the INH of the different PHYs can be connected together and this signal functions are Wired-OR (due to the open drain configuration of INH). The power supplies are cut-off only after all the PHYs are in sleep mode. Hence, there will be high current consumption from the supplies even though one or some of the PHYs are in sleep. The functionality of the PHYs in sleep will not be affected during this case. To achieve the lowest power consumption in the above case, PMIC must be separated for both the PHYs.

Figure 5-2 shows one of the examples where two PHYs share the same PMIC.

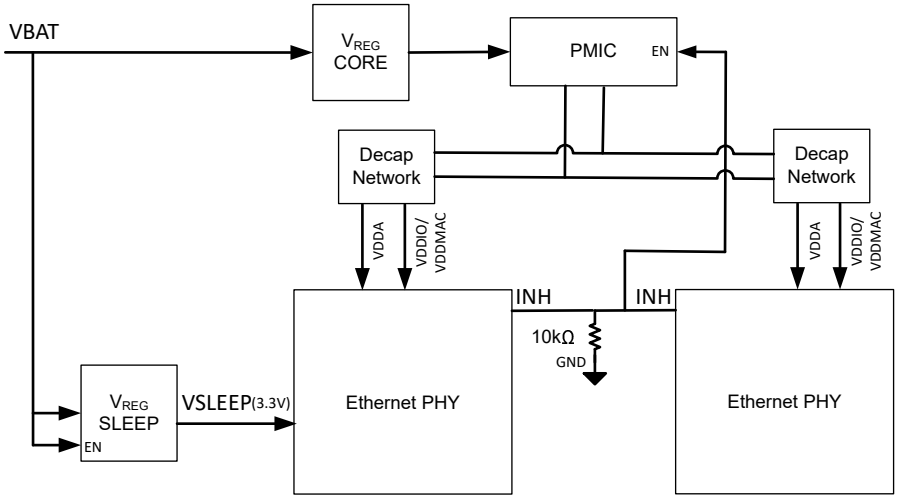

Figure 5-2. Power Network With Shared Core Supplies

6 Sequence of Events and Timing

6.1 Local Wake Timing

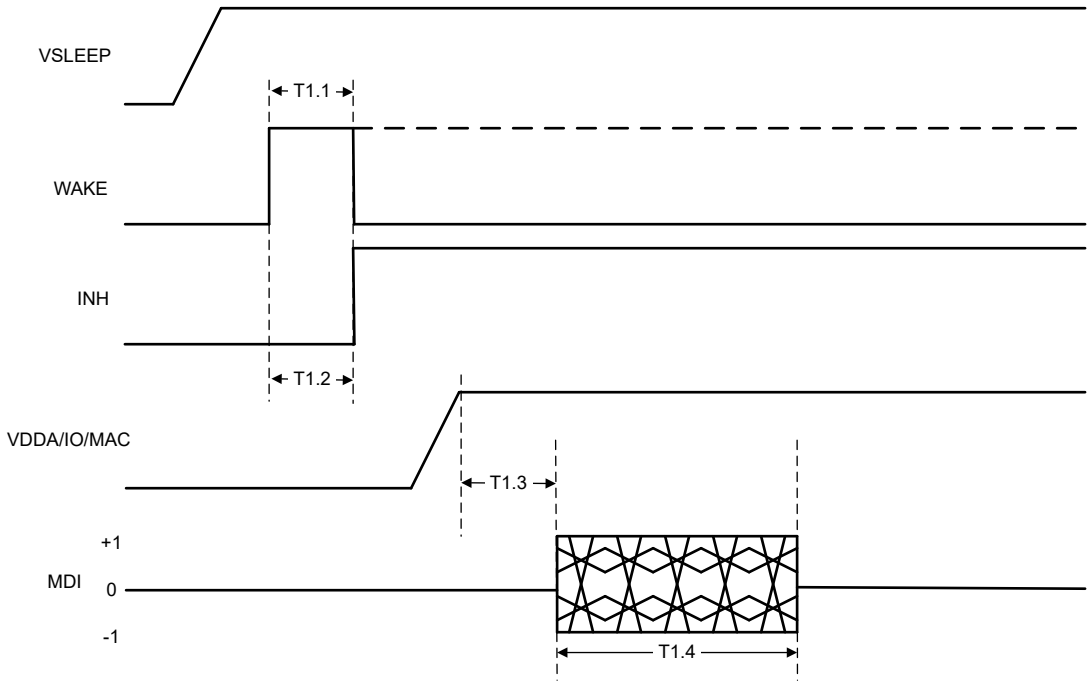

Figure 6-1. Timing - Local Wake

Table 6-1. Timing - Local Wake

Parameter	Description	Units	Min	Typ	Max
T1.1	Pulse width on WAKE pin which can successfully wake-up the device	µs	40		
T1.2	WAKE to INH delay	µs			40
T1.3	Supply ramp done to WUP transmission delay	ms			12
T1.4	Width of WUP transmitted by DP83TC812/3	ms	1		

6.2 Remote Wake Timing

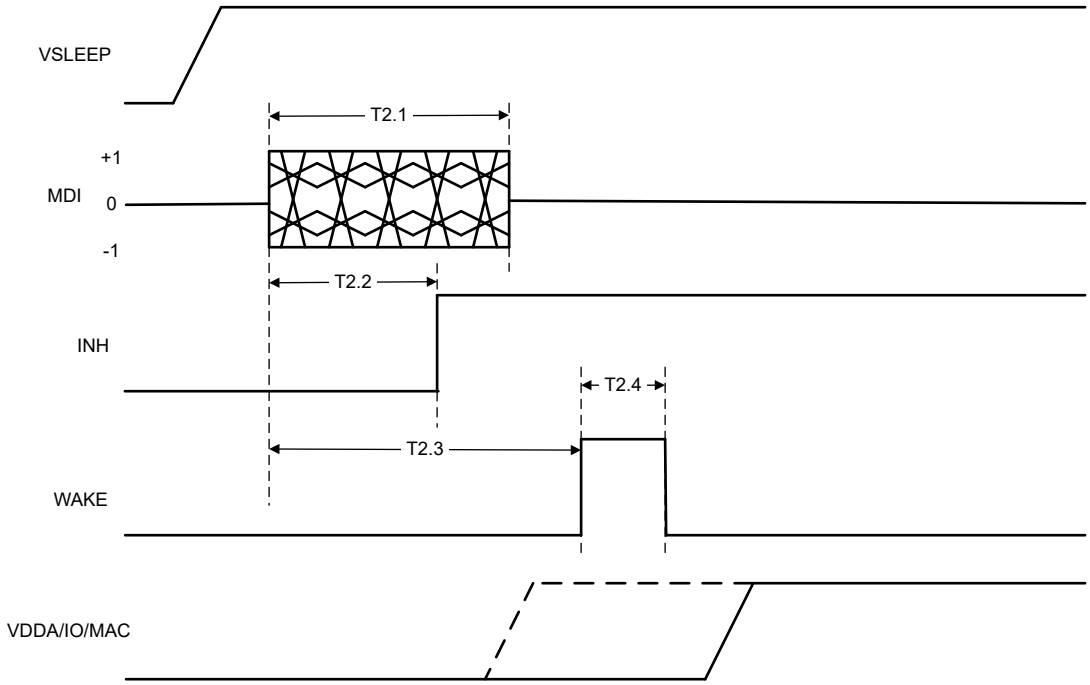

Figure 6-2. Timing - Remote Wake

Table 6-2. Timing - Remote Wake

Parameter	Description	Units	Min	Typ	Max
T2.1	Pulse width of WUP required by DP83TC812/3 for detection	ms	0.7		
T2.2	WUP to INH delay	ms			0.7
T2.3	WUP to Wake forward delay	ms			1.4
T2.4	Pulse Width of Forwarded Wake Pulse after remote wake	µs	48	80	120

6.3 Successful Sleep Negotiation Timing

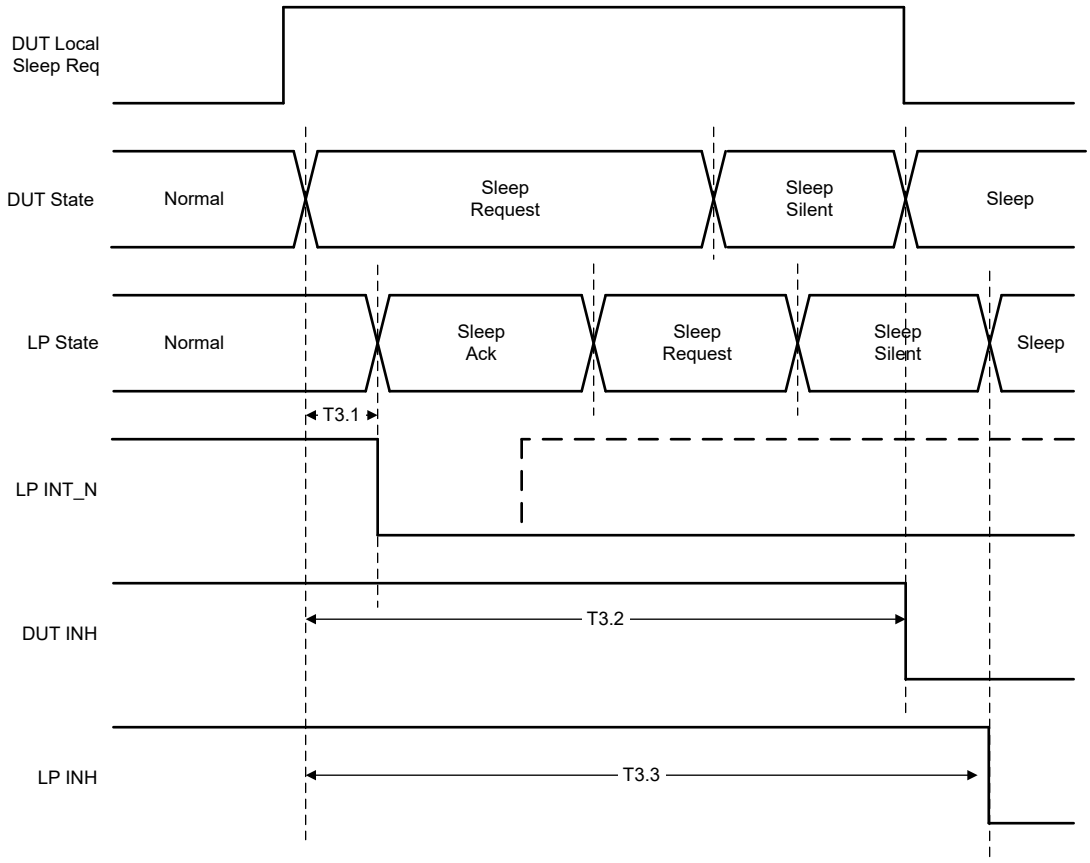

Figure 6-3. Timing - Successful Sleep Negotiation

Table 6-3. Timing - Successful Sleep Negotiation

Parameter	Description	Units	Min	Typ	Max
T3.1	Sleep Request on DUT to LPS Received Interrupt on LP delay (DP83TC812/3 LP)	µs			10
T3.2	Sleep Request on DUT to DUT Sleep delay	ms			10
T3.3	Sleep Request on DUT to LP Sleep delay	ms			10

6.4 Sleep Abort Timing

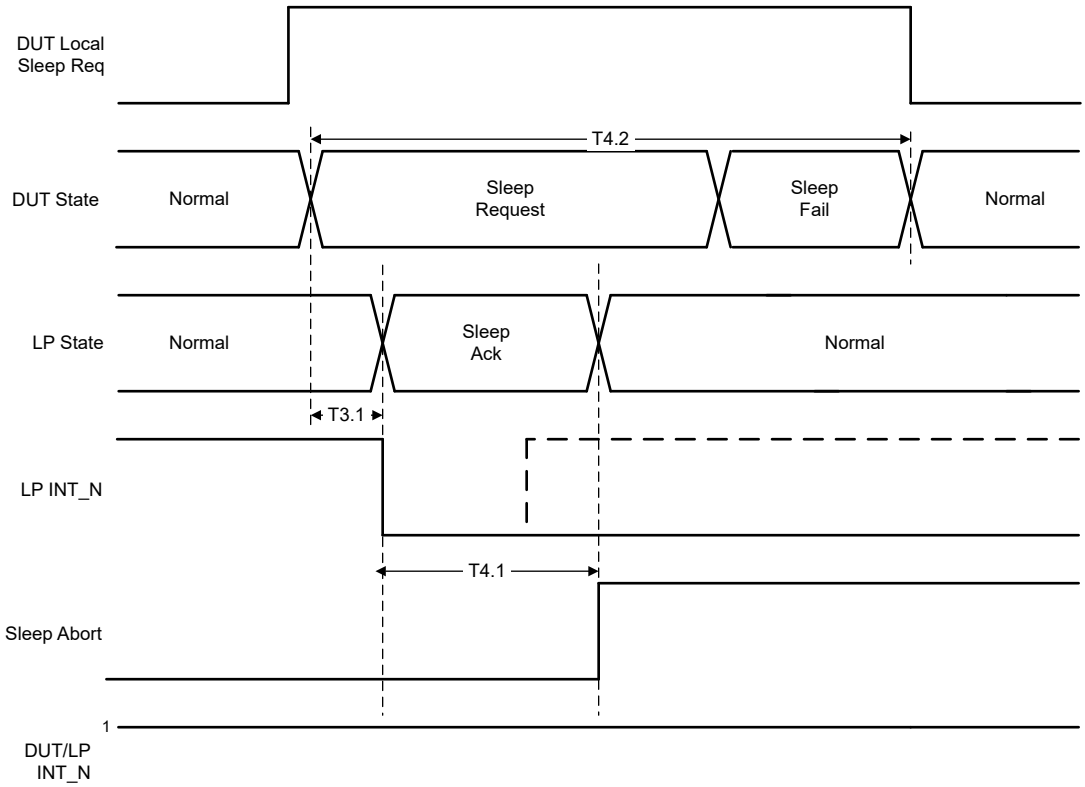

Figure 6-4. Timing - Sleep Abort by MAC

Table 6-4. Timing - Sleep Abort by MAC

Parameter	Description	Units	Min	Typ	Max
T4.1	Time available for MAC to abort sleep from Interrupt indication	ms			8
T4.2	DUT recovery to Normal mode delay	ms			16

6.5 WUR Timing

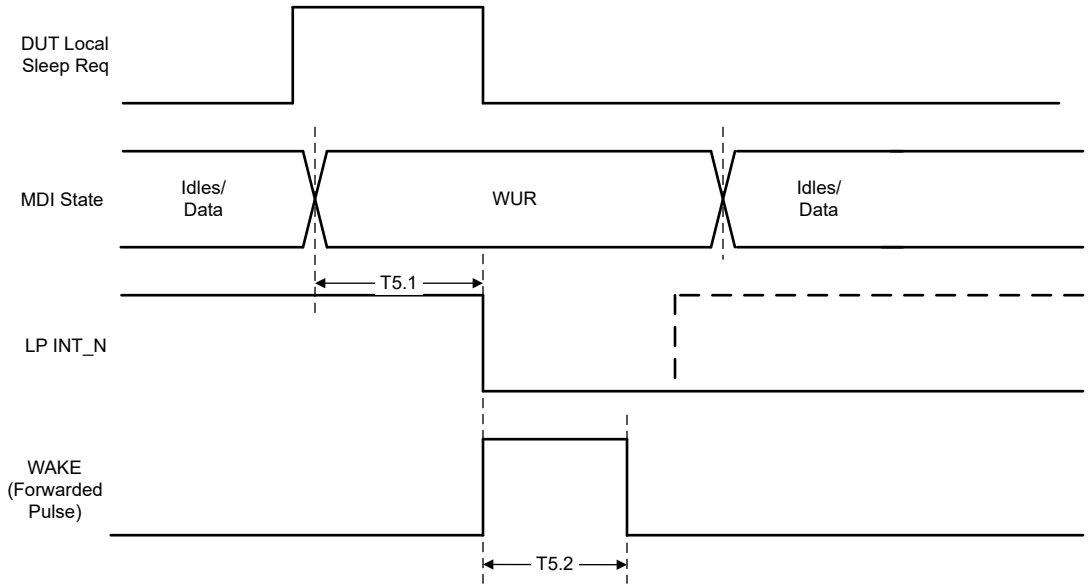

Figure 6-5. Timing - Wake-Up Request

Table 6-5. Timing - Wake-Up Request

Parameter	Description	Units	Min	Typ	Max
T5.1	WUR symbols to LP interrupt indication/Wake forward (DP83TC812/3 LP)	µs			10
T5.2	Width of Forwarded Wake pulse after WUR Reception	µs	50	50	

7 Ethernet Network Wake-up

Wake Forwarding feature in DP83TC812/3 can be leveraged for waking up the whole ethernet network. This section shows a simple ethernet network and timing of the wake-up of all the ethernet PHYs in the network.

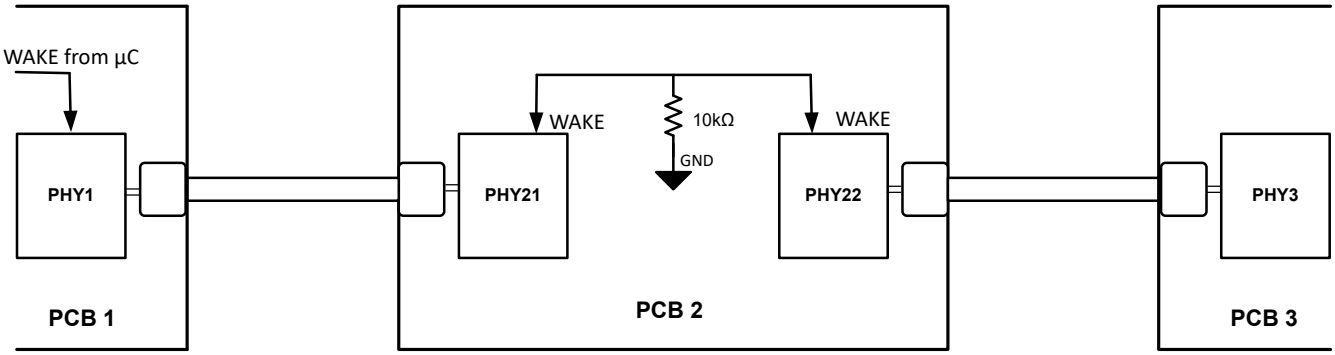

Figure 7-1. Simple Ethernet Network

When PHY1 wakes-up locally, it powers up and immediately transmits WUP. PHY21 wakes-up on reception of the WUP and immediately transmits >40µs pulse on the WAKE pin. Since the WAKE of PHY21, PHY22 are connected together, PHY22 wakes up after the reception of the >40µs pulse. PHY22 now wakes-up and then transmits WUP which wakes up PHY3.

The following image and table show the wake timing of this network.

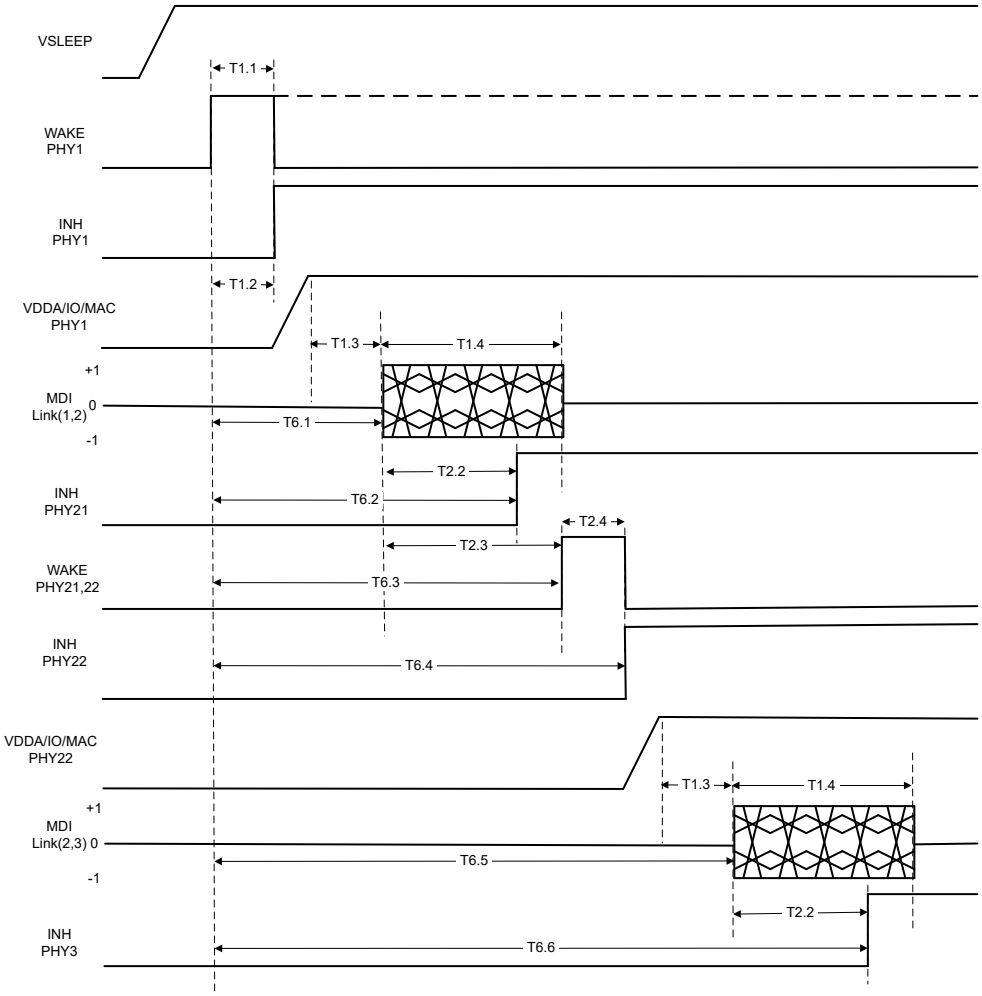

Figure 7-2. Timing - Network Wake

The timing numbers are derived based on assumption that power supplies are enabled immediately after INH is driven high and the total supply ramp time is 5 ms. All the timing numbers in the table are tabulated from start of WAKE on PHY1.

Table 7-1. Timing - Network Wake

Parameter	Event	Units	Min	Typ	Max
T6.1	WUP on MDI line(1,2)	ms			17.04
T6.2	INH high of PHY21	ms			17.74
T6.3	WAKE pulse output from PHY21	ms			18.44
T6.4	INH high of PHY22	ms			18.48
T6.5	WUP on MDI line (2,3)	ms			35.48
T6.6	INH high of PHY3	ms			36.18

8 Configuration for non-TC10 Applications

The following configuration is recommended for DP83TC812/3 in applications where TC10 sleep/wake-up functionality is not required.

Hardware Configuration

- VSLEEP pin can be connected to VDDA (or any 3.3 V supply source).
- WAKE pin should be pulled up to corresponding VSLEEP supply connection directly or through a resistor lower than 10 kΩ. WAKE pin can't be pulled up to VDDIO/VDDMAC supply.
- INH can be left floating.

Software Configuration

To disable the TC10 functionality, an additional setting ***reg<0x018B>[8] = 1*** should be programmed along with the other initialization settings.

9 Additional Features

9.1 WUR Initiation Through WAKE Pin

As mentioned in Section 3.2, WUR can be initiated through a register write. Apart from the register option, WUR can also be initiated from a PHY if a pulse of >40µs is driven on the WAKE pin of the PHY. To enable this feature, reg<0x017F>[15] = 1 should be programmed.

9.2 Programmable Wake-Forward Pulse Width

The width of the pulse forwarded on the WAKE pin when a PHY receives WUR is programmable. Table 9-1 shows the register write needed for each of the pulse width options available.

Table 9-1. WUR Wake Pulse Width

S.No	Width of pulse	Register Write
1	50 µs	0x0184[3:2] = 2'b00
2	500 µs	0x0184[3:2] = 2'b01
3	2 ms	0x0184[3:2] = 2'b10
4	20 ms	0x0184[3:2] = 2'b11

The forwarded wake-pulse when the device wakes up from sleep through WUP is not programmable.

10 Conclusion

This application note highlights the use of DP83TC812, DP83TC813 in TC10 sleep applications. DP83TC812, DP83TC813 are interoperable with different TC10 compatible PHYs and can be effectively used in any TC10 sleep/wake-up application.

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