Application Note

Ethernet, Clock and Data Recovery, and Temperature Optimization

Drew Miller

ABSTRACT

TI's Ethernet retimers are designed to function across a variety of data rates and operating conditions. One system in a retimer that plays a critical role is the clock and data recovery (CDR) system. This application note provides an introduction to the CDR system and some of the considerations that must be made when configuring the CDR system.

Table of Contents

1 Ethernet 2
2 Clock and Data Recovery 2
3 Temperature Optimization 3

List of Figures

Figure 2-1. CDR Jitter Transfer 2
Figure 3-1. Impact of Temperature on VCO Frequency 3

List of Tables

Table 1-1. Ethernet Data Encoding 2

Trademarks

1 Ethernet

Ethernet is a widespread industry standard for Local Area Networks (LAN) and is used in a variety of applications ranging from personal electronics to data centers. The Ethernet IEEE specification, IEEE 802.3, is incredibly broad and pertains to many different data rates and transmission mediums. However, one of the core functions of this specification is to standardize the physical media type and data rate used in various Ethernet systems. TI Ethernet retimers are able to lock to several of these data rates. Common Ethernet data rates that TI Ethernet retimers can lock to include 1 Gbps, 10 Gbps, and 25 Gbps. Besides the differences in data rate, there is also a difference in the encoding typically found at each of these data rates. This can be seen in Table 1-1.

Table 1-1. Ethernet Data Encoding

Ethernet Data Rate	Data Encoding
1 Gbps	8b/10b
10 Gbps	64b/66b
25 Gbps	64b/66b

In general, TI's Ethernet retimers are able to lock to any data rate that is within the device's VCO range and subrates of that frequency. For example, the DS110DF410's VCO can be set from 8.5 – 11.3 GHz. By setting the VCO to 10.3125 GHz and using a divider of 1, the device can lock to 10.3125 Gbps data. By setting the VCO to 10 GHz and using a divider of 8, the device can lock to 1.25 Gbps data. A wide range of VCO frequencies and subrates are supported across TI's Ethernet retimer family and additional details on these can be found in each device-specific data sheet.

2 Clock and Data Recovery

Clock and data recovery (CDR) is an important part of a retimer that is used to reduce the jitter that is transferred from a high-speed input to a high-speed output. This is accomplished by locking an internal voltage controlled oscillator (VCO) to the incoming data. Having an internal oscillator in phase with the input data enables the retimer to sample the data and then retransmit it.

CDR jitter transfer is limited by the phase locked loop (PLL) design. A PLL typically acts like a low-pass filter with regards to jitter. Low frequency jitter is typically passed through the CDR system, but high frequency jitter is typically removed from the CDR system. An example of CDR jitter transfers can be seen in Figure 2-1. The CDR bandwidth can typically be adjusted through retimer registers. This is detailed in the device-specific retimer programming guide. The impact of adjusting the CDR bandwidth is that the jitter transfer from input to output is also impacted. Reducing the bandwidth improves the jitter transfer, but limits the ability of the CDR system to track the input signal. Increasing the bandwidth increases the jitter transfer, but allows the CDR system to better track the input signal.

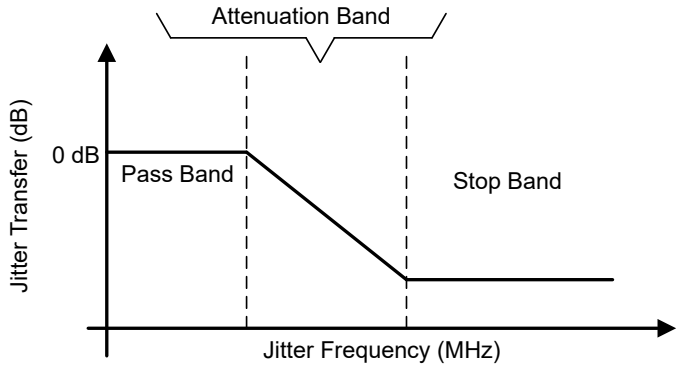

Figure 2-1. CDR Jitter Transfer

Typically, a certain frequency of data transitions is required in order to achieve CDR lock to the high-speed input. Data encoding ensures that transitions occurs even if the message being transmitted is all 0s or 1s. However, different sets of encoding results in the potential for longer runs of all 0s or all 1s. The impact of this is that a retimer designed for 64b/66b encoded data might struggle to lock to 128b/130b data. In practical implementations of TI's retimers, data encoding is typically not a concern since the retimer is designed to meet relevant criteria of the IEEE 802.3 specification.

For additional details about CDR, see https://training.ti.com/what-is-clock-and-data-recovery.

3 Temperature Optimization

When designing a system, it is important to consider the temperature range that the system may experience over the course of its operation. As it pertains to TI retimers, there are primarily two considerations that must be made. The first consideration is that the operating temperature of the device impacts the VCO of the CDR system. The second consideration is the impact of temperature on insertion loss.

Different temperatures create an offset in the VCO frequency vs VCO control voltage curve, shown in Figure 3-1.

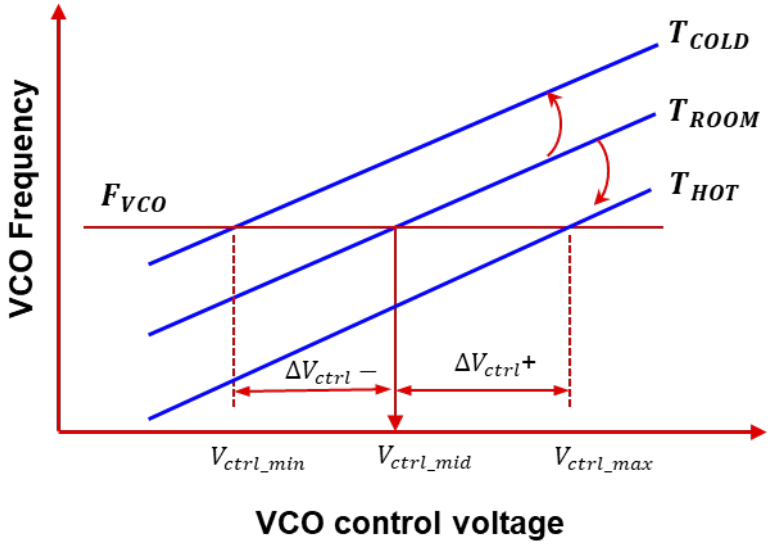

Figure 3-1. Impact of Temperature on VCO Frequency

By varying device temperatures, it is possible to disrupt the CDR lock. Temperature lock range (TLR) is the operating temperature range for which the CDR can reliably maintain lock. This can often be found in the device-specific retimer's data sheet. On TI's 25 Gbps and 28 Gbps retimers, it is also possible to compensate for temperature. For more information, see *DS2X0DF810 Junction Temperature Readback and Temperature Lock Range (TLR) Extension Procedures*.

Insertion loss typically increases as temperature increases. The amount of variation depends on the transmission medium and transmission length. A variation in insertion loss during retimer operation can impact the ability of the retimer to re-transmit data without errors. This is due to the fact that RX compensation in the retimer is typically only adapted when initially establishing CDR lock. Without re-adapting, insertion loss variation may impact the BER of the system. TI's 25 Gbps and 28 Gbps retimer families offer more flexibility in compensating for this than the 10 Gbps retimer family. In the 25 Gbps and 28 Gbps retimers, it is possible to enable continuous adaption of the DFE. This enables the retimer to adapt DFE while maintaining CDR lock. If DFE continuous adaption is enabled, the retimers are able to compensate for about ± 3dB of insertion loss variation. It may also be necessary to increase the tap weight of the 1st DFE tap since this tap is primarily responsible for compensating for insertion loss. Procedures for setting DFE continuous adaption and adjusting tap weights can be found in the programming guide for 25 Gbps and 28 Gbps retimers.

In general, TI's 25 Gbps and 28 Gbps retimer family offers more flexibility in designing a system that will experience large temperature swings while operating.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265