Application Note

DP83TC812, DP83TC813, and DP83TC814: Configuring for Open Alliance Specification Compliance

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ABSTRACT

Open Alliance (OA) mandates different tests for 100Base-T1 PHY. This document describes the procedure to put the DP83TC812, DP83TC813, and DP83TC814 (hereafter referred to as *DP83TC81x*) devices in the required test mode to carry out different Open Alliance tests.

The software and hardware configuration used during the testing of the DP83TC81x is found in this document. This configuration has been tested across different OA compliance houses: UNH, FTZ, and C&S and needs to be treated as a minimum requirement. Further improvement based on the system use-case of the customer is possible with additional hardware and software configuration.

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1 Introduction

The DP83TC81x was evaluated in accordance with the following OPEN Alliance (OA) specifications:

- OPEN Alliance 100BASE-T1 EMC Test Specification for Transceivers - Revision 2.0, by FTZ Zwickau
- OPEN Alliance 100BASE-T1 Interoperability Test Suite v1.0, by C&S Group, GmbH
- OPEN Alliance 100BASE-T1 test specifications for Physical Coding Sublayer (v. 1.0), PHY Control (v. 1.0), and Physical Media Attachment (v. 1.2) by the University of New Hampshire (UNH) Inter-Operability Lab.

This application note provides the details of unique hardware and software configuration used for all of the previously-listed tests.

Document also provides the required procedure details for these tests and this should assist customers implementing corresponding ECU level tests.

2 Hardware Configuration

2.1 Schematic

Schematics and the right components for MDI, reference clock, and power network are critical for the performance of 100Base-T1 PHY. This section captures the recommended schematics and component values used during OA TC-1 testing.

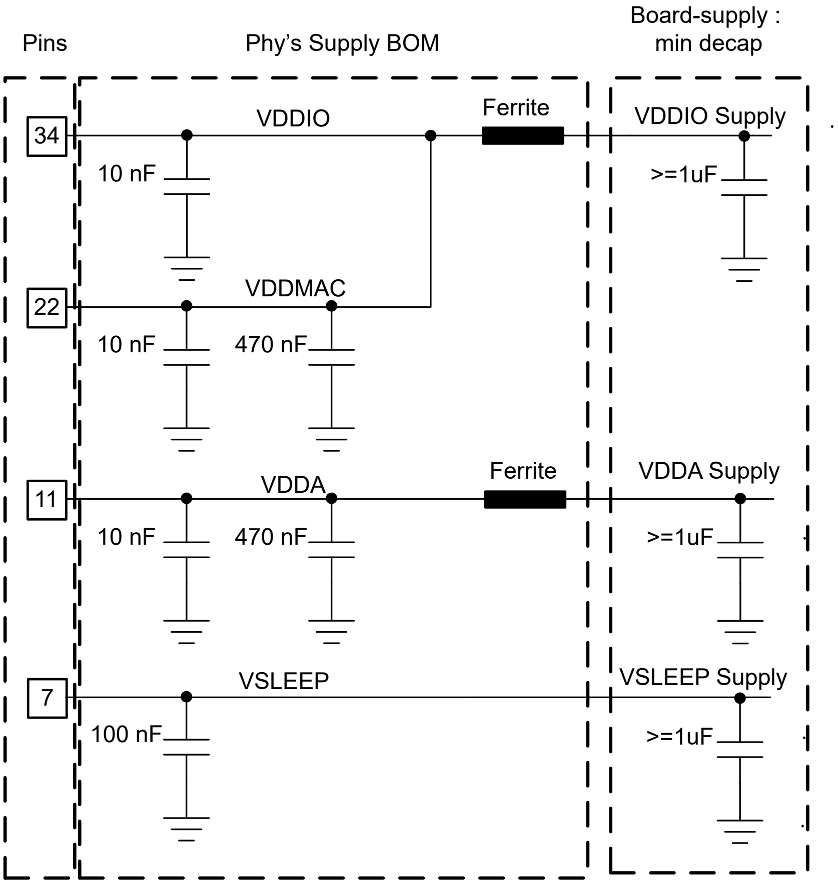

Figure 2-1. Power Supply Network: For Applications With Sleep Mode Requirement (DP83TC812)

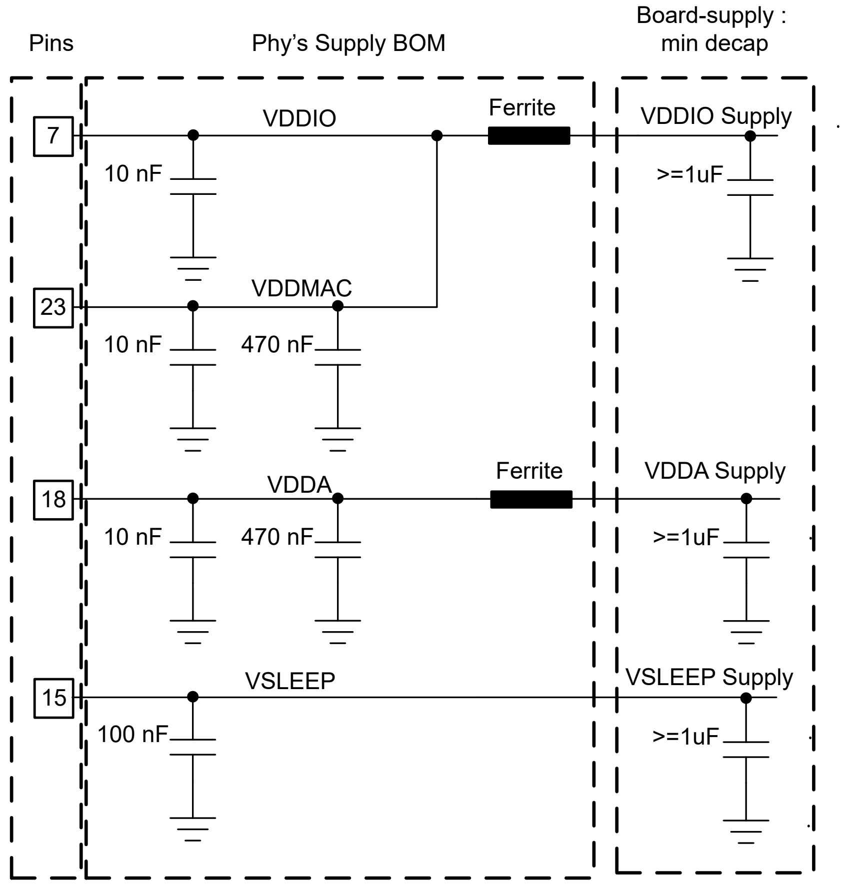

Figure 2-2. Power Supply Network: For Applications With Sleep Mode Requirement (DP83TC813)

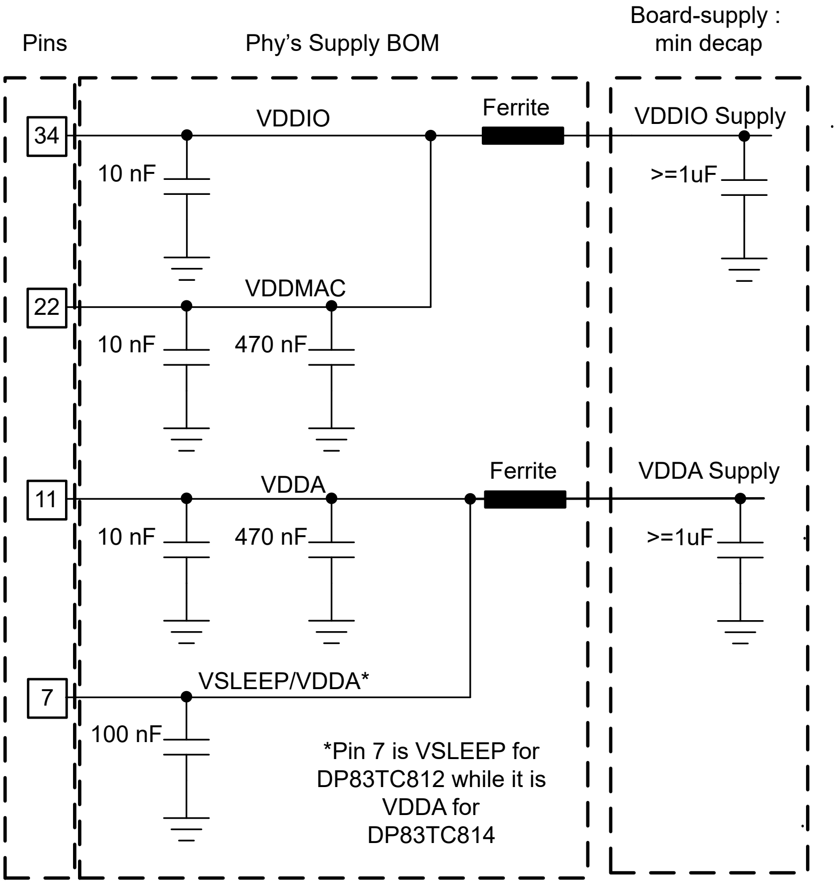

Figure 2-3. Power Supply Network: For Applications Without Sleep Mode Requirement (DP83TC812 and DP83TC814)

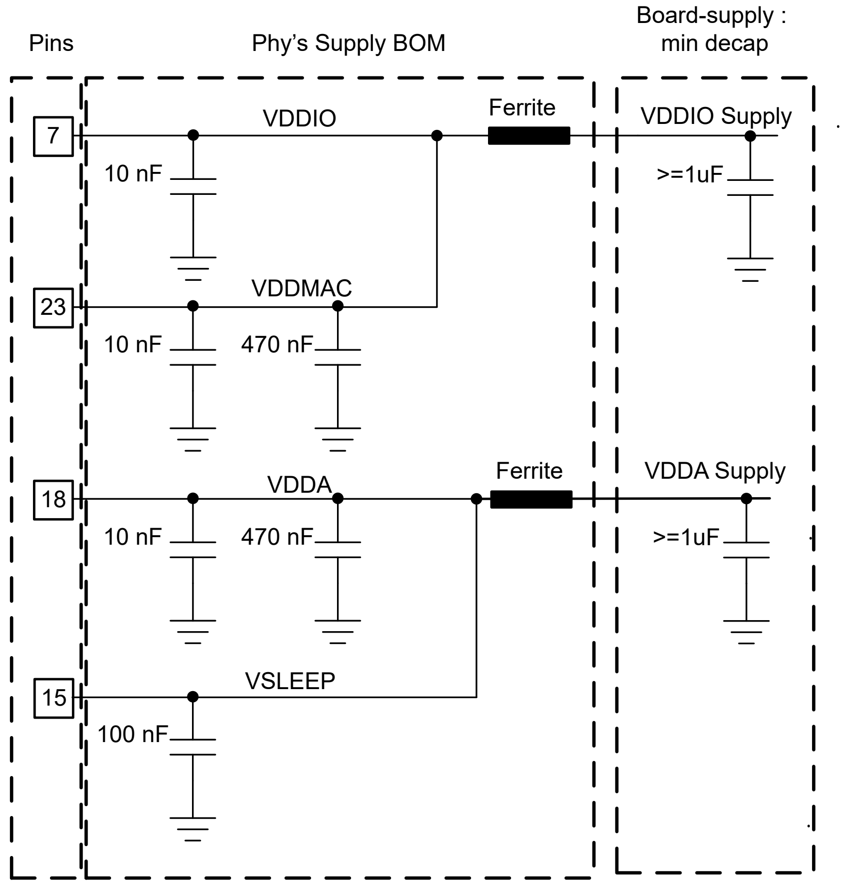

Figure 2-4. Power Supply Network: For Applications Without Sleep Mode Requirement (DP83TC813)

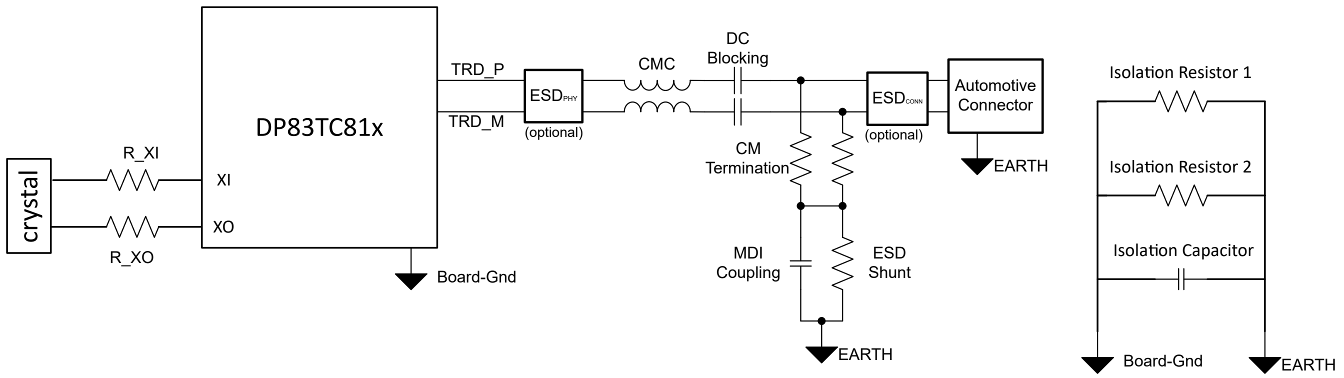

Figure 2-5. MDI and Crystal Schematic

Table 2-1. Parameters, Components, and Values

Parameter | Component	Value
V_{DDIO} | V_{DDMAC}	1.8V, 2.5V, or 3.3V
De-Coupling Capacitors V_{DDIO}	10nF
De-Coupling Capacitors V_{DDMAC}	10nF, 470nF
Combined Ferrite Bead for V_{DDIO} | V_{DDMAC} [1]	BLM18KG601SH1
V_{DDA}	3.3V
De-Coupling Capacitors V_{DDA}	10nF, 470nF
(Optional): Ferrite Bead for V_{DDA}	BLM18KG601SH1
V_{sleep}	3.3V
De-Coupling Capacitors V_{sleep}	0.1µF

Table 2-1. Parameters, Components, and Values (continued)

Parameter | Component	Value
DC Blocking Capacitors (1% accurate, 100V)	0.1µF
Common-Mode Choke	DLW43MH201XK2L, DLW32MH201XK2, AE2002, ACT1210L-201
Common-Mode Termination Resistors (1% accurate, 0.75 W, Size: 2010)	1 kΩ
MDI Coupling Capacitor	4.7nF
ESD Shunt (5% accurate, 0.125 W, Size: 0805	100 kΩ
Isolation Resistor 1 (0.25 W, Size: 1206)	0 Ω
Isolation Resistor 2 (0.25 W, Size: 1206)	0 Ω
Isolation Capacitor	Not populated
R_XI	100 Ω
R_XO	Minimum required for crystal wattage specification
ESD_{CONN} (Optional)	ESD devices qualified by *Open Alliance 100BASE-T1 EMC Test Specification for ESD suppression devices* with clamping voltage >100V and load capacitance < 5 pF. PESD1ETH1GLS-Q, for example.
ESD_{PHY} (Optional)	PESD2ETHX-Q. Connect V_{CC} pin to 3.3V rail. This adds protection if ethernet cable is shorted to battery, and from other transients <100V.

(1) If V_{DDIO} is separate from V_{DDMAC}, then additional ferrite bead and a 0.47-µF capacitor are required on V_{DDIO}. This ferrite bead has the same component number: BLM18KG601SH1.

3 Software Configuration

This section contains the register settings of DP83TC81x used during tests in different OA compliance test houses. These settings are recommended as the minimum requirement. Further parameters are available to be programmed if required by system- or board-level constraints. The default values listed are read upon power up or hard reset of the device.

The PHY supports bootstrap option to configure in Autonomous or Managed mode and it is in Autonomous mode by default. Managed mode strap option is recommended to prevent the link-up process from initiating while the software configuration from Table 3-1 and Table 3-2 is being executed. Once the software configuration is completed, the PHY can be removed from Managed mode by setting bit 0x18B[6] to ‘1’.

Table 3-1. Master Mode Configuration

MMD	REGISTER	VALUE	DESCRIPTION
1f	x001F	x8000	Hard reset
1f	x0523	x0001	To disable link-up start until configuration is complete
01	x0834	xC001	To configure PHY in Master mode
1f	x081C	x0FE2	Configuration for Interoperability
1f	x0873	x0021	Configuration for Interoperability
1f	x089E	x0010	Configuration for Interoperability
1f	x0874	x6866	Configuration for Interoperability
1f	x0875	x6868	Configuration for Interoperability
1f	x0812	x00F2	Configuration for Interoperability
1f	x0816	x0300	Configuration for Interoperability
1f	x0806	x293A	Configuration for Interoperability
1f	x0807	x3348	Configuration for Interoperability
1f	x0808	x3D56	Configuration for Interoperability
1f	x083E	x045F	Configuration for Interoperability
1f	x0834	x8000	Configuration for Interoperability
1f	x0843	x4639	Configuration for Interoperability
1f	x0862	x0330	Configuration for Interoperability
1f	x0896	x32CB	Configuration for Interoperability
1f	x003E	x0009	Configuration for Interoperability
1f	x0830	x0143	Configuration for Interoperability
1f	x0820	x03AA	Configuration for Interoperability
1f	x0826	x1407	Configuration for Interoperability
1f	x083D	x0047	Configuration for Interoperability
1f	x080A	x0015	Configuration for Interoperability
1f	x0831	x0703	Configuration for Interoperability
1f	x0856	x0600	Configuration for Interoperability
1f	x0857	x0500	Configuration for Interoperability
1f	x0858	x0500	Configuration for Interoperability
1f	x0859	x0500	Configuration for Interoperability
1f	x0411	x3F09	Configuration for Interoperability
1f	x0456	x0021	Reduce the slew rate of MAC interface IO drivers
1f	x0452	x0303	**(Optional):** Disable CLKOUT and LED outputs to reduce emissions
1f	x0453	x0003	
1f	x045F	x000F	
1f	x085A	x3000	Configuration to improve RF immunity performance
1f	x085B	x3000	

Table 3-1. Master Mode Configuration (continued)

MMD	REGISTER	VALUE	DESCRIPTION
1f	x0189	x0018	Configuration for TC10 Interoperability
1f	x018B	x144B	
1f	x041C	x8802	Configuration for Interoperability
			Wait 0.01ms
1f	x041C	x0000	Configuration for Interoperability
			Wait 1ms
1f	x0514	x0640	Configuration for Interoperability
1f	x0514	x0600	Configuration for Interoperability
1f	x001F	x4000	Soft reset
1f	x0523	x0000	Enable link-up start after end of configuration
1f	x0431	x3B90	**Only needed in RGMII TX/RX shift mode and RMII mode. Not needed in RGMII align, SGMII, or MII modes.** Registers for RX_CLK to turn on reliably.
1f	x0431	x3B80	

Table 3-2. Slave Mode Configuration

MMD	REGISTER	VALUE	DESCRIPTION
1f	x001F	x8000	Hard reset
1f	x0523	x0001	To disable link-up start until configuration is complete
01	x0834	x8001	To configure PHY in Slave mode
1f	x0862	x0330	Configuration for Interoperability
1f	x086E	x1868	Configuration for Interoperability
1f	x0812	x00F4	Configuration for Interoperability
1f	x0816	x0300	Configuration for Interoperability
1f	x0873	x0021	Configuration for Interoperability
1f	x0896	x22FF	Configuration for Interoperability
1f	x089E	x0000	Configuration for Interoperability
1f	x0411	x3F09	Configuration for Interoperability
1f	x0456	x0021	Reduce the slew rate of MAC interface IO drivers
1f	x0452	x0303	**(Optional):** Disable CLKOUT and LED outputs to reduce emissions
1f	x0453	x0003	
1f	x045F	x000F	
1f	x085A	x3000	Configuration to improve RF immunity performance
1f	x085B	x3000	
1f	x0189	x0018	Configuration for TC10 Interoperability
1f	x018B	x144B	
1f	x041C	x8802	Configuration for Interoperability
			Wait 0.01ms
1f	x041C	x0000	Configuration for Interoperability
			Wait 1ms
1f	x0514	x0040	Configuration for Interoperability
1f	x0514	x0000	Configuration for Interoperability
1f	x001F	x4000	Soft reset
1f	x0523	x0000	Enable link-up start after end of configuration
1f	x0431	x3B90	**Only needed in RGMII TX/RX shift mode and RMII mode. Not needed in RGMII align, SGMII, or MII modes.** Registers for RX_CLK to turn on reliably.
1f	x0431	x3B80	

4 Testing PMA

OA TC-1 specifies different electrical tests for the front end of the 100Base-T1 PHY. Different test modes have been specified in the standard document. In each test mode, PHY is supposed to generate patterns on MDI lines or expose internal clock signal on a pin for measurement of different electrical parameters.

DP83TC81x supports all these test modes. This section gives details of the required configuration to enter into each test mode.

A detailed PMA test report from UNH (OA compliance test house) with OA- and IEEE-compliant results is available on request.

4.1 PMA Testing Procedure

Note

- Before programming any of the test modes, DP83TC81x need to be loaded with the respective initialization register configuration (master or slave) as described in Section 3.

Table 4-1. Programming PMA Test Modes

TEST MODE	MMD	REGISTER	VALUE
Test Mode 1	x01	0x0836	0x2000
Test Mode 2	x01	0x0836	0x4000
Test Mode 4: Tx_Tclk 25 MHz on the CLKOUT pin.	x01	0x0836	0x8000
	x1F	0x045F	0x000D (DP83TC812/814) 0x0007 (DP83TC813)
Test Mode 5	x01	0x0836	0xA000

5 Testing IOP: Link-up and Link-down

OA TC-1 specifies different PHY level tests to test link-up time, link-down time, and link stability. This section highlights the test sequence used for these IOP tests for PHY-level testing and the same can be ported for ECU level tests.

TC-1 interoperability tests are carried out by OA compliance test house C&S. To test interoperability of DP83TC81x, C&S tests each of these parameters with DP83TC81x and other 100Base-T1 certified PHYs as its link-partners. Each of these parameters are tested for a large number of iterations over different temperatures and cable lengths.

A detailed IOP test report from C&S with OA compliant results is available on request.

5.1 IOP Testing Procedure

Use the following IOP testing procedure:

- Start of measurement:

  For the IOP tests measuring link-up time either after power-up or after hardware reset, it is important to start the measurement of link-up time after the initialization configuration is loaded back into DP83TC81x. As the configuration is loaded into the PHY by a controller, we recommend the controller to give an indication (a software bit or an IO state) after the last configuration register is written. This indicator going high is the start of measurement of link-up time.
- Status to be polled:

  Link-status is indicated by bit 2 of register 0x1: 1 = link-up; 0 = link-down. This needs to be polled to indicate the event of link-up or link-down during these tests.

Note

- If system desires no automatic link-up after power-up (link to only happen after writing the initialization script), managed mode of DP83TC81x should be used by using strap on pin LED_1.
- The PHY supports the bootstrap option to configure in Autonomous or Managed mode and it is in Autonomous mode by default. Managed mode strap option is recommended to prevent the link up process from initiating while the software configuration is being executed. Once the software configuration is completed, the PHY can be removed from Managed mode by setting bit 0x18B[6] to 1.

6 Testing SQI

SQI gives the indication of signal quality on the copper cable.

OA TC-1 indicates that SQI values should decrease monotonically with increase in noise levels.

A detailed SQI test report from C&S with OA compliant results is available on request.

6.1 SQI Value Interpretation

Register bits 0x871[3:1] contain the SQI value. This register can be polled to understand the appropriate range of MSE values for each SQI value.

Table 6-1. SQI Values for Register Bits 0x871[3:1]

0x871 [3:1]	OPEN ALLIANCE SQI	MSE VALUES
0x0	SQI = 0 (Worst)	MSE > 133
0x1	SQI = 1	11 < MSE ≤ 133
0x2	SQI = 2	7 < MSE ≤ 11
0x3	SQI = 3	5 < MSE ≤ 7
0x4	SQI = 4	4 < MSE ≤ 5
0x5	SQI = 5	3 < MSE ≤4
0x6	SQI = 6	2 < MSE ≤ 3
0x7	SQI = 7 (Best)	MSE ≤ 2

7 Testing TDR

This section describes the procedure to test cable faults: open or short.

A detailed TDR test report from C&S with OA-compliant results is available on request.

Note

OA TC-1 tests done at C&S tests are for open and short cable fault test cases. Also TDR is usually run to find the root-cause when there is no link. The test procedure described in Section 7.1 has an extra step over the compliance test procedure: to force link-down condition when possible (use if required).

7.1 TDR Testing Procedure

Table 7-1. TDR Run Procedure

SEQUENCE	DESCRIPTION	REGISTER READ/WRITE
Step 1: For DP83TC81x as master	Force the link-down by writing register and enable link-partner to go silent. In case of valid open and short cable faults, TDR still works fine without step 1. For good cable case, TDR register 0x001E may show *Fail* on bypassing this step.	Write Reg[0x1834] = 0x8001 To make master go silent.
Step 1: For DP83TC81x as slave	Force the link-down by writing register and enable link-partner to go silent. In case of valid open and short cable faults, TDR still works fine without step 1. For good cable case, TDR register 0x001E may show *Fail* on bypassing this step.	If DP83TC81x is link partner, write reg[0x1834] = 0x8001 on the link partner to make it silent. If other PHY is used, contact the vendor for register write to make link partner silent

Step 2	TDR configuration: Pre-run	Reg[0x0523] = 0x0001 //Transmit disable
		Reg[0x0827] = 0x4800
		Reg[0x0301] = 0x1701
		Reg[0x0303] = 0x023D
		Reg[0x0305] = 0x0015
		Reg[0x0831] = 0x3003
		Reg[0x001F] = 0x4000
		Reg[0x0523] = 0x0000 //Transmit enable
		Reg[0x001F] = 0x0000

Step 3	Start TDR	Reg[0x001E(15)] = 1
Step 4	Wait for 100 ms (Sufficient for TDR to converge for maximum cable length)	
Step 5	Read 0x001E[1:0] = [TDR done : TDR fail]. Value should be [1,0]. Fault type and locations are valid only if this correct value is read. Value other than [1,0] means that there is some noise on the line which is causing TDR to fail.	

Table 7-1. TDR Run Procedure (continued)

SEQUENCE	DESCRIPTION	REGISTER READ/WRITE	
Step 6	Fault type and location is read.	Read Reg 0x0310 for fault status and fault type. For fault types:	
		TDR_TC-1 Reg 0x0310[7] = peak_detect	
		0b	Fault not detected
		1b	Fault detected
		TDR_TC-1 Reg 0x0310[6] = peak_sign	
		0b	short
		1b	open
		**peak_sign only valid if Fault detected in cable If a valid fault detected: register 0x0310[5:0] = is the fault location in meters.	

8 Testing EMC and EMI

OA TC-1 specifies conducted EMC and EMI tests. For DP83TC81x, these tests were carried out in OA compliance test house FTZ and testing of emissions on MDI, emissions on each supply pin, immunity to RF signals are part of the test suite. The board was designed in accordance with OA specifications by FTZ.

Hardware and software configurations highlighted in the document were used for these conducted EMC and EMI tests. Configurations are available if further enhancement over TC-1 specs are required for an application.

A detailed test report from FTZ with procedures and OA-compliant results is available on request.

Other than conducted emission tests (for OA TC-1 compliance), DP83TC81x (with mentioned hardware and software configuration) has been tested against different radiated emission and radiated immunity requirements of different OEMs. Details of radiated emission and immunity test results are available on request. Configurations are available if further enhancement of margins is required for an application.

9 Revision History

Changes from Revision E (February 2025) to Revision F (August 2025) **Page**

- Added optional ESD diode recommendation for MDI pins.......... 2
- Added register 0x431 writes to turn on RX_CLK reliably in RGMII shift and RMII modes.......... 7

Changes from Revision D (January 2025) to Revision E (February 2025) **Page**

- Added delays after writes to register 0x41C.......... 7

Changes from Revision C (July 2024) to Revision D (January 2025) **Page**

- Updated Master and Slave configuration for Interoperability.......... 7
- Removed 0x0306 write from TDR Pre-run. Removed 0x310[8] indication. Changed value of register 0x0831 to 0x3003.......... 13

Changes from Revision B (April 2024) to Revision C (July 2024) **Page**

- Updated Master and Slave configuration with additional registers.......... 7

Changes from Revision A (May 2022) to Revision B (April 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Updated 0x18B[6].......... 7
- Deleted Test Mode 1 note comment.......... 10
- Updated *0x18B[6] to 0* to *0x18B[6] to 1* 11
- Added 0x0831=0x0903 write to TDR pre-run configuration.......... 13

Changes from Revision * (December 2021) to Revision A (May 2022) **Page**

- Added support for DP83TC813 and DP83TC814 devices throughout the document.......... 1
- Added ESD component description to *Parameters, Components, and Values*. Added optional notice for VDDA decoupling capacitor. Updated ferrite bead recommendation for VDDIO or VDDMAC. Added footnote for VDDIO and VDDMAC ferrite bead. Modified figures to include pertinent information relating to DP83TC813 and DP83TC814.......... 2
- Added *Power Supply Network: For Applications With Sleep Mode Requirement (DP83TC813)*, *Power Supply Network: For Applications Without Sleep Mode Requirement*, *Typical DP83TC814 Application with Peripheral* figures.......... 2
- Updated Test Mode 4 command for DP83TC813.......... 10

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