Technical White Paper

Connecting Zonal Automotive Architectures with PCIe

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ABSTRACT

As Original Equipment Manufacturers (OEMs) and Tier-1s prepare to support technological advances in both Advanced Driver Assistance Systems (ADAS) and vehicle connectivity, they are rethinking the automotive data backbone architecture. To enable distributed processing in zonal architectures, the automotive data backbone must employ high-speed interfaces that support high bandwidth and low latency. In particular, careful consideration for ultra-low latency must be taken when the shared data is used for safety-critical real-time processing. The Peripheral Component Interconnect Express (PCIe®) ecosystem is emerging in popularity as an interface well-equipped to serve the automotive industry in the same way it already serves the industrial data center market. This technical white paper addresses industry trends in automotive backbone architectures and focuses on advantages and tradeoffs of PCIe compared to other interface technologies. In addition, this paper explains how signal conditioning devices such as redrivers and retimers are essential to enabling the reach extension and link margin required in harsh automotive environments.

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Trademarks

1 Introduction – Automotive Industry Trends in ADAS and Vehicle Connectivity

In recent years, the automotive industry has witnessed an impressive growth in computing throughput as data integration, machine-learning (ML), and artificial intelligence (AI) have become an integral part of the automotive ecosystem. According to a 2020 report by Global Market Insights, the market size for advanced driver assistance systems (ADAS) is expected to grow from a $35 billion industry in 2019 to over $60 billion by 2026 with >10% compound annual growth rate (CAGR). Such significant expansion is attributed to increasing vehicle safety regulations and driver assistance capabilities as vehicles reach full autonomy. With the onset of 5G networks revolutionizing vehicle-to-everything (V2X) connectivity for connected car applications, computing needs will further increase to enhance vehicle connectivity. Gone are the days of electronic control units (ECUs) that perform a singular function in an isolated environment. Today's vehicles resemble *data centers on wheels* comparable to traditional High-Performance Computing (HPC) platforms deployed in enterprise servers.

As Original Equipment Manufacturers (OEMs) and Tier-1s prepare to support technological advances in both ADAS and vehicle connectivity, they are rethinking the automotive data backbone architecture. Rather than rely on computing to be implemented based on domains (for example, ADAS domain), future automotive data backbones are shifting from domain to zonal architectures. This is accomplished by incorporating local computing nodes, or *zone controllers*, to connect ECUs and interfaces based on location within their *zone*, regardless of their respective domain. These zone controllers then connect to a powerful central compute node that handles the data accordingly. The value of the zonal architecture approach is three-fold:

1. **Reduction in Overall ECUs and Cable Weight:** By connecting ECUs and interfaces based on location rather than domain while incorporating more processing into a central computing node, the total number of ECUs and total weight of cables can be significantly reduced.
2. **Distribution of Processing Resources**: It is economically infeasible to assemble a processor in a single package that has the computing power to handle the entire amount of Tera-Operations per second (TOPS) needed for full vehicle autonomy. Through shared processing enabled by the zone controllers and central compute node, the overall computing throughput and utilization of memory resources (e.g. solid-state drives (SSDs)) are optimized without over-stressing the system.
3. **Processing Redundancy**: Backup processing options are needed to mitigate the risk of a singular point-of-failure. System redundancy, particularly by connecting physically distant zone controllers in a ring, presents an attractive option to avoid a failure scenario where one specific region of the vehicle is affected.

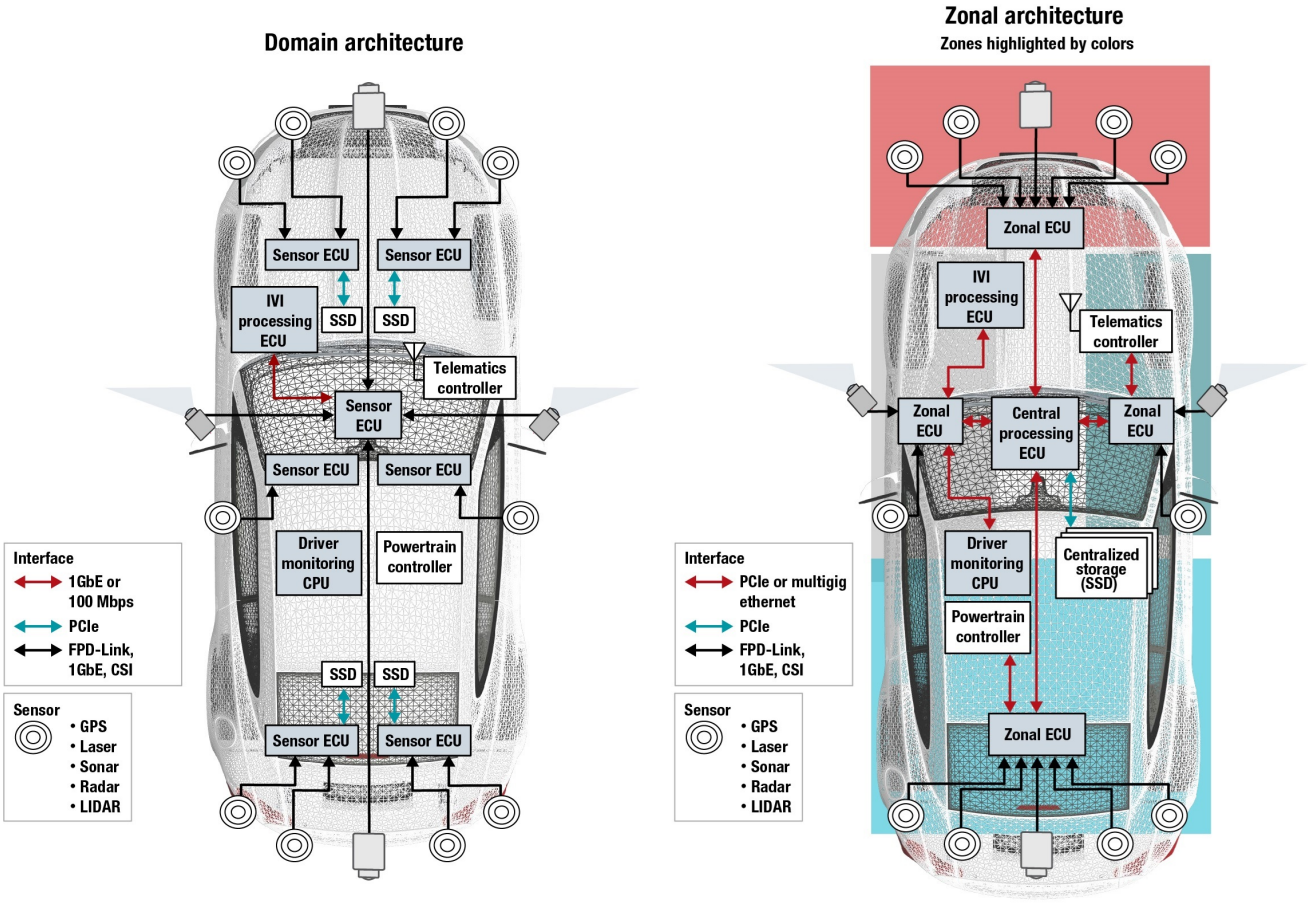

Figure 1-1. Domain Architecture vs. Zonal Architecture

In zonal automotive architectures, high-speed interfaces are required that enable both high bandwidth and low latency. In situations where safety-critical real-time processing is implemented, ultra-low latency becomes a must-have requirement. Fortunately, there is no need to re-invent the wheel when seeking an appropriate interface for these applications. The Peripheral Component Interconnect Express (PCIe®) ecosystem has successfully met the high bandwidth, ultra-low latency performance demands in industrial data centers, and this interface is well-suited to be used in a similar fashion for the automotive industry.

2 PCIe for Automotive ECU-to-ECU Interconnects

2.1 Advantages of PCIe Technology

PCIe is not new to automotive. In fact, PCIe has an extensive history as an intra-ECU, board-to-board interface between processors and automotive network interface cards (NICs) for years.

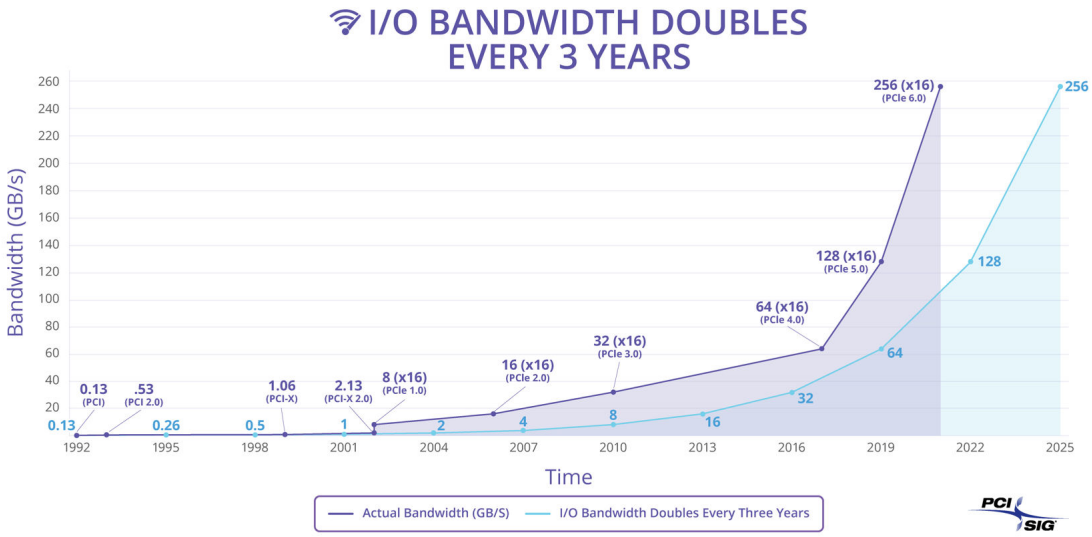

Figure 2-1. PCIe Historical Bandwidth Support for High-Speed Interconnects (source: PCI-SIG)

There are several key advantages to using PCIe:

1. **Bandwidth Scalability:** As cited by the PCI-SIG standards body, the PCIe bandwidth has doubled with each generation (for example, 8 GT/s for PCIe 3.0, 16 GT/s for PCIe 4.0, and 32 GT/s for PCIe 5.0), enabling designers to implement a future-proof interface that scales with increasing bandwidth needs. PCIe also offers flexible link widths, where parallel lanes can easily expand the bandwidth from x1 to x2, x4, x8, or x16.
2. **Ultra-Low Latency and Reliability:** PCIe incorporates minimal data overhead and guaranteed reliable transport on the hardware level, reducing latency to the order of tens of nanoseconds. Comparatively, traditional networking technologies like Ethernet rely on software-level handling in the TCP/IP layer to manage data integrity and transport reliability, resulting in overhead that increases latency to the order of several microseconds. This order-of-magnitude difference in latency, multiplied across end-to-end automotive interconnects, creates significant challenges for automotive applications with real-time needs (for example, ADAS and V2X).
3. **Direct Memory Access (DMA):** PCIe provides a built-in DMA method without packetization to reduce CPU processing overhead resources. This further optimizes latency for remote shared storage use cases. Whereas other interface technologies incur a cost in CPU cycles access, copy, and buffer memory data from another domain, ease of DMA implementation in PCIe allows processors to access shared memory efficiently as if the memory were locally available.
4. **PCIe Ecosystem Breadth:** PCIe is non-proprietary and well-adopted by central processing units (CPUs), graphics processing units (GPUs), and hardware accelerators across a vast array of vendors. Its pervasiveness across the industry enables flexible interoperability with off-the-shelf components and readily available IP blocks. Moreover, various elements of the networking ecosystem are beginning to support PCIe natively, including SSD storage and PCIe-based switch fabrics with non-transparent bridging (NTB) topologies.

2.2 PCIe and Multigig Ethernet Co-Existence in the Automotive Data Backbone

PCIe and Ethernet co-exist as essential interfaces for the automotive data backbone. Presently, PCIe is mostly contained to intra-ECU processor connections only, whereas high-speed inter-ECU connectivity over automotive cabling is predominantly enabled by automotive Ethernet. Automotive Ethernet serves well as an ideal inter-ECU interface due to the creation of NBASE-T1 standards for full duplex signaling of TX and RX over a single differential pair. With the ratification of the Multigig Ethernet standard IEEE802.3ch in 2020, Ethernet bandwidth further increases to support up to 10 Gbps (10GBASE-T1) over a single shielded twisted pair (STP) cable up to 15 m. With a minimal cabling interface, OEMs have used automotive Ethernet to reduce overall cable count significantly and optimize fuel economy due to reduced cable weight. For high-bandwidth inter-ECU cabling applications where minimal cable count is prioritized over real-time processing and maximized TOPS, automotive Ethernet will continue to provide numerous benefits as a high-speed interface.

As the automotive industry trends towards shared processing and redundancy across the data backbone, transporting native PCIe end-to-end beyond the PCB becomes increasingly attractive in comparison to the traditional method of converting PCIe via NIC to Ethernet for cabling interconnect and then converting back to PCIe at the destination ECU. By converting one interface technology to another, the inherent benefits of PCIe are lost. Instead, processors connected end-to-end by native PCIe can exploit the benefits of the protocol's ultra-low latency, guaranteed reliability, and DMA that are critical for maximizing computational efficiency and optimizing real-time processing performance. For high-bandwidth inter-ECU cabling applications where both real-time processing and maximized TOPS are prioritized over cable count, PCIe emerges as a worthy and valid high-speed complement to automotive Ethernet.

3 PCIe Signal Conditioning for Intra-ECU and Inter-ECU Interfaces

Redrivers and retimers are needed to recover and counteract the additional insertion loss and signal-to-noise ratio degradation that naturally occur when transporting PCIe over lossy media, whether that is through PCB or automotive cable channels. Both redrivers and retimers have a deep-rooted history in the PCIe ecosystem. Redrivers have been a part of the PCI-SIG Integrator's List of approved components since PCIe 2.0. Meanwhile, retimers formally became part of the PCIe Base Specification since PCIe 4.0. TI offers the industry's largest portfolio of PCIe redrivers, retimers, and passive switches to address a multitude of industrial and automotive use cases.

Table 3-1. Linear Redriver vs. Retimer Comparison

PCIe Linear Redriver (1)	PCIe Retimer
Low power consumption solution (no heat sink is required)	High power consumption solution (most cases require heat sink)
Ultra-low latency (100 ps)	Medium latency (less than or equal to 64 ns based on PCIe 4.0 Specification Requirement)
Does not participate in link training but is transparent to negotiations between Root Complex (CPU) and Endpoint (EP) (Protocol agnostic)	Fully participates in link training with Root Complex (CPU) and Endpoint (EP) (Protocol aware)
No 100-MHz reference clock is required	100-MHz reference clock is required
Helps with insertion loss	Helps with insertion loss, jitter, crosstalk, reflections and lane-to-lane skew
CTLE is the typical equalization circuit used	CTLE, DFE and transmitter FIR are typical equalization circuits used
Total solution cost is ~X	Total solution cost is ~(1.3X - 1.5X)

(1) For additional comparison details, refer to the technical article Signal Conditioning functions go mainstream in PCI Express Gen 4.

4 Conclusion

PCIe is an attractive interface for addressing critical high-bandwidth and ultra-low latency computing demands by next-generation distributed automotive architectures. In the near-future, PCIe automotive interconnects have the potential to exist as both *intra*-ECU and *inter*-ECU interfaces. PCIe signal redrivers, retimers, and analog switches will help enable automotive processors to realize their full TOPS computing, efficiency, and connectivity potential.

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