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TEXAS INSTRUMENTS

Application Report
SNLA333–September 2019

AR8031 to DP83867 and DP83869 System Rollover

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ABSTRACT

This application report outlines the necessary and potential steps for replacing the Qualcomm Atheros AR8031 10/100/1000 Mb/s Ethernet PHY with either TI's DP83867CR/CS/E/IR/IS or DP83869HM.

Contents

1 Purpose

While the Qualcomm Atheros AR8031 Ethernet PHY has many similarities with the TI Ethernet PHY products, the DP83867 and DP83869 offer several features that improve performance and offer greater system customization. This system rollover document outlines how to replace the Qualcomm Atheros AR8031 PHY with either TI's DP83867CR/CS/E/IR/IS or DP83869HM by comparing differences including:

- Required external components
- Pin functions
- Feature set
- Register operation

The impact to a design is dependent on PHY configuration and features used.

2 Required Changes

This section describes the hardware or circuit modifications required to transition from using the Qualcomm Atheros AR8031 to either TI's DP83867 or DP83869.

2.1 Package

All three devices, AR8031, DP83867, and DP83869, are available in a 48-pin QFN package. Additionally, the DP83867IR has a 64-pin QFP variant that supports MII/GMII.

The differences in the physical size and pin count of the packages are shown in *Table 1*.

Table 1. Packaging Differences

	DP83867CS/CR/E/IS	DP83867IR	DP83869HM	AR8031
Package	48-QFN	48-QFN / 64-QFP	48-QFN	48-QFN
Footprint	7 mm x 7 mm	7 mm x 7 mm / 10 mm x 10 mm	7 mm x 7 mm	6 mm x 6 mm

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2.2 Pinout

All three devices have the 48-pins each, additionally the DP83867IR has a 64-pin variant. The functionality of pins on each of these devices are different. Please see Appendix A for the pin mapping between the AR8031 and the DP83867/9, as well as pins not applicable for the DP83867/9.

2.3 Bias Resistor

Internal biasing between the devices is accomplished in a similar manner. The only difference is the value of the bias resistor and the bias connector pin.

The DP83867/9 uses an 11 kΩ (±1%) resistor on pin 12 in the QFN package, or pin 15 in the QFP package.

AR8031 uses a 4.99 kΩ (±1%) resistor on pin 30. The differences in the bias resistor requirements are shown in *Table 2*.

Table 2. Bias Resistor Values

	DP83867/DP83869	AR8031
Bias Resistor Value	11 kΩ (±1%)	2.37 kΩ (±1%)
Pin Number	12(QFN) / 15(QFP)	9

2.4 Strapping Configuration

The DP83867 and the DP83869 strap options allows configuring the PHY address, functional mode selection (speed and interface), and Auto-Negotiation and Mirror Mode enable. In addition, the DP83867 strap options also allows configuring RGMII clock skew and SGMII enable. The DP83867 uses a 4-level strap option, while the DP83869 uses 2-level for functional configurations and 4-level for PHY address strapping. Do not connect the strap pins directly to VDDIO or GND, since strap pins may have alternate functions after reset is deasserted.

For specific strap options, please refer to the *Strap Configuration* section of the *DP83867IR/CR* data sheet, *DP83867E/IS/CS* data sheet, or *DP83869HM* data sheet .

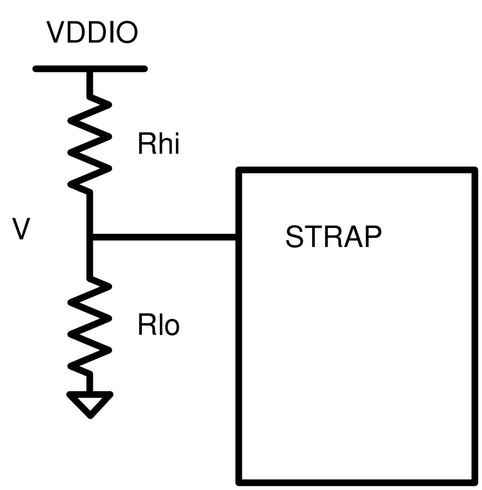

Figure 1. DP83867 and DP83869 Strapping Configuration

Unlike the DP83867/9, the AR8031 does not have any dedicated GPIO pins. However, the device uses multi-function pins to help configure the device at power on. The AR8031 strapping options are 2-level, and allow configuring the PHY address, Mode Definition (speed and interface), and LED polarity. Refer to the *Power-on Strapping Pins* section of the AR8031 datasheet for more information on strapping options.

2.5 MDIO Pull-Up Resistor

The AR8031, DP83867, and DP83869 each require a pull-up resistor on their respective MDIO pins for the SMI/MIIM interface. TI recommends using a 2.2-kΩ resistor to pull up pin 17 on the DP83867 QFN package, pin 21 on the DP83867 QFP package, and pin 41 on the AR8031. The AR8031 requires a 1.5-kΩ pull up resistor on pin 48.

2.6 Signal Detect

The AR8031 and DP83869 have Signal Detect functionality, while the DP83867 does not.

On the DP83869, the JTAG_TDI/SD pin 24 can be connected to the optical transceiver. Pin 24 must be configured to SD by strapping LED_1 (pin 46) high at power up.

The AR8031 has a dedicated Signal Detect — pin 41. When the pin is pulled high, the signal is valid; when pulled low, the signal is lost.

2.7 LEDs

2.7.1 LED Modes

The DP83867 and DP83869 have similar configurable LED modes. The AR8031 LEDs have dedicated functions.

The DP83867 and the DP83869 LED operation mode is configured by programming the register at address 0x0018. This is register is called the LEDCR1 on the DP83867, and LEDS_CFG1 on the DP83869. The LEDs can be configured to reflect transmit and receive activity and errors, collision detect, and link status.

The AR8031 LED pins: LED_ACT, LED_LINK10_100, and LED_LINK1000 represent 10/100/1000 BASE-T activity, 1000 BASE-T link, and 10/100 BASE-T link respectively.

2.7.2 LED Circuits

The DP83867 and DP83869 LED circuits must be reconfigured from the AR8031 depending on the PHY configuration.

For the DP83867 and the DP83869, the LED output pins are also used as straps, so the external components required for strapping and LED usage must be considered in order to avoid contention. If the input is resistively pulled high, then the corresponding output must be an active low driver. Otherwise, the output must be an active high driver. LED circuits must be configured accordingly. It is recommended to operate the LED from higher supply, as operating from a 1.8-V supply results in dim LEDs. Example configurations are provided in the *LED Configuration* sections of the *DP83867IR/CR* data sheet, *DP83867E/IS/CS* data sheet, and *DP83869HM* data sheet.

On the AR8031, LED_ACT and LED_LINK1000 pins are also used as straps. These pins may require external resistors to configure the device as needed. Refer to the AR8031 datasheet for more information.

2.8 Power Configurations

Both the DP83867 and DP83869 can be operated in two or three supply mode with the option of a separate VDDIO supply (for digital and analog isolation). Refer to the *Power Supply Recommendations* sections of the *DP83867IR/CR* data sheet, *DP83867E/IS/CS* data sheet, and *DP83869HM* data sheet for configuration diagrams, and notes on timing in case all power supplies cannot be powered together.

The AR8031 can be powered from one external supply, however, the internal regulators requires other external components and traces. Refer to the AR8031 datasheet for more information.

The DP83867 and DP83869 does not require these additional components.

Table 3 describes the differences in power supply configurations between the devices.

Table 3. Power Configurations

	DP83867 / DP83869	DP83867 / DP83869 Considerations	AR8031	AR8031 Considerations
One-supply mode	—	—	Yes	3.3-V supply is required. 1.1 V and 2.5 V is supplied by an internal regulator, with external traces connecting the regulator outputs to the supply pins. LX (pin 3) requires a 4.7-uH / 500-mA power inductor. The analog power supply rails AVDDL and AVDD33 require a ferrite bead each.
Two-supply mode	Yes	1.1-V and 2.5-V supplies required.1.8 V is supplied internally by regulator.	—	1.1-V and 3.3-V supplies required. 2.5 V is supplied as described above.
Three-supply mode	Yes	1.1-V, 1.8-V and 2.5-V supplies required.	—	—

3 Potential Changes

The following section describes the specific changes that may be needed in converting to a DP83867 or DP83869 design. The default values for the DP83867 or the DP83869 may be enough for transition between parts.

3.1 Power Up Timing

Each of the devices (the DP83867, DP83869, and AR8031) require RESET_N set high for normal operation.

The DP83867 does not require any external circuitry for the correct power-up timing, whereas the DP83869 and AR8031 do require some external circuitry.

The AR8031 requires the input clock, including the crystal and external input clock, to be stable for at least 1 ms before RESETn can be deasserted. Because of this required delay from power up, an external circuit is recommended. When using the crystal, the internal clock is generated after power is stable. The AR8031 data sheet recommends keeping the reset low for 10 ms after power on to ensure the clock is stable, and the 1 ms requirement mentioned previously is satisfied.

The DP83869 needs external control over RESET_N pin during power up. If the RESET_N pin is connected to host controller, then the PHY must be held in reset for a minimum of 200 ms after the last supply powers up. If the host controller cannot be connected to RESET_N, then a 100-Ω resistor and 47-uF capacitor are required to be connected in series between RESET_N pin and ground, as shown in Figure 2.

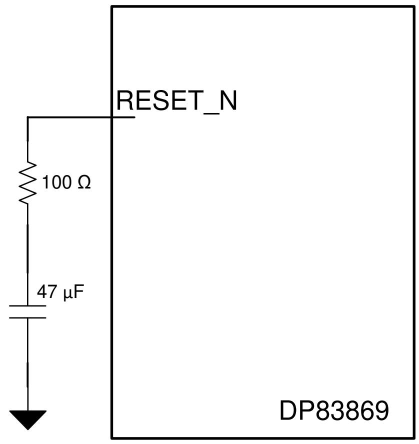

Figure 2. RESET_N Circuit

3.2 RGMII Internal Delay

The DP83867 and DP83869 provide a configurable clock skew amount in addition to a clock skew enable setting, while the AR8031 only provides a way to enable or disable clock skew.

The DP83867 and DP83869 must be configured to “Shift” mode by setting RGMII Control Register (0x0032). In Shift mode, the clock skew can be introduced in 0.25-ns increments (via register configuration). In addition, the DP83867 also allows for both transmit and receive RGMII internal skew to be configured via strapping options for eight configurations.

The AR8031 does not provide a configurable clock skew, instead register configuration can be used to turn the transmit and receive clock skew on or off. See the AR8031 data sheet for more details.

3.3 Integrated Termination Resistors

The DP83867 and DP83869 offer programmable termination impedance for the MAC interface, and integrated MDI termination resistors. These features allow the removal of external series termination resistors. See register 0x0170 in the *DP83867IR/CR* data sheet, *DP83867E/IS/CS* data sheet, or the *DP83869HM* data sheet for the termination impedance setting.

3.4 PHY Address

The DP83867 and DP83869 default to PHY address 0x0, while the AR8031 defaults to PHY address 0x1. However, all three can be strapped to another PHY address by adding pullup or pulldown resistors to the appropriate pin, or pins, and register configuration.

Refer to the *Strap Configuration* section of the *DP83867IR/CR* data sheet, *DP83867E/IS/CS* data sheet, or the *DP83869HM* data sheet for details.

3.5 Physical Layer ID Register

The PHY Identifier Registers #1 (0x02) and #2 (0x03) together form a unique identifier for the DP83869. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor model number, and the model revision number.*Table 4* details the differences in the PHY Identifier Registers.

The OUI (Organizationally Unique Identifier) for Texas Instruments is 0x080028.

The vendor model number is represented by bits 9 to 4 in PHYIDR2, and the revision number is represented by bits 3 to 0 in PHYIDR2.

Table 4. PHYID Comparison

Register Address	Register Bits	Description	DP83867	DP83869	AR8031
0x02	15:0	Bits 3 to 18 of the OUI	0010 0000 0000 0000	0010 0000 0000 0000	0000 0000 0100 1101
0x03	15:10	Bits 19 to 24 of the OUI	1010 00	1010 00	1101 00
0x03	9:4	Vendor Model Number	10 0011	00 1111	00 0111
0x03	3:0	Revision Number	0001	0001	0100

3.6 MDIO Register Writes

The DP83867, DP83869, and AR8031 all have both standard and extended SMI/MIIM (MDIO) registers.

The DP83867 and DP83869 can access the extended registers through the indirect method (using standard registers 0x000D and 0x000E as outlined in IEEE 802.3).

4 Informational Changes

This section describes features offered in DP83867 and DP83869, and how to transition to implementing them. These functions may or may not be offered in the Qualcomm Atheros AR8031 device. *Table 5* lists the changes described later in this section.

Table 5. Feature Set Comparison

Features	DP83867CR/CS/E/IS	DP83867IR	DP83869HM	AR8031
RGMII	Yes	Yes	Yes	Yes
GMII	No	Yes	No	No
SGMII	Yes[1]	No	Yes	Yes
Interrupt	Yes	Yes	Yes	Yes
WoL	Yes	Yes	Yes	Yes
Time Domain Reflectometry (TDR)	Yes	Yes	Yes	Yes
JTAG	Yes	Yes	Yes	No
IEEE 1588 SFD	Yes	Yes	Yes	Yes
IEEE 802.3 Test Modes	Yes	Yes	Yes	Yes
Loopback Modes	Yes	Yes	Yes	Yes
BIST / PRBS	Yes	Yes	Yes	No

(1) DP83867CR does not support SGMII.

4.1 Power Down / Interrupt

The DP83867 and DP83869 offer a separate, multifunction pin to allow the system to power down the device, or to indicate an interrupt. In default configurations, the pin is set as power down. The AR8031 has a dedicated INT pin; however, register configuration must be used to put the device in the power-down state.

The AR8031 requires an external 10-kΩ pull-up resistor on the INT pin.

In the DP83867 and DP83869, the PWR_DOWN/INT pin may be asserted low to put the device in a power down state. The interrupt allows a MAC to act upon the status in the PHY without polling the PHY registers. The interrupt source can be selected through the interrupt registers, MICR (0x0012) and the interrupt status can be read from ISR (0x0013). When operating this pin as an interrupt, an external 2.2 kΩ connected to the VDDIO supply is recommended. Additionally, on the DP83869, the fiber interrupt can be selected with FIBER_INT_EN (0x0C18), and interrupt status can be read with FIBER_INT_STTS (0x0C19).

4.2 Wake on LAN (WoL)

The DP83867, DP83869, and AR8031 offer Wake-on-LAN function. This function provides a mechanism for bringing the Ethernet PHY out of a low-power state using a special Ethernet packet, called a Magic Packet.

The AR8031 has two hardware pins that can be used for triggering the WoL interrupt. Both of these pins (5, 40) require an external 10 kΩ pull-up resistor. The INT pin (pin 5) can be configured to output an active low signal, or the WOL_INT pin can output a pulse width of 32 clock cycles at the reception of the WoL packet.

The DP83867 and DP83869 can be configured to generate an interrupt to wake up the MAC when a qualifying packet is received. An option is also available to generate a signal or pulse through any of the GPIO pins to inform a connected controller that a wake event has occurred. If using the interrupt pin, it is recommended that the PWR_DOWN/INT pin is pulled up to the VDDIO supply using an external 2.2-kΩ resistor. Register 0x134 can be used to configure the WoL receive configuration, including the pulse width length.

For customized packet configuration and secure-on password configuration, see the *Wake-on-Lan Packet Detection* section of the *DP83867IR/CR* data sheet, *DP83867E/IS/CS* data sheet, or *DP83869HM* data sheet.

4.3 Time Domain Reflectometry (TDR)

The DP83867, DP83869, and AR8031 each support Time Domain Reflectometry (TDR) cable diagnostics.

In the AR8031, the TDR cable diagnostic is part of a cable diagnostics test. Certain registers must be written and read from to set up and see the results of the test. The procedure is outlined in the AR8031 data sheet.

On the DP83867 and DP83869, TDR control and status can be managed using specific MDIO registers. Software resets before and after TDR tests are recommended. TDR measurements are allowed on these devices when the link partner is disconnected, the link partner is quiet (for example, in power down mode), or can also be set up to be activated automatically. TDR can be automatically activated when the link fails, or is dropped by setting bit 7 of register 0x0009 (CFG1). The results of the TDR run after the link fails are saved in the TDR registers.

In addition, the DP83867 also supports Active Link Cable Diagnostics (ALCD) for cable diagnostics with an active link partner.

Refer to the *TDR* section of the *DP83867IR/CR* data sheet, *DP83867E/IS/CS* data sheet, or *DP83869HM* data sheet for more information.

4.4 Linux Driver

TI supplies a DP83867 Linux Driver, available at http://www.ti.com/tool/dp83867sw-linux.

The Linux Driver is also available in the Linux mainline kernel.

The DP83869 Linux driver is available soon. Please contact TI for more information.

4.5 SGMII

SGMII is supported by the DP83867CS/E/IS and the DP83869HM. The Serial Gigabit Media Independent Interface (SGMII) provides a means of conveying network data and port speed between a 100/1000 PHY and a MAC with significantly less signal pins (four or six pins) than required for GMII (24 pins) or RGMII (12 pins). The DP83869HM only supports a 4-pin SGMII interface. The SGMII interface uses 1.25 Gbps LVDS differential signaling, which has the added benefit of reducing EMI emissions relative to GMII or RGMII. The following pins are used in SGMII mode:

- SGMII_SIP
- SGMII_SIN
- SGMII_SOP
- SGMII_SON

- SGMII_COP(6-pin mode)
- SGMII_CON(6-pin mode)

4.6 GMII

GMII is supported in the DP83867IR 64-QFP package. The Gigabit Media Independent Interface (GMII) is the IEEE-defined interface for use between an Ethernet PHY and an Ethernet MAC. GMII is available on the PAP devices only. The purpose of GMII is to make various physical media transparent to the MAC layer. The GMII Interface accepts either GMII or MII data, as well as control and status signals, and routes them either to the 1000BASE-T, 100BASE-TX, or 10BASE-Te modules, respectively. The following pins are used in GMII mode:

- TX_EN
- TX_ER
- GTX_CLK
- TX_D[7:0]
- RX_DV
- RX_ER
- RX_CLK
- RX_D[7:0]
- CRS
- COL

4.7 RGMII

RGMII is supported in DP83867IR/CR/CS/E/IS (48-pin QFN and 64-pin QFP) and DP83869HM. The Reduced Gigabit Media Independent Interface (RGMII) is designed to reduce the number of pins required to interconnect the MAC and PHY (12 pins for RGMII relative to 24 pins for GMII). To accomplish this goal, the data paths, and all associated control signals, are reduced and are multiplexed. Both rising and trailing edges of the clock are used. The following pins are used in RGMII mode:

- TX_CTRL
- TX_CLK
- TX_D[3:0]
- RX_CTRL
- RX_CLK
- RX_D[3:0]

Pinout Mapping

Table 6. Pinout Mapping

	DP83867CS/CR/E/IS	DP83867IR	DP83869HM	AR8031	Description
MAC Interface					
TX_D[3:0] in RGMII mode TX_D[7:0] in GMII/MII mode	25,26,27,28	31,32,33,34,35,36,37,38	25,26,27,28	36,37,38,39	Transmit Data
RX_D[3:0] in RGMII mode RX_D[7:0] in GMII/MII mode	33,34,35,36	44,45,46,47,48,49,50,51	33,34,35,36	27,28,30,31	Receive Data
RX_CLK	32	43	32	33	RGMII Receive Clock
GTX_CLK	29	40	29	35	RGMII Transmit Clock.
SGMII_SIP/N	27,28	—	16,17	46,45	Differential SGMII Data Input
SGMII_SOP/N	35,36	—	14,15	43,42	Differential SGMII Data Output
SGMII_COP/N	33,34	—	—	—	Differential SGMII Clock Output
TX_CTRL	37	52	37	—	Transmit Control
RX_CTRL	38	53	38	—	Receive Control
CRS	—	56	—	—	Carrier Sense
COL	—	55	—	—	Collision Detect
RX_ER	—	54	46	—	Receive Error
RX_DV	—	53	38	32	Receive Data Valid
TX_EN	—	52	37	34	Transmit Enable
TX_ER	—	39	21	—	Transmit Error
GPIO					
GPIO_0:1	39,40	48,49,50,51,54,55,56	22,45	—	General Purpose I/O
Management Interface					
MDC	16	20	42	1	Management data Clock
MDIO	17	21	41	48	Management Data I/O
INT/PWDN	44	60	44	5	Interrupt / Power Down (Default Power Down) *AR8031: pin 5 is only INT pin, not INT/PWDN*
WOL_INT	—	—	—	40	*AR8031: Wake-on-LAN Interrupt*
Reset					
RESET_N	43	59	43	2	Reset *AR8031: called RSTn*
Clock Interface					
XI	15	19	20	7	Crystal/Oscillator Input
XO	14	18	10	6	Crystal Output
CLK_OUT	18	22	40	25	Clock Output

Table 6. Pinout Mapping (continued)

	DP83867CS/CR/E/IS	DP83867IR	DP83869HM	AR8031	Description
PPS	—	—	—	22	*AR8031: Pulse Per Second Output*
JTAG Interface Pins					
JTAG_TRSTN	—	24	—	—	JTAG Test Reset
JTAG_CLK	20	25	21	—	JTAG Test Clock
JTAG_TDO	21	26	22	—	JTAG Test Data Output
JTAG_TMS	22	27	23	—	JTAG Test Mode Select
JTAG_TDI	23	28	24	—	JTAG Test Data Input
LED Interface					
LED_0:2	47,46,45	61,62,63	47,46,45	23,24,26	External LED Connections. *AR8031: Pins LED_ACT, LED_LINK1000, LED_LINK10_100*
Media Dependent Interface					
TD_P/M_A	1,2	2,3	1,2	11,12	Differential Transmit and Receive Signals
TD_P/M_B	4,5	5,6	4,5	14,15	Differential Transmit and Receive Signals
TD_P/M_C	7,8	10,11	7,8	17,18	Differential Transmit and Receive Signals
TD_P/M_D	10,11	13,14	10,11	20,21	Differential Transmit and Receive Signals
Other Pins					
RBIAS	12	15	12	30	Bias Resistor Connection.
SD	—	—	24	41	Signal Detect for Optical Transceiver
Power and Ground Pins					
VDDIO	19,30,41	23,41,57	18,30	—	I/O Power
VDDA1P8	13,48	17,64	13,48	—	1.8-V Analog Supply (±5%).
VDDA2P5	3,9	4,12	3,9	—	2.5-V Analog Supply (±5%).
VDD1P1	6,24,31,42	8,29,42,58	6,31,39	—	1.1-V Analog Supply (±5%).
GND	Die Attach Pad	Die Attach Pad	Die Attach Pad	Die Attach Pad	Ground
LX	—	—	—	3	*AR8031: Power Inductor Pin*
VDD33	—	—	—	4	*AR8031: 3.3-V Input for Regulator*
AVDD33	—	—	—	16	*AR8031: 3.3-V Input for PHY*
DVDDL	—	—	—	47	*AR8031: 1.1-V Digital Supply*
AVDDL	—	—	—	8,13,19,44	*AR8031: 1.1-V Analog Supply*
VDDH_REG	—	—	—	10	*AR8031: 2.5-V Regulator output*
VDDIO_REG	—	—	—	29	*AR8031: Regulator ouput* for RGMII I/O voltage