DS110DF111, DS125DF111, DS100DF410, DS110DF410, and DS125DF410 Programming Guide

1 Introduction

This document provides a reference for the DS110DF111, DS125DF111, DS100DF410, DS110DF410 and DS125DF410 Retimers (hereafter referred to as DS1xxDFxxx) from a register programming perspective. It contains detailed information related to the retimer diagnostic and debug capabilities, as well as advanced configuration options. The intended audience includes software engineers working on system diagnostics and control software.

TI recommends that the reader be familiar with one of these datasheets before reading this guide:

- DS110DF111 Low-Power, Multi-rate, 2-Chanel Retimer Datasheet (SNLS461)
- DS125DF111 Low-Power, Multi-rate, 2-Chanel Retimer Datasheet (SNLS450)
- DS100DF410 Low-Power, Multi-rate, 4-Chanel Retimer Datasheet (SNLS399)
- DS110DF410 Low-Power, Multi-rate, 4-Chanel Retimer Datasheet (SNLS397)
- DS125DF410 Low-Power, Multi-rate, 4-Chanel Retimer Datasheet (SNLS398)

These and all other collateral data related to the DS1xxDFxxx Retimers are available to download from the TI website. Alternatively, contact your local Texas Instruments field sales representative.

Table 1 highlights the key features on these devices.

Table 1. Dual and Quad Channel Retimers

	DS110DF111	DS125DF111	DS100DF410	DS110DF410	DS125DF410
Channel	2	2	4	4	4
VCO Range (Gbps)	8.5 to 11.3	9.8 to 12.5	10.3125	8.5 to 11.3	9.8 to 12.5
Package	4 mm x 4 mm QFN	4 mm x 4 mm QFN	7 mm x 7 mm QFN	7 mm x 7 mm QFN	7 mm x 7 mm QFN
EQ Boost	34 dB @ 5.65 GHZ	33 dB @ 6.25 GHZ	34 dB @ 5 GHZ	34 dB @ 5 GHZ	34 dB @ 5 GHZ
De-Emphasis	12 dB	12 dB	12 dB	12 dB	15 dB
Latency	300 ps	300 ps	300 ps	300 ps	300 ps
Power Consumption	220 mW/Channel	220 mW/Channel	220 mW/Channel	220 mW/Channel	220 mW/Channel

2 Access Methods

Two methods are provided for accessing the 10G retimers. The methods are:

- Register control via the Serial Management Bus (SMBus™)
- Automatic configuration via an external EEPROM

In a typical system, SMBus access is used to configure the device and monitor its status. If an EEPROM is used to configure the device initially, then the SMBus is subsequently used to monitor the status and adjust the configuration. Rarely is the EEPROM method used without the SMBus also being used to monitor the device status.

2.1 Register Programming via SMBus

2.1.1 Register Programming via SMBus

The DS1xxDFxxx internal registers can be accessed through standard SMBus protocol. The SMBus slave address is determined at power up based on the configuration of the ADDR pins. The pin state is read on power up, after the internal power-on reset signal is de-asserted, at which point the SMBus slave address is fixed until the next time the device is power cycled.

The ADDR pins are two-level LVCMOS IOs. Together the ADDR pins provide for 16 unique SMBus addresses for the DF410 part numbers, and for four unique addresses for the DF111 part numbers:

Table 2. SMBus Address Map

8-BIT SMBus SLAVE WRITE ADDRESS [HEX]	REQUIRED ADDRESS PIN STRAP VALUE				
	ADDR_3(DF410s)	ADDR_2(DF410s)	ADDR_1	ADDR_0	APPLICABLE TO
0x30	0	0	0	0	DS111s and DF410s
0x32	0	0	0	1	DS111s and DF410s
0x34	0	0	1	0	DS111s and DF410s
0x36	0	0	1	1	DS111s and DF410s
0x38	0	1	0	0	DF410s
0x3A	0	1	0	1	DF410s
0x3C	0	1	1	0	DF410s
0x3E	0	1	1	1	DF410s
0x40	1	0	0	0	DF410s
0x42	1	0	0	1	DF410s
0x44	1	0	1	0	DF410s
0x46	1	0	1	1	DF410s
0x48	1	1	0	0	DF410s
0x4A	1	1	0	1	DF410s
0x4C	1	1	1	0	DF410s
0x4E	1	1	1	1	DF410s

2.1.2 Read-Modify-Write Operations

In the following sections, some programming examples are provided which modify only a portion of an 8-bit register. Smaller sections of an 8-bit register are called fields. Each register can contain multiple fields that affect different circuits and features. The best way to modify a specific field without altering the other bits in a register is to use a read-modify-write operation. This approach consists of the following:

1. Read the target register.
2. Modify the register value by changing only the specific fields of interest. This involves the use of a write mask.
3. Write the modified value to the target register.

The logical expression for determining the final write value used in step 3 based on the original register value, the write value, and the write mask is as follows:

W_{FV} = Final write value (1)

R_{OV} = Original read value (2)

W_V = Desired write value (3)

W_M = Write mask (4)

$W_{FV} = [R_{OV} \mid (W_V \& W_M)] \& [(W_V \& W_M) \mid \sim W_M]$ (5)

The write mask provided in the example below and throughout this document identifies which bits in a register are intended to be affected. If a bit position has a mask value of 0, then that bit should not be affected during the read-modify-write operation. The following is an example of a read-modify-write operation to write 4'b1100 to Reg_0x2F[7:4]:

Table 3. Example Read-Modify-Write Operation

STEP	OPERATION	ADDRESS [HEX]	WRITE VALUE [HEX]	WRITE MASK [HEX]	FINAL WRITE VALUE [HEX]	READ-BACK VALUE [HEX]	COMMENT
1	Read	2F	-	-	-	06	Reg_0x2F has power-on default value of 0x06
2	Modify	2F	C0	F0	-	-	The write mask modifies bits 7, 6, 5, and 4 only.
3	Write	2F	-	-	C6	C6	

2.2 Device Configuration via External EEPROM

The DS1xxDFxxx can automatically read its initial configuration from an EEPROM at power up. The EN_SMB pin is used to configure the DS1xxDFxxx for SMBus Slave or SMBus Master mode. When this pin is pulled to VDD though a 1 kΩ resistor, the DS1xxDFxxx acts as an SMBus slave. When this pin is floating (unconnected), the DS1xxDFxxx acts as an SMBus Master and reads from an external EEPROM upon the assertion of the READ_EN_N pin low. Once the EEPROM read is complete, the DS1xxDFxxx reverts to being an SMBus Slave, and it asserts the ALL_DONE_N output low to indicate the completion of the EEPROM read. The EN_SMB pin should not be dynamically changed between the high and float states.

Multiple TI high-speed signal conditioning devices can be programmed with a single EEPROM, and the use of an EEPROM eliminates the need for an external microprocessor or software driver to program desired register settings upon each system power-up. An external SMBus Master is still recommended for the purposes of reading status information from TI devices.

Programming EEPROM for the DS1xxDFxxx requires an understanding of the relationship between EEPROM register bits and Slave Mode register bits. While an EEPROM allows devices to start up with settings different than the factory default, the EEPROM only maps a subset of the SMBus register bits. SMBus register bits in the device that are not stored in EEPROM cannot be changed from default at device startup. In order to program EEPROM successfully for the DS1xxDFxxx, configure the EEPROM based on the following properties.

Table 4. DS1xxDFxxx EEPROM Programming Properties

EEPROM PROGRAMMING FUNCTION	DESCRIPTION
EEPROM File Format	EEPROM hex file format is recommended for programming EEPROM for TI high-speed signal conditioning devices.
CRC (Cyclic Redundancy Check)	If enabled, each programmed device slot has a CRC value calculated from all the Bytes used by the device to load from EEPROM.
Address Map Headers	If enabled, a 2 or 3 Byte Address Map Header is included in the hex file to indicate the start address of the EEPROM data of each device.
EEPROM > 256 Bytes Enable Bit	This bit must be enabled for the device to load properly from an EEPROM memory location greater than Address 0xFF.
Common Channel Configuration	If enabled, the settings for all channels in each device die is programmed with one common Channel Register settings.
EEPROM Burst Size	The programmed value indicates the maximum number of Bytes to read during a burst read operation. A value of 0x10 is recommended.

For more in-depth information, including examples of how to program EEPROM for the DS1xxDFxxx devices, refer to the *Understanding EEPROM Programming for 10-G to 12.5-G Retimers Application Report*.

2.3 Register Types

The DS1xxDFxxx has two types of registers:

- Shared Registers – These registers are used for device-level configuration and device-level status observation.
- Channel Registers – These registers are used for channel-specific configuration and channel-specific status observation. All channels have the same channel register set and can be configured independent of each other.

Reg_0xFF is used to select between the shared register set and the channel register set.

Table 5. Register Page Select Register

GLOBAL REGISTER	BIT	DESCRIPTION
0xFF	7:4	Reserved
	3	Selects All Channels for Register Write
	2	Enable Register Write to One or all Channels, and Register Read from One channel 1: Channel Register 0: Shared registers
	1:0	Select Target Channel for Register Reads and Writes: 00: Channel 0 on DF410s, Channel A on DF111s 01: Channel 1 on DF410s, Channel B on DF111s 10: Channel 2 on DF410s 11: Channel 3 on DF410s

The contents of the channel select register, register 0xff, cannot be read back over the SMBus. Read operations on this register always yield an invalid result. All eight bits of this register should always be set to the desired values whenever this register is written. Always write 0x0 to the four MSBs of register 0xff. The register set target selected by each valid value written to the channel select register is shown in Table 6.

Table 6. Channel Selection Register Values Mapped to Register Set Target

REGISTER 0xFF VALUE	SHARED/CHANNEL REGISTER SELECTION	BOARDCAST CHANNEL REGISTER SELECTION	TARGET CHANNEL SELECTION	COMMENTS
0x00	Shared	N/A	N/A	All reads and writes target shared register set.
0x04	Channel	NO	0 (A for DF111s)	All reads and writes target channel 0 register set.
0x05	Channel	NO	1 (B for DF111s)	All reads and writes target channel 1 register set.
0x06	Channel	NO	2	All reads and writes target channel 2 register set.
0x07	Channel	NO	3	All reads and writes target channel 3 register set.
0x0C	Channel	YES	0	All writes target all channel register sets, all reads target channel 0 register set.
0x0D	Channel	YES	1	All writes target all channel register sets, all reads target channel 1 register set.
0x0E	Channel	YES	2	All writes target all channel register sets, all reads target channel 2 register set.
0x0F	Channel	YES	3	All writes target all channel register sets, all reads target channel 3 register set.

2.4 Common Device Configurations

The DS1xxDFxx is easily configurable for multiple applications through a simple sequence of register commands. The following sections provide guidance for programming the DS1xxDFxxx for some common applications.

2.4.1 Front-Port Ingress (Module-to-Host)

The following sequence configures the DS1xxDFxx with settings that are common in a 10.3125 Gbps Front-Port Ingress direction:

- 10.3125 Gbps data rate
- Adapt mode 0 (that is CTLE fixed, DFE Powered Down)
- Transmit VOD = ~800 mVppd (Default)
- De-Emphasis = 0 dB

NOTE: At the Ingress direction, PCB trace Length is fixed, so Adapt mode 0 is recommended. A sweep of values Transmit VOD and De-Emphasis setting is recommended for determining the optimal settings for the specific application.

Once this sequence has been programmed, to reset the receiver and re-acquire lock at any time, simply run a CDR reset and reset-release sequence.

Table 7. 10.3125-Gbps Front-Port Ingress Configuration Sequence

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENTS
1	Global	Write	FF	0C	0C	Select channel registers and enable broadcast mode to write to all channels.
2	Channel	Write	00	04	04	Reset channel registers, self-clearing.
3	Channel	Write	0A	0C	0C	Assert CDR reset.
4	Channel	Write	2F	C0	F0	Select 10.3125Gbps standard rate mode for DS125DF410. Check the 0x2F register setting for other devices for 10.3125 Gbps.
5	Channel	Write	31	00	60	Set Adapt Mode 0.
6	Channel	Write	03	00	FF	EQ=0x00, Select the right value depending on the channel loss.
7	Channel	Write	3A	00	FF	Same as Reg_0x03
8	Channel	Write	40	00	FF	Same as Reg_0x03
9	Channel	Write	1E	08	08	Power down DFE
10	Channel	Write	2D	08	08	Enable overriding the EQ setting from 0x03 register setting(Need to set for DF111s).
11	Channel	Write	2D	02	07	Configure VOD, 800 mV.
12	Channel	Write	15	00	47	Configure the DEM, 0 db.
13	Channel	Write	0A	00	0C	Release CDR reset.

2.4.2 Front-Port Egress (Host-to-Module)

The following sequence configures the DS1xxDFxx with settings that are common in a 10.3125 Gbps Front-Port Egress direction.

- 10.3125 Gbps data rate
- Adapt mode 1 (that is CTLE adaptive, DFE Powered Down)
- Transmit VOD = ~600 mVppd(Default)
- De-Emphasis = 0 dB

NOTE: At the Egress direction, keep the loss of PCB trace from Retimer transmitter to Optical Module input to be less than < 5 dB, so that there is enough margin to pass the SFF8431 Point B compliance test.

Table 8. 10.3125-Gbps Front-Port Egress Configuration Sequence

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENTS
1	Global	Write	FF	0C	0C	Select channel registers and enable broadcast mode to write to all channels.
2	Channel	Write	00	04	04	Reset channel registers, self-clearing.
3	Channel	Write	0A	0C	0C	Assert CDR reset.
4	Channel	Write	2F	C0	F0	Select 10.31. Select 10.3125 Gbps standard rate mode for DS125DF410. Check the 0x2F register setting for other devices for 10.3125 Gbps.

Table 8. 10.3125-Gbps Front-Port Egress Configuration Sequence (continued)

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENTS
5	Channel	Write	31	20	20	Set Adapt Mode 1.
6	Channel	Write	3A	00	FF	Set fixed EQ setting value for divide by 4 and divide by 8 rates.
7	Channel	Write	1E	08	08	Power down DFE.
8	Channel	Write	2D	00	07	Configure VOD, 600 mV.
9	Channel	Write	15	00	47	Configure the DEM, 0 db.
10	Channel	Write	0A	00	0C	Release CDR reset.

2.4.3 Backplane and Cable

The following sequence configures the DS1xxDFxx with settings that are common in a 10.3125 Gbps backplane and Cable Applications.

- 10.3125 Gbps data rate
- Adapt mode 2 (that is CTLE adaptive, DFE Adaptive)
- Transmit VOD = ~600 mVppd
- De-Emphasis = 0 dB

NOTE: A sweep of values Transmit VOD and De-Emphasis setting is recommended for determining the optimal settings.

Table 9. 10.3125-Gbps Backplane and Cable Configuration Sequence

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Global	Write	FF	0C	0C	Select channel registers and enable broadcast mode to write to all channels.
2	Channel	Write	00	04	04	Reset channel registers, self-clearing.
3	Channel	Write	0A	0C	0C	Assert CDR reset.
4	Channel	Write	2F	C0	F0	Select 10.31. Select 10.3125 Gbps standard rate mode for DS125DF410. Check the 0x2F register setting for other devices for 10.3125 Gbps.
5	Channel	Write	31	20	20	Set Adapt Mode 1.
6	Channel	Write	3A	00	FF	Set fixed EQ setting value for divide by 4 and divide by 8 rates.
7	Channel	Write	1E	00	08	Power UP DFE.
8	Channel	Write	2D	00	07	Configure VOD, 600 mV. Tune the VOD setting as needed.
9	Channel	Write	15	00	47	Configure the DEM, 0db, Tune the DEM setting as needed.
10	Channel	Write	0A	00	0C	Release CDR reset.

3 Channel Register Commands

3.1 Reset Channel Registers

Reset all channel registers to power-on default values.

Table 10. Reset Channel Registers

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	00	04	04	Assert channel register reset. This bit is self-clearing.

3.2 Assert CDR Reset

Assert CDR reset.

Table 11. Assert CDR Reset

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	0A	0C	0C	Assert CDR reset.

3.3 Release CDR Reset

Release CDR reset.

Table 12. Release CDR Reset

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	0A	0C	0C	Release CDR reset.

3.4 Check for Signal Detect Status (DF111s Only)

Check the signal detect status of a channel to determine if there is a signal present at the input. This information can be a valuable debug tool, since it indicates whether a signal is present or not at the input of the device.

Table 13. Check Signal Detect Status

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Read	54			Reg_0x54[7] = sd_status
2	To determine Signal Detect status: signal_detected = Reg_0x54[7]					

3.5 Check for CDR Lock Status

Check the CDR status of a channel to determine if the CDR is in lock.

Table 14. Check CDR Lock Status

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Read	2			Reg_0x2[4:3] = cdr_lock_status
2	To determine CDR lock status: CDR_lock = Reg_0x2[4:3]=2b'11'					

3.6 Interrupts

Table 15 describes the signal detect and lock related Interrupt registers.

Table 15. Interrupt Registers

REGISTERS	DEFINITION	DESCRIPTIONS
Channel Register 0x01[0]	Signal Detect Loss Interrupt	Means this was one loss of signal event (Read Clear)
Channel Register 0x01[4]	CDR Lock Loss Interrupt	Means this was one loss of lock event (Read Clear)
Channel Register 0x054[0]	Signal Detect Interrupt	Signal Detect Interrupt (Read Clear), DF111s only
Channel Register 0x054[1]	CDR Lock Interrupt	CDR Lock Interrupt (Read Clear), DF111s only

3.7 Enable Interrupt (DF111 only)

Table 16 describes the Interrupt Enable related registers.

Table 16. Enable Interrupt

REGISTERS	DEFINITION	DESCRIPTIONS
Channel Register 0x56	Bit[3] =CDR lock interrupt enable	Enable CDR clock interrupt for bit1 of reg0x54
	Bit[2]=Signal Detect Interrupt enable	Enable Signal Detect interrupt for bit0 of reg0x54
	Bit[1] =CDR loss of lock interrupt enable	Enable the CDR loss of lock interrupt for bit4 of reg0x1
	Bit[0]=Loss of Signal interrupt enable	Enable the Loss of signal Interrupt bit0 of reg0x1

3.8 Frequency PPM Counter (DF111 only)

These two registers are used for VCO frequency readback.

Table 17. Frequency PPM Counter

REGISTERS	DEFINITION	DESCRIPTIONS
Channel Register 0x3B	Frequency PPM counter(MSB)	The VCO value can be determined with the following register reading a calculation. Channel Register 0x3B = Channel Register 0x3C of VCO msb = Channel Register of VCO lsb VCO Frequency (GHz) = [(decimal (Reg 3B) x 256 + decimal (Reg 3C)) x 32] / 40960 Example register reading and calculation Reg 0x3B = 33'h (decimal value = 51) Reg 0x3C = 8E'h (decimal value = 142) VCO (GHz) = [(51x256 + 142) x 32] / 40960 VCO (GHz) = 10.3109 Reg 0x3B = 31'h (decimal value = 49) Reg 0x3C = 8E'h (decimal value = 254) VCO (GHz) = [(49x256 + 254) x 32] / 40960 VCO (GHz) = 9.998
Channel Register 0x3C	Frequency PPM counter(LSB)	

3.9 Standard Data Rate Settings

The DS1xxDFxxx channels must each be preprogrammed for the expected data rates to ensure CDR lock. You can program the rate/sub-rate to one of a set of pre-defined standard values to quickly configure the DS1xxDFxxx. The rate/sub-rate settings are programmed by writing to channel Reg_0x2F[7:4]. Check the datasheet for the definition of each device. Table 18 shows an example for the DS125DF410.

Table 18. DS125DF410 Standard Rate Modes Configurable from Reg_0x2F

STANDARD RATE SETTING	REG_0x2F VALUE [HEX]	REG_0x2F WRITE MASK [HEX]
2.5 Gbps, 5 Gbps ,10 Gbps	26	F0
2.4576 Gbps, 4.9152 Gbps, 9.8304 Gbps	36	
3.072 Gbps, 6.144 Gbps	46	
6.25 Gbps	A6	
3.125 Gbps, 6.25 Gbps	B6	
10.3125 Gbps	C6	
1.25 Gbps, 10.3125 Gbps	F6	

3.10 Manual Data Rate Configuration

Alternatively, you can manually program a channel to receive a specific data rate. If an application requires a data rate that exists within the VCO range or the divide-by-2 or divide-by-4 VCO or divide-by-8 VCO ranges, but is not listed in the rate sub rate table, then those data rate parameters must be manually programmed into the device. This procedure involves writing the PPM count registers 0x60, 0x61, 0x62, 0x63 based on the desired data rate and the frequency of the calibration clock (CAL_CLK_IN). The DS1xxDF1xx support a 25-MHz calibration clock.

3.10.1 25-MHz Calibration Clock

The procedure for calculating the register 0x60, 0x61, 0x62, 0x63 values when the calibration clock is 25 MHz is as follows:

REG_0x60_val = Floor{(DataRate ×1024) / (32 × 25E6)} & 0x00FF (6)

REG_0x61_val = Floor{(DataRate × 1024) / (32 × 25E6)} & 0xFF00 >> 8 | 0x80 (7)

REG_0x62_val = Reg_0x60_val (8)

REG_0x63_val = Reg_0x61_val (9)

For reference, Table 19 shows the register values for manually programming a few standard data rates. See more descriptions from the datasheet as well.

Table 19. Register Settings for Common Data Rates using 25-MHz Calibration Clock

DATA RATE	REG_0x60 VALUE [HEX]	REG_0x61 VALUE [HEX]	REG_0x62 VALUE [HEX]	REG_0x63 VALUE [HEX]	REG_0x2F[7:4] Divider Ratio Setting VALUE(DS125DF410 as example) [HEX]
10.3125 Gbps(1)	90	B3	90	B3	C (Divider by 1)
9.8304 Gbps(1)	26	B1	26	B1	C (Divider by 1)
10 Gbps(1)	00	B2	00	B2	C (Divider by 1)
12.5 Gbps	80	BE	80	BE	C (Divider by 1)
5 Gbps(1)	00	B2	00	B2	A (Divider by 2)
2.5 Gbps(1)	00	B2	00	B2	A (Divider by 4)

(1) These rates can also be configured by selecting the appropriate rate setting in Reg_0x2F.

Table 20. Set Data Rate(DS125DF410 as example)

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENTS
1	Channel	Write	60	REG_0x60_val from above	FF	
2	Channel	Write	61	REG_0x61_val from above	FF	
3	Channel	Write	62	REG_0x62_val from above	FF	
4	Channel	Write	63	REG_0x63_val from above	FF	
5	Channel	Write	64	FF	FF	Set PPM tolerance to max.
6	Channel	Write	2F(1)	C0	F0	divide-by-1(DS125DF410 Definition: Group 0 and Group 1)
				A0	F0	divide-by-2(DS125DF410 Definition: Group 0 and Group 1)
				B0	F0	divide-by-4(DS125DF410 Definition: Group 0 and Group 1)
				F0	F0	divide-by-4(DS125DF410 Definition)
8	Channel	Write	0A	0C	0C	Assert CDR reset (6.3).
9	Channel	Write	0A	00	0C	Release CDR reset (6.4).

(1) Check the datasheet of each device for the Divider Ratio Setting versus Register 0x2F setting.

3.11 Read Horizontal and Vertical Eye Opening

Read the horizontal eye opening (HEO) and vertical eye opening (VEO).

Table 21. Read HEO and VEO

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Read	27			Read HEO register.
2	To convert HEO to UI: HEO_UI = Reg_0x27 / 64					
3	Channel	Read	28			Read VEO register.
4	To convert VEO to mV: VEO_mV = Reg_0x28 * 3.125					

3.12 Mute/Un-Mute Driver Output

When the driver output is muted, the differential peak-to-peak output voltage is approximately 0 mVppd.

Table 22. Register Writes to Mute the Driver Output

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	09	20	20	Enable output mux override.
2	Channel	Write	1E	E0	E0	Set pre-lock mux to mute the driver output (this is also the default setting).

3.13 Invert Output Data Polarity

Invert the polarity of the output data.

Table 23. Invert the Polarity of the Output Data

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	1F	80	80	Inverting the Output Polarity

3.14 Set Receiver Adapt Mode

Set the equalization adapt mode of the receiver. The Receiver CTLE and DFE equalization circuits are automatically adapted at lock time to maximize a figure of merit (FOM) which is based on the post-equalized eye opening. There are three modes of adaption which control how the CTLE and DFE are adapted.

Table 24. Receiver Equalization Adaption Modes

ADAPT MODE REG_0x31[6:5]	DESCRIPTION
0	Manual CTLE and DFE. The CTLE and DFE do not adapt, rather they are manually set by the user.
1	CTLE only. The CTLE automatically adapts at lock time to maximize the FOM. The DFE is not adapted and should be disabled. This mode is typically suitable for channels up to 30 dB of insertion loss when reflections and crosstalk are fairly well-controlled. For channels where reflections and crosstalk are a concern, adapt mode 2 may yield better performance.
2	CTLE adapted until optimal, then DFE, then CTLE again. The CTLE automatically adapts to maximize the FOM, then the DFE automatically adapts to further maximize the FOM, then the CTLE adapts a final time to further maximize the FOM. **This mode generally offers the best performance and is recommended for most high-loss channels where reflections and/or crosstalk are also a concern.** This mode places more equalization burden on the CTLE compared to the DFE.

Table 24. Receiver Equalization Adaption Modes (continued)

ADAPT MODE REG_0x31[6:5]	DESCRIPTION
3	CTLE adapted until CDR lock, then DFE, then CTLE again. The CTLE automatically adapts to achieve CDR lock, then the DFE automatically adapts to maximize the FOM, then the CTLE adapts again to further maximize the FOM. This mode places more equalization burden on the DFE compared to the CTLE. This mode should only be considered if adapt mode 2 does not produce adequate results.

Table 25. Register Writes to Set Rx Adapt Mode

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
N/A	Channel	Write	31	00	60	Set adapt_mode = 0
				20	60	Set adapt_mode = 1
				40	60	Set adapt_mode = 2
				60	60	Set adapt_mode = 3

3.15 Set CTLE Adaption Table

Select the set of CTLE settings which comprise the adaption table used during adaption modes 1, 2, and 3. Note that the default CTLE adaption table is suitable for the vast majority of channels, and this should only be changed in circumstances where a customized application-specific CTLE adaption table is desired. Table 26 shows an example for the DS125DF111. Check the datasheet for the CTLE Adaptation Table on each device.

Table 26. Program the CTLE Adaption Table

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	4F	F9	FF	Final adapt index, customize value if needed
2	Channel	Write	4E	E6	FF	Customize value if needed.
3	Channel	Write	4D	A5	FF	Customize value if needed.
4	Channel	Write	4C	99	FF	Customize value if needed.
5	Channel	Write	4B	D5	FF	Customize value if needed.
6	Channel	Write	4A	69	FF	Customize value if needed.
7	Channel	Write	49	95	FF	Customize value if needed.
8	Channel	Write	48	B0	FF	Customize value if needed.
9	Channel	Write	47	A0	FF	Customize value if needed.
10	Channel	Write	46	54	FF	Customize value if needed.
11	Channel	Write	45	90	FF	Customize value if needed.
12	Channel	Write	44	C0	FF	Customize value if needed.
13	Channel	Write	43	50	FF	Customize value if needed.
14	Channel	Write	42	80	FF	Customize value if needed.
15	Channel	Write	41	40	FF	Customize value if needed.
16	Channel	Write	40	00	FF	First adapt index, customize value if needed
17	Channel	Write	39	00	1F	Start adaption at index 0.

3.16 HEO/VEO Minimum Required Hits

Set the minimum required hits for each phase/voltage offset during the HEO/VEO measurement. Any hits below this number are treated as zero hits.

Table 27. Set HEO/VEO Minimum Required Hits

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	2B	02	0F	Set EOM min required hits to 2. Minimum value is 0 and maximum is 15.

3.17 Disable the DFE

Disable the DFE.

Table 28. Disable the DFE

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	1E	08	08	Disable DFE (DFE_PD=1)

3.18 Enable the DFE

Enable the DFE.

Table 29. Enable the DFE

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	1E	00	08	Enable DFE (DFE_PD=0)

3.19 Read DFE Tap Values

The DFE tap polarities and tap weights can be read back from channel Reg_0x71 through 0x75.

Table 30. Read DFE tap Values

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
N/A	Channel	Read	71	-	-	DFE Tap 1 If Reg_0x71[5]=1, DFE1 magnitude = -1 * Reg_0x71[4:0] If Reg_0x71[5]=0, DFE1 magnitude = +1 * Reg_0x71[4:0]
N/A	Channel	Read	72	-	-	DFE Tap 2 If Reg_0x72[4]=1, DFE2 magnitude = -1 * Reg_0x72[3:0] If Reg_0x72[4]=0, DFE2 magnitude = +1 * Reg_0x72[3:0]
N/A	Channel	Read	73	-	-	DFE Tap 3 If Reg_0x73[4]=1, DFE3 magnitude = -1 * Reg_0x73[3:0] If Reg_0x73[4]=0, DFE3 magnitude = +1 * Reg_0x73[3:0]
N/A	Channel	Read	74	-	-	DFE Tap 4 If Reg_0x74[4]=1, DFE4 magnitude = -1 * Reg_0x74[3:0] If Reg_0x74[4]=0, DFE4 magnitude = +1 * Reg_0x74[3:0]
N/A	Channel	Read	75	-	-	DFE Tap 5 If Reg_0x75[4]=1, DFE5 magnitude = -1 * Reg_0x75[3:0] If Reg_0x75[4]=0, DFE5 magnitude = +1 * Reg_0x75[3:0]

3.20 Set CTLE Boost Value

Manually set the CTLE boost value. This is only applicable in adapt mode 0, where the CTLE is not adapted. There are 255 total CTLE boost settings. A subset of these settings, spanning the full range of the CTLE, is listed in Table 31 for THE DS125DF111.

Table 31. CTLE Boost Table (Subset of 255 Available Settings)

EQ TABLE INDEX	CTLE BOOST SETTINGS REG_0X03[7:0] [HEX]	HIGH-FREQUENCY BOOST (Gain @ 6.25 GHZ) [dB]
0	00	3
1	40	8
2	80	11
3	50	13
4	C0	14
5	90	15
6	54	17
7	A0	18
8	B0	20
9	95	24
10	69	26
11	D5	27
12	99	28
13	A5	29
14	E6	31
15	F9	33

Table 32. Set CTLE Boost Value for DF111s

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	2D	08	08	Enable CTLE boost override
2	Channel	Write	03	80	FF	Set CTLE boost to 0x80. When input data rate is divided by 1 or 2 VCO setting, use 0x3A as a satiable CTLE level. Different input channel loss requires different CTLE settings.
3	Channel	Write	3A	00	FF	Set CTLE boost to 0x00. When input data rate is divided by 4 or 8 VCO setting, use 0x3A as a satiable CTLE level. Different input channel loss requires different CTLE settings.

Table 33. Set CTLE Boost Value for DF410s

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	03	80	FF	Set CTLE boost to 0x80. When input data rate is divided by 1 or 2 VCO setting, use 0x3A as a satiable CTLE level. Different input channel loss requires different CTLE settings.
2	Channel	Write	3A	00	FF	Set CTLE boost to 0x80. When input data rate is divided by 4 or 8 VCO setting, use 0x3A as a satiable CTLE level. Different input channel loss requires different CTLE settings.
3	Channel	Write	40	00	FF	Same value as Channel Register Reg_0x03

3.21 Read CTLE Value

Channel Reg_0x03 is the primary observation point for the CTLE boost value.

Table 34. Read CTLE Boost Value

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Read	3	-	-	Read CTLE boost value.

3.22 Enable PRBS Generator

Enable the PRBS generator diagnostic feature.

NOTE: The PRBS generator is a test feature and is not intended for mission mode usage. Enabling the PRBS generator increases current consumption and raises the junction temperature of the device. First configure the device to lock, and make sure that RX CDR locks before enabling the PRBS Generator, so that the PRBS generator is clocked by the recovered clock of the retimer, synchronized to the data applied to the input of the retimer.

Table 35. Register Writes to Enable PRBS Generator

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	09	20	20	Override Output Multiplexer Select.
2	Channel	Write	1E	80	E0	Turn on serializer (ser_en=1).
3	Channel	Write	1E	10	10	Power-up PRBS Generator.
4	Channel	Write	30	00	08	Reset PRBS Clock.
5	Channel	Write	30	08	08	Power-up PRBS Clock.
6	Channel	Write	30	00 02	03	Select PRBS9 pattern. Select PRBS31 pattern.
7	Channel	Write	0D	20	20	Enable PRBS Clock triggering on Div/Clock so that the eye diagram is viewable. Disabling results in Pattern Cycle triggering.

3.23 Adjust CDR Bandwidth and Charge Pump

The CDR has an adjustable bandwidth allowing you to track more or less low-frequency input jitter. When the CDR tracks low-frequency jitter, this jitter is passed through to the output, potentially with some attenuation. Any jitter which is outside the bandwidth of the CDR is not tracked and, therefore, does not pass through to the output.

Table 36 illustrates how to manually adjust the CDR bandwidth.

Table 36. Adjust CDR Bandwidth

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT	APPROXIMATE CDR –3-dB BANDWIDTH AT 10.3125 Gbps
1	Channel	Write	1C	00	FC	Force CP = 0	2.3 MHZ
				24	FC	Force CP = 1	4 MHZ
				48	FC	Force CP = 2	6.5 MHZ
				90	FC	Force CP = 3	9 MHZ
				B4	FC	Force CP = 4	12 MHZ
				D8	FC	Force CP = 5	14 MHZ
				FC	FC	Force CP = 6	15 MHZ
4	Channel	Write	0A	40	40	Enable cp_idac override	

3.24 Disable Unused Channels

Disable and power down unused channels. This is recommended for all channels which are not used in an application in order to achieve the minimum power consumption.

Table 37. Disable and Power Down Unused Channels

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	14	40	40	Force signal detect status to 0 (that is no signal detected).

3.25 Force Enabling Channel

User can force the signal detect result as High so that the channel is enabled, regardless of the input signal amplitude.

Table 38. Force Enabling Channel

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	14	80	80	Force signal detect status to 1 (that is signal detected).

3.26 Raw mode (CDR Bypassed)

When the input data rate is not supported with CDR enabled, CDR can be bypassed so that the device is under RAW mode.

Table 39. Bypass CDR

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
1	Channel	Write	0	04	04	Reset channel register to default.
2	Channel	Write	09	20	20	Enable override output mux use reg_0x1e.
3	Channel	Write	1E	00	E0	Output raw data.

Table 39. Bypass CDR (continued)

STEP	SHARED/CHANNEL REGISTER SET	OPERATION	REGISTER ADDRESS [HEX]	REGISTER VALUE [HEX]	WRITE MASK [HEX]	COMMENT
4	Channel	Write	3F	80	80	Disable fast research for refmode 3.
5	Channel	Write	31	00	60	Set adapt mode to 0.
6	Channel	Write	3A	00	FF	Set EQ boost value as 0.
7	Channel	Write	40	00	FF	Set EQ boost value as 0.
8	Channel	Write	03	00	FF	Set EQ boost value as 0.
9	Channel	Write	2D	08	08	Enable overriding the EQ setting from 0x03 register setting(Need to set for DF111s).
10	Channel	Write	A	0C	0C	CDR Reset.
11	Channel	Write	A	00	0C	Release CDR Reset.

3.27 Channel Register 0x02

Once CDR locks, by configuring Bit[7:4] of Channel Register 0x0C to '0011', Bit[5:3] of Channel Register 0x02 reflects the Divider Ratio.

Table 40. Channel Register 0x02

	Bit7:Bit4 of register 0x0C	Definition	Description
Channel Register 0x02	0000 (Default)	Bit[7] = PPM Count met	The “PPM count met” indicator bit shows if the incoming data-rate falls inside the VCO frequency +/- PPM range in Reg 0x64. If the frequency is correct for the current Rate/Subrate setting and Reg 0x60-0x64, then this bit = 1. If the frequency is not correct this bit = 0.
		Bit[6] = Auto Adapt Complete	EQ Adapt Mode (1 -2 -3) as selected in 0x31[6:5] is finished
		Bit[5] = Fail Lock Check	High if CDR unlocked
		Bit[4] = Lock	Real time lock status
		Bit[3] = CDR Lock	Real time lock status
		Bit[2] = Single Bit Limit Reached	Single Bit Threshold met (periodic updates)
		Bit[1] = Comp LPF High	High side Loop filter comparison voltage
		Bit[0] = Comp LPF Low	Low side Loop filter comparison voltage
	0011	Bit[5]=sm_divsel[2]	This is the result of divider ratio that the device is now using. 000 means divided by 1 001 means divided by 2 010 means divided by 4 011 means divided by 8
		Bit[4]=sm_divsel[1]	
		Bit[3]=sm_divsel[0]	

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265