Application Report
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DP83869 1000Base-X Link Detection

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ABSTRACT

The DP83869 supports multiple operating modes as defined in the DP83869 data sheet. This application note is only applicable while the DP83869 is operating in RGMII-to-1000Base-X mode and Gigabit Media Converter mode.

When the DP83869 is used in 1000Base-X mode or Gigabit Media Converter mode, register monitoring at start-up is necessary to confirm that the link is established. In the case that the link is not established, this application note provides details on remedial actions that can be taken to establish the link.

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1 Introduction

When an Ethernet communication system uses a discrete Ethernet PHY, the PHY is generally connected to a host controller with a MAC entity. The MAC sends and receives Ethernet data through the PHY through standard MAC interfaces (RGMII, SGMII, and so forth). The host controller uses the Serial Management Interface (MDC and MDIO signals) to check the PHY status and configuration.

Typically, after power up, reset or link loss, a host controller polls for the link up status before it attempts to initiate the data transfer over the MAC interface. The link status is stored in PHY registers for the host controller to read via the MDIO-MDC interface. In RGMII-to-1000Base-X mode or Gigabit Media Converter mode, reading additional bits is required to ensure to verify that auto negotiation and link-up successfully completed. Under certain conditions, additional intervention by the host controller may be necessary. This is described in the following sections.

2 1000Base-X Link-Up

The DP83869 1000Base-X link status is stored in the FX_STS register bit [1] (0xC01[1]). If this bit is 1, then the link is valid. If this bit is 0, then there is no link.

Along with the FX_STS register, the host controller must also check the Serdes Synchronization status bit in the SERDES_SYNC_STS register (0x4F[8]). This bit indicates if a valid signal from link partner is detected. If this bit is 1, then synchronization is established, but if the bit is 0, then synchronization is not established.

In most cases, when the Serdes Synchronization status bit is set, the PHY is able to complete auto-negotiation and achieve a successful 1000Base-X link-up (FX_STS bit[1]=1). However, in rare cases, the link is not established even when the Serdes Synchronization status bit is set to 1 (FX_STS bit[1] =0). In such cases, the host controller must write 1 to FX_CTRL register (0xC00[9]) to restart auto negotiation. Table 1 lists the possible combinations of the link status bit and Serdes Sync status bit, the interpretation for each condition, and any follow-up action that should be undertaken by the host controller.

Table 1. 1000Base-X Link-Up Table

LINK STATUS BIT	SERDES SYNC STATUS BIT	COMMENTS
0xC01[1]	0x4F[8]	
0	0	No valid signal detected from link partner
0	1	Valid signal detected and synchronization established but no link up. Restart auto negotiation through the 0xC00[9] register
1	1	Link-up successful
1	0	Not Applicable. Link will not be established if SerDes does not have synchronization.

3 Example Flowchart

Figure 1 shows an example of how a host controller can implement the logic for restarting auto negotiation.

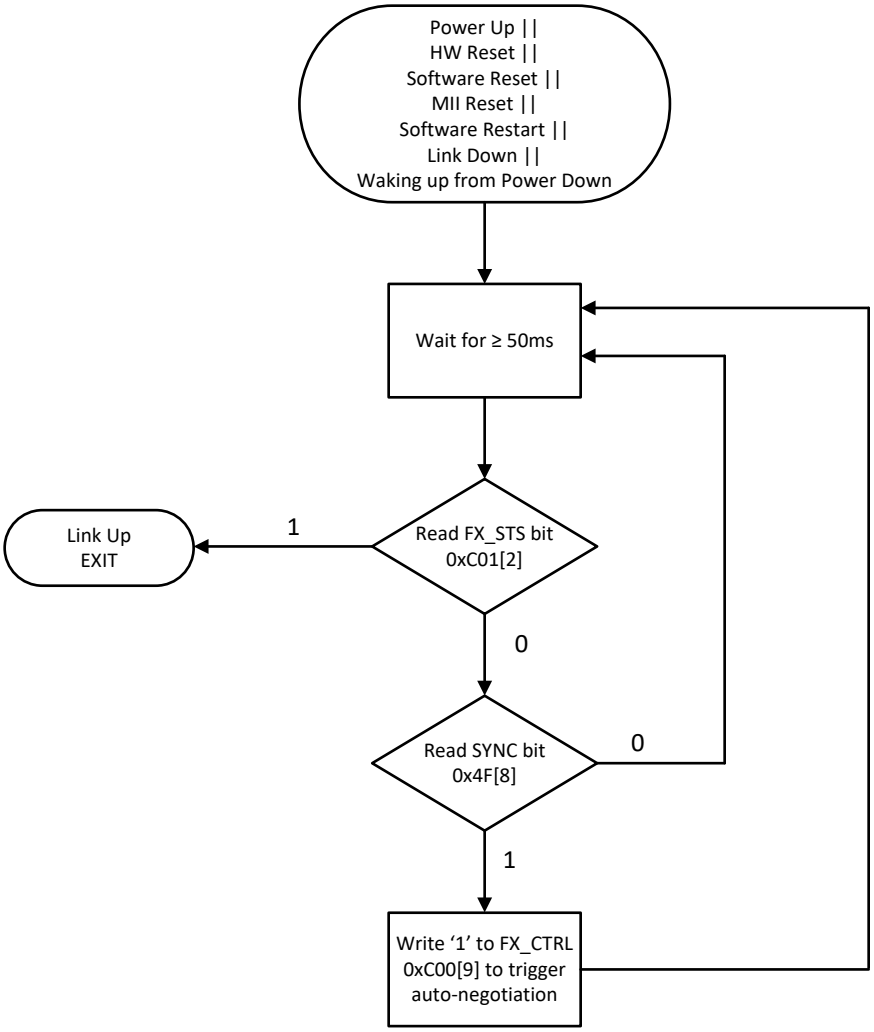

Figure 1. 1000Base-X Link-Up Flowchart

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