Application Report
SNLA301–January 2019

Margin Analysis Program (MAP) and strobe positions for DS90UB954-Q1 and DS90UB960-Q1

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ABSTRACT

TI's DS90UB954-Q1 and DS90UB960-Q1 deserializers includes multiple forms of automatic adaptations to improve link reliability. One such method is the use of automatically adjusted strobe positions, which control where data is sampled in the signal eye. Different strobe positions may be the most effective in different circumstances depending on factors such as cable length, cable quality, and temperature. The Margin Analysis Program (MAP) checks for errors and lock at combinations of the strobe positions and EQ levels to analyze the margin in the system. This document will provide an overview of strobe positions in the DS90UB954-Q1 and DS90UB960-Q1, including what strobe positions mean, how to configure strobe positions, and how to use the Margin Analysis Program (MAP) in the Analog LaunchPad™ development kit with the DS90UB954-Q1 and DS90UB960-Q1 devices.

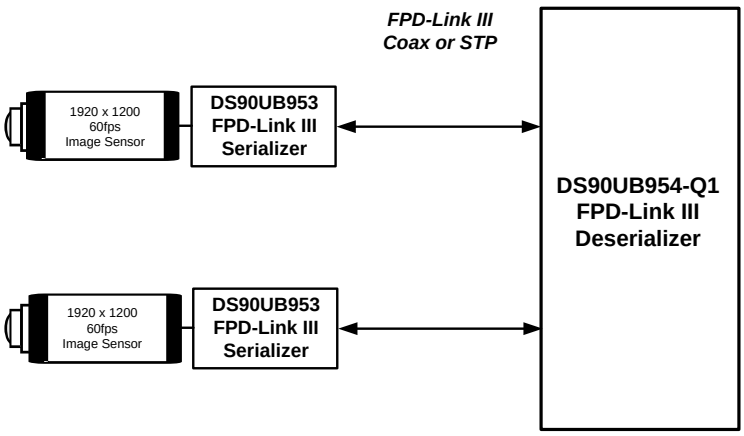

Figure 1. DS90UB954-Q1 System Diagram

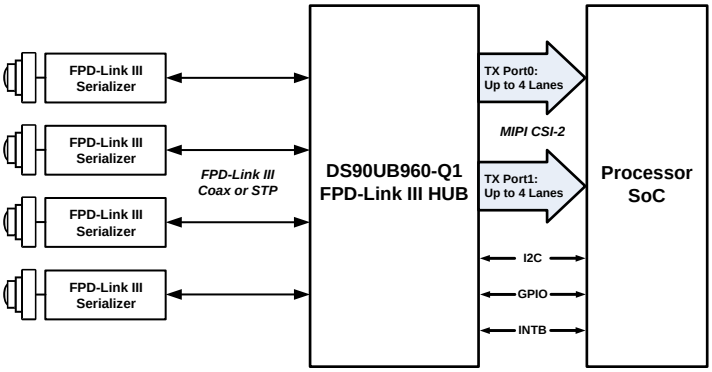

Figure 2. DS90UB960-Q1 System Diagram

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1 Introduction

Strobe positions are used in the DS90UB954-Q1 and DS90UB960-Q1 deserializers to control where in the eye data is sampled. There are fifteen possible strobe positions where seven positions use delayed sampling, seven positions use advanced sampling, and one position uses sampling at the nominal point. Usually, the strobe position is selected automatically as part of the Adaptive Equalization (AEQ) process. However, register settings can be used to control how, when, and which strobe positions are considered. Automatic adaptation may also be disabled and strobe positions may be controlled manually. Setting strobe positions manually can be used in combination with manual EQ settings to create representations of the eye that may be used for system evaluation using the Margin Analysis Program (MAP) that is built into the DS90UB954-Q1 and DS90UB960-Q1 profiles in the Analog LaunchPad development kit.

2 Strobe Position Overview and Default Operation

2.1 What Are Strobe Positions

Strobe position refers to where in the signal eye data is sampled in the clock and data recovery (CDR) block. The strobe (used to refer to the point of sampling) is either left at the nominal position, shifted to the right (“late” sampling) or to the left (“early” sampling), as shown in Figure 3. In the case of a clean eye, it is expected that early, nominal, and late sampling at the points shown in the image would result in a sampled value matching the intended value. Even in the case of the clean eye, extremely early or late sampling can cause errors by sampling in the transition region. However, compared to the noisy eye, the region in which errors may occur is much smaller. Using adaptive strobe positions allows for the appropriate position to be selected based on the actual signal eye.

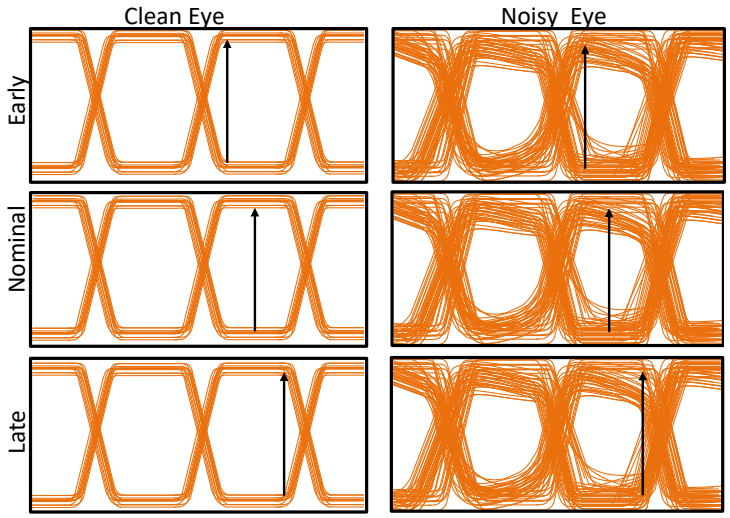

Figure 3. Early, Nominal, and Late Sampling

Early and late sampling are implemented through two methods. First, the clock can be delayed, which will move the strobe to the right and result in late sampling. The amount of clock delay is divided into eight settings from 0 to 7. Secondly, the data can be delayed while the strobe remains fixed, which effectively moves the strobe to the left and results in early sampling. The amount of data delay is divided into eight settings from 0 to 7. These clock and data delay settings are combined into a set of fifteen strobe positions as shown in Table 1.

Table 1. Strobe Positions

Sampling Type	Clock Delay	Data Delay	Strobe Position
Late	7	0	0
Late	6	0	1
Late	5	0	2
Late	4	0	3
Late	3	0	4
Late	2	0	5
Late	1	0	6
Nominal	0	0	7
Early	0	1	8
Early	0	2	9
Early	0	3	10
Early	0	4	11
Early	0	5	12
Early	0	6	13
Early	0	7	14

There are two amounts of base delay for clock and data delay: 6 buffer delay and 0 buffer delay. This 6 buffer base delay will increase the distance between Position 7 and Position 6 and the distance between Position 8, causing all strobe positions to move further away from the nominal sampling position. By default, the 6 buffer delay is used, but the 0 buffer base delay may be selected through STROBE_SET[7] and STROBE_SET[3] as shown in Table 18. The current clock delay value is recorded in Register 0xD6[2:0] (Table 16) and the data delay value is recorded in Register 0xD7[2:0] (Table 17). In a stable system, the clock and data delay should be a constant value. If the device is cycling through different clock and data delays, it indicates that the system is not stable. There are two strobe adaption modes: AEQ adaption mode, and manual adaption mode.

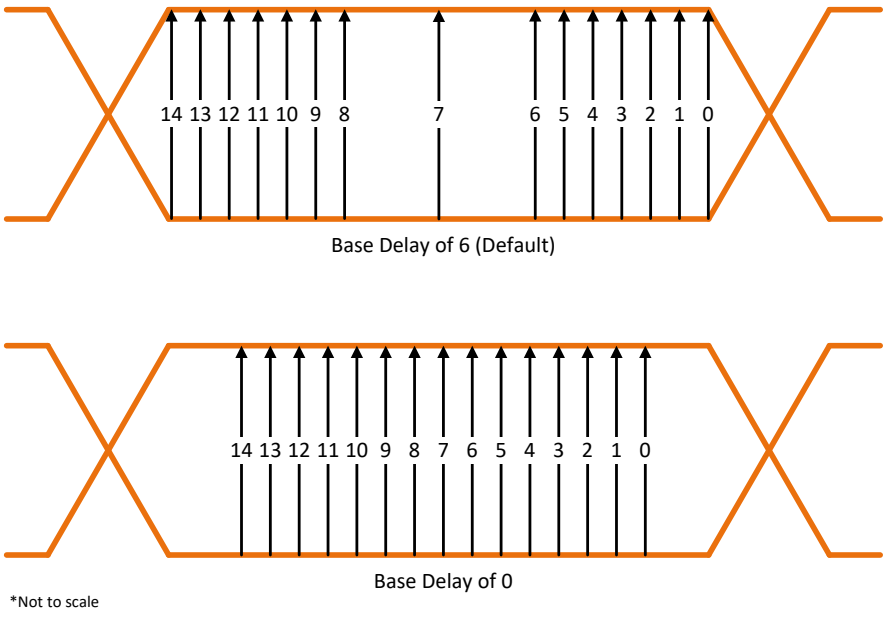

Figure 4. Base Delay Effect on Strobe Positions

As summarized in Table 2 and Figure 5, the strobe position is set through the AEQ process in the AEQ adaption mode, and the strobe position is set directly through the registers in manual mode.

Table 2. Strobe Adaption Modes

Adaption Mode	Description
AEQ Adaption Mode	Strobe position is selected as part of AEQ. This is the default mode.
Manual Adaption Mode	The strobe position is selected manually and will remain at the specified position until a new one is chosen. This mode is recommended as an evaluation and debugging mode.

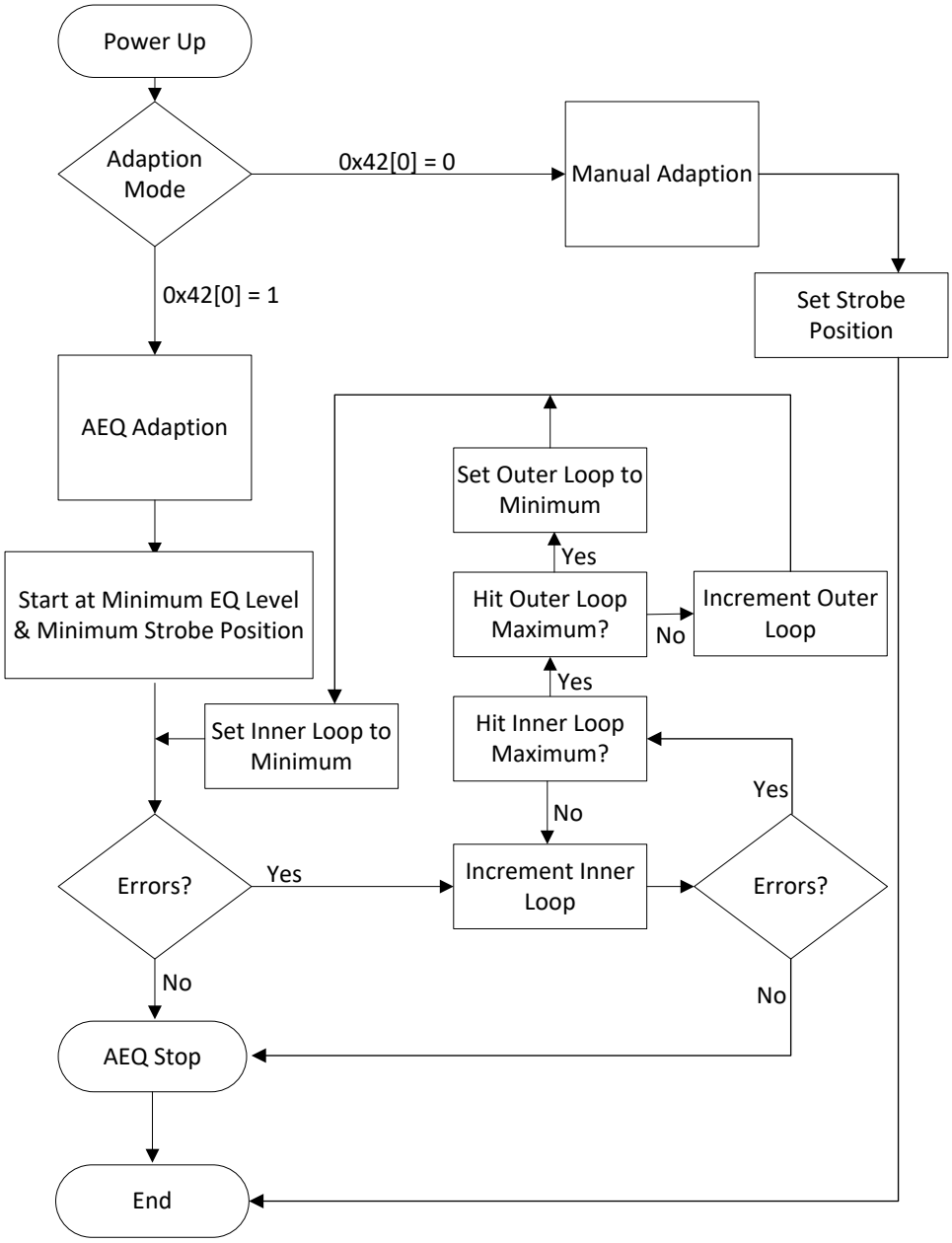

Figure 5. Adaption Mode Summary

2.2 Default Operation: AEQ Adaption Mode

Under the default settings, the strobe position is selected as part of the AEQ process. The strobe is the outer loop of the process, meaning that the device will first search through all EQ levels at the initial strobe position before incrementing the strobe position and searching through all EQ levels with the new strobe position. This process will continue until a passing state is detected. Under the default settings, the strobe position will start at the strobe position minimum and increment to the strobe position maximum. The DS90UB954-Q1 has a strobe position minimum of 7 and a maximum of 10. For the DS90UB960-Q1, the strobe position minimum is 0 and the maximum is 14. The requirements for a passing state are set by register settings and by default require lock and zero parity and encoder errors.

2.3 Configuration Options for AEQ Adaption Mode

While the AEQ process automatically selects the strobe position, the register settings control how this selection occurs. These configuration options are summarized in Table 3. The primary configuration option is to change the minimum and maximum strobe positions and EQ levels. The strobe position thresholds can be set to any value from 0 to 14, and the EQ levels can be set to any value from 0 to 15. However, EQ Level 15 is a duplicate of EQ Level 14 and TI recommends to exclude EQ Level 15. In general, TI does not recommend setting a maximum EQ level less than EQ Level 14, because cable aging may cause higher EQ levels to be more effective than they are in newer cables. After modifying the minimum or maximum positions, set AEQ_RESTART(0xD2[3]) to 1 to restart the AEQ process.

Another configuration option is to change which errors are checked by the AEQ process. By default, which is the recommended setting, packet encoding errors, parity errors, clock errors, and lock status are considered, but fewer conditions may be selected. By default, the strobe position is the outer loop, meaning that all EQ levels are checked at a given strobe position, then the strobe position is incremented, and so on until a passing state is found. The strobe position can also be set to the inner loop, meaning that the device will first try the initial EQ level with all strobe settings and then, if there is no passing state, increment the EQ level.

Additionally, as in any adaption mode, the base delay can be set to either the 6 buffer base delay (default) or to a 0 buffer base delay through STROBE_SET.

Table 3. AEQ Adaption Mode Configuration Options

Property	Description
Base Delay	0 Buffer Base Delay: • STROBE_SET[7] = 1 and STROBE_SET[0] = 1 6 Buffer Base Delay (default) • STROBE_SET[7] = 0 and STROBE_SET[0] = 0
Loop Position	Strobe Position Inner Loop: • 0x42[1] = 1: All strobe positions checked at a given EQ level, then increment EQ level and repeat until a passing state is found Strobe Position Outer Loop (default): • 0x42[0] = 0: All EQ levels checked at a given strobe position, then increment strobe position and repeat until a passing state is found
Min/Max EQ Levels	Minimum: • Set 0xD2[2] = 1 to enable using EQ minimum (enabled by default) • Set 0xD5[7:4] from 0 to 15 (default is 2) Maximum: • Set 0xD5[3:0] from 0 to 15 (default is 15, but recommended value is 14)
Min/Max Strobe Positions	Minimum: • Set 0x41[7:4] from 0 to 14 (default is 7) Maximum: • Set 0x41[3:0] from 0 to 14 (default is 10)
Errors Checked	An EQ/strobe position setting will be considered error-free only if the deserializer is locked and there are zero errors of each enabled error type: • FPD-Link III clock errors: set 0x42[6] = 1 (1 by default) • Packet encoding errors: set 0x42[5] = 1 (1 by default) • Parity errors: set 0x42[4] = 1 (1 by default)

3 Manual Strobe Control

Strobe settings may also be controlled manually. Manual control may be used to examine all strobe settings, which can be used to diagnose the condition of the eye. Manual control can also be helpful during design development and debug analysis.

3.1 How to Manually Change Strobe Settings

To change the strobe settings, write to the STROBE_SET registers shown in Table 18. The process for reading and writing indirect access registers is described in Section 5.2. Before modifying the strobe settings manually, make sure that the AEQ adaption mode is disabled by setting register 0x42[0]. The data delay setting can be set by writing to STROBE_SET[6:4], and the clock delay setting can be set by writing to STROBE_SET[2:0]. As in any adaption mode, the base delay can be set to either the 6 buffer base delay (default) or to a 0 buffer base delay through STROBE_SET[7] and STROBE_SET[3].

It is also possible to mimic manual adaption mode by leaving AEQ adaption mode enabled and setting the minimum and maximum strobe position to the same value. For example, setting register 0x41 will fix the strobe position to Position 9.

Generally, manual strobe control is used in combination with manual EQ control. EQ levels can be controlled manually by setting 0xD4[0] to 1. The EQ levels are controlled by EQ STAGE 1 SELECT VALUE (0xD4[7:5]) and EQ STAGE 2 SELECT VALUE (0xD4[3:1]). There are sixteen valid EQ levels as shown in Table 4. Minimum and maximum EQ levels can be programmed through 0xD5 (Table 15). For the minimum setting to apply, 0xD2[2] (Table 13) must be set to 1, as in the default register settings.

Table 4. EQ Levels

EQ Level	EQ2	EQ1
0	0x0	0x0
1	0x0	0x1
2	0x0	0x2
3	0x0	0x3
4	0x0	0x4
5	0x0	0x5
6	0x0	0x6
7	0x0	0x7
8	0x1	0x7
9	0x2	0x7
10	0x3	0x7
11	0x4	0x7
12	0x5	0x7
13	0x6	0x7
14	0x7	0x7
15 (1)	0x7	0x7

(1) EQ Level 15 is a duplicate of EQ Level 14. When setting the maximum EQ Level, it is recommended to set it to 0xE, excluding EQ Level 15.

4 Margin Analysis Program (MAP) Using Manual Strobe Control

Manual strobe control is a useful tool for system evaluation, as it can be used to evaluate the condition of the eye with only an I2C connection. In general, this is done by creating a representation of the eye, also called margin analysis plots, as shown in Figure 7 in which the status of the deserializer is monitored for each combination of EQ and strobe setting. These diagrams track lock status, parity errors, forward channel CRC errors, forward channel sequencing errors, and forward channel encoding errors (0x4D[5:2]

and 0x4E[5]) over all EQ settings and strobe positions using the smaller base delay. The green squares indicate passing settings, in which the deserializer and serializer are locked with zero errors. EQ levels with at least four passing strobe positions are considered recommended EQ levels. In general, TI recommends having a margin of at least three EQ levels with four passing strobe positions, including a contiguous rectangle of passing states that measures two EQ levels by four strobe positions.

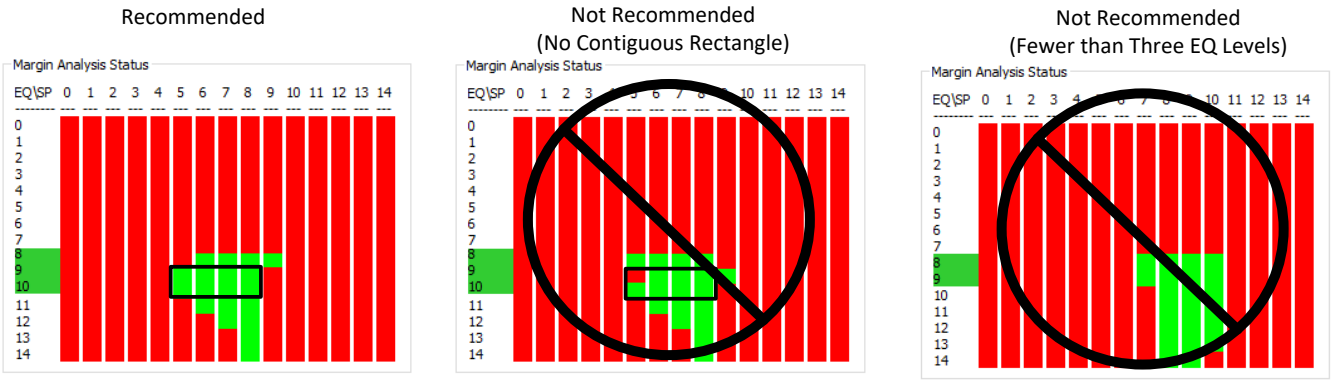

Figure 6. Margin Guidelines

Figure 7 shows the margin analysis plots for a DS90UB953-Q1 and DS90UB954-Q1 system using DACAR 302 cables with lengths of 15m, 10m, 5m, and 2m and using DACAR 462 cables with lengths of 15m, 10m, 5m, and 2m. These diagrams were created using the Margin Analysis Program built into the Analog LaunchPad development kit, as explained in the *MAP User's Guide* (SNLU243). These plots were generated using the smaller base delay and a dwell time of 1000 ms, meaning that errors and loss of lock were checked after 1000 ms after changing the EQ level or strobe position.

All of these cables show at least one EQ level with at least four strobe positions with no errors or loss of lock. All of the margin analysis plots meet TI's recommendation for sufficient margin with the exception of the 15m DACAR 462 cable. Even among the cables meeting TI recommendations, the appropriate minimum EQ level, minimum strobe position, and maximum strobe position vary for each cable. In general, TI recommends to set the minimum EQ level to the lowest EQ level with four valid strobe positions. TI also recommends to leave the maximum EQ level at 14, as higher EQ levels are more effective for cables with greater degradation, which may occur as cables age. The strobe position minimum and maximum should be set such that the majority of EQ levels have four valid strobe positions.

EXAMPLE: Based on these plots, for the 302 5m cable, the recommended EQ range is from EQ Level 0 to EQ Level 14 and the recommended strobe position range is from Position 7 to Position 11. However, for the 462 2m cable, the recommended EQ range is from EQ Level 0 to EQ Level 14 and the recommended strobe position range is from Position 7 to Position 10. These thresholds can be programmed as shown inTable 5 and Table 5. Since these thresholds were based on margin analysis plots using the 0 buffer base delay, the 0 buffer base delay should be used by setting STROBE_SET[7] = 1 and STROBE_SET[0] = 1.

Table 5. Example 302 5m Thresholds

Minimum EQ	Maximum EQ	Minimum Strobe Position	Maximum Strobe Position
Set 0xD5[3:0] = 0x0	Set 0xD5[7:4] = 0xE	Set 0x41[3:0] = 0x7	Set 0x41[7:4] = 0xB

Table 6. Example 462 2m Thresholds

Minimum EQ	Maximum EQ	Minimum Strobe Position	Maximum Strobe Position
Set 0xD5[3:0] = 0x0	Set 0xD5[7:4] = 0xE	Set 0x41[3:0] = 0x7	Set 0x41[7:4] = 0xA

In cases in which lock time is a high priority, using a limited number of strobe positions may be used to reduce lock time. In general, most passing states fall between Position 7 and Position 10. These can be used as an initial range to limit lock time. Reducing this range even further, such as from Position 8 to Position 10 may further reduce lock time under some circumstances, but will also limit the systems ability to adapt to the environment.

Comparing the two cables types, the margin is similar for DACAR 302 and DACAR 462 cables for lengths of 2m, 5m, and 10m, but the margin for the 15m DACAR 462 cable is much smaller than for the DACAR 302 15m cable, and it does not meet TI's recommended margin. Based on these measurements, TI recommends that this system use a DACAR 302 cable instead of a DACAR 462 cable for lengths greater than 10m. The insertion loss measurements for these cables is similar for the two cable types for 2m, 5m, and 10m cables (Figure 8 to Figure 11). As in the margin analysis plots, the 15m DACAR 462 cable shows noticeably worse performance compared to the 15m DACAR 302 cable, with a difference of more than 8 dB at 2 GHz.

Figure 7. Margin Analysis Plots With 0 Buffer Base Delay (1000-ms Dwell Time)

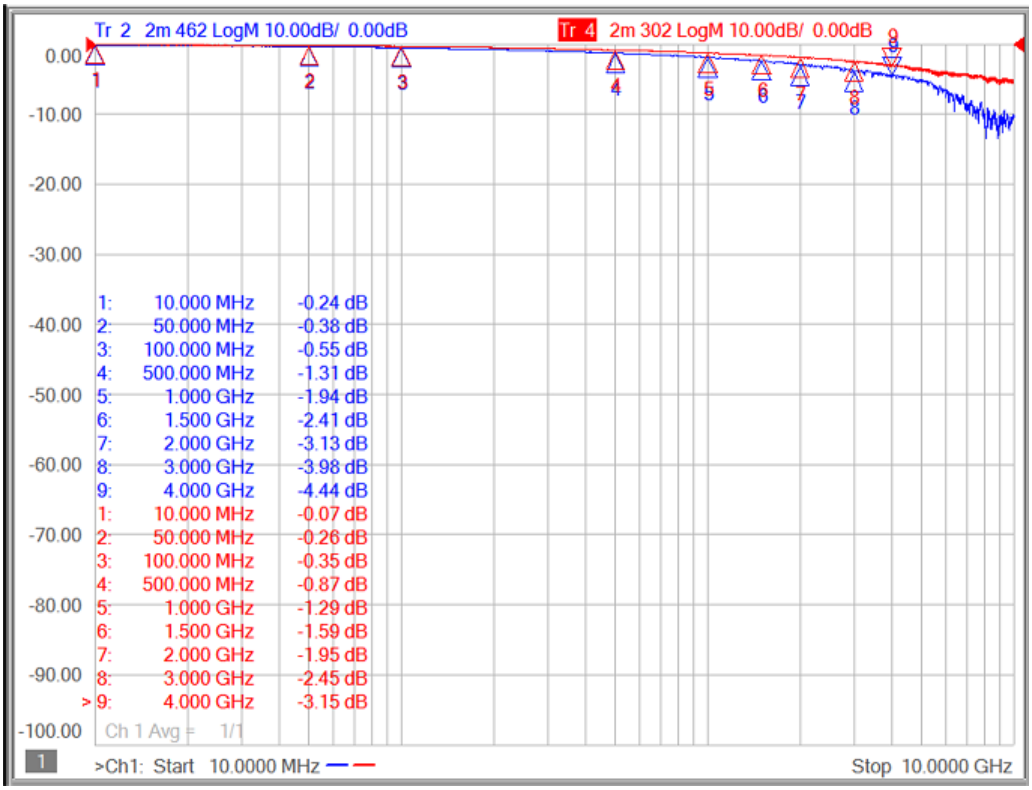

Figure 8. Insertion Loss for 2m Cables

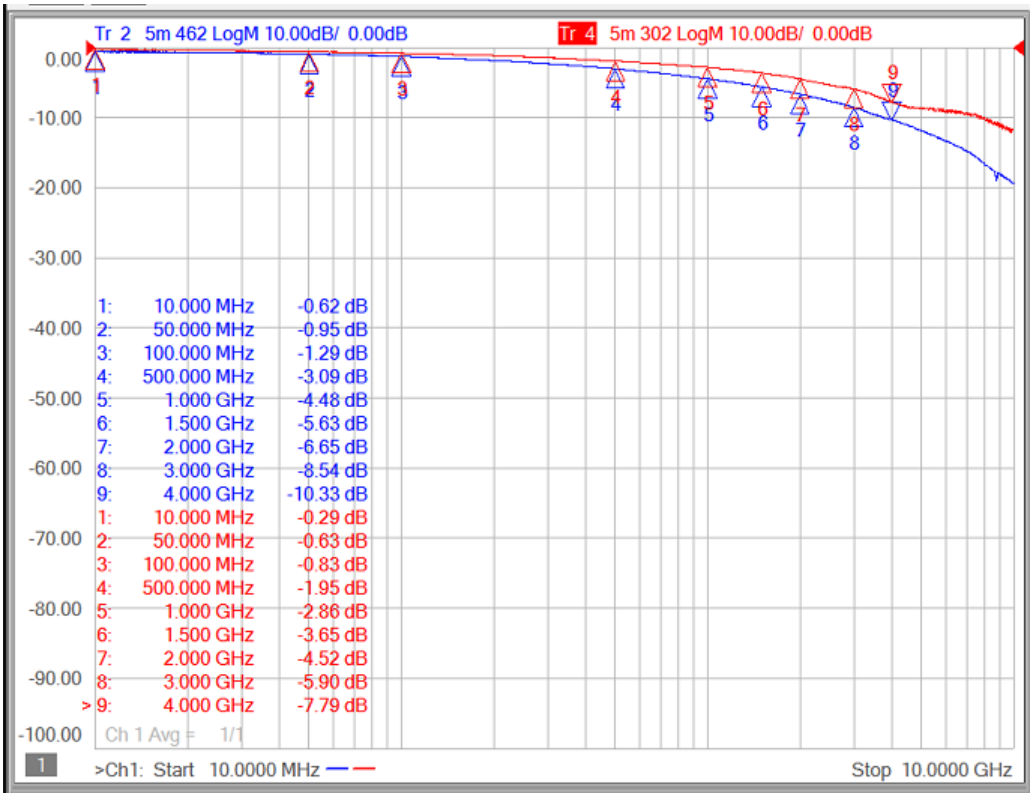

Figure 9. Insertion Loss for 5m Cables

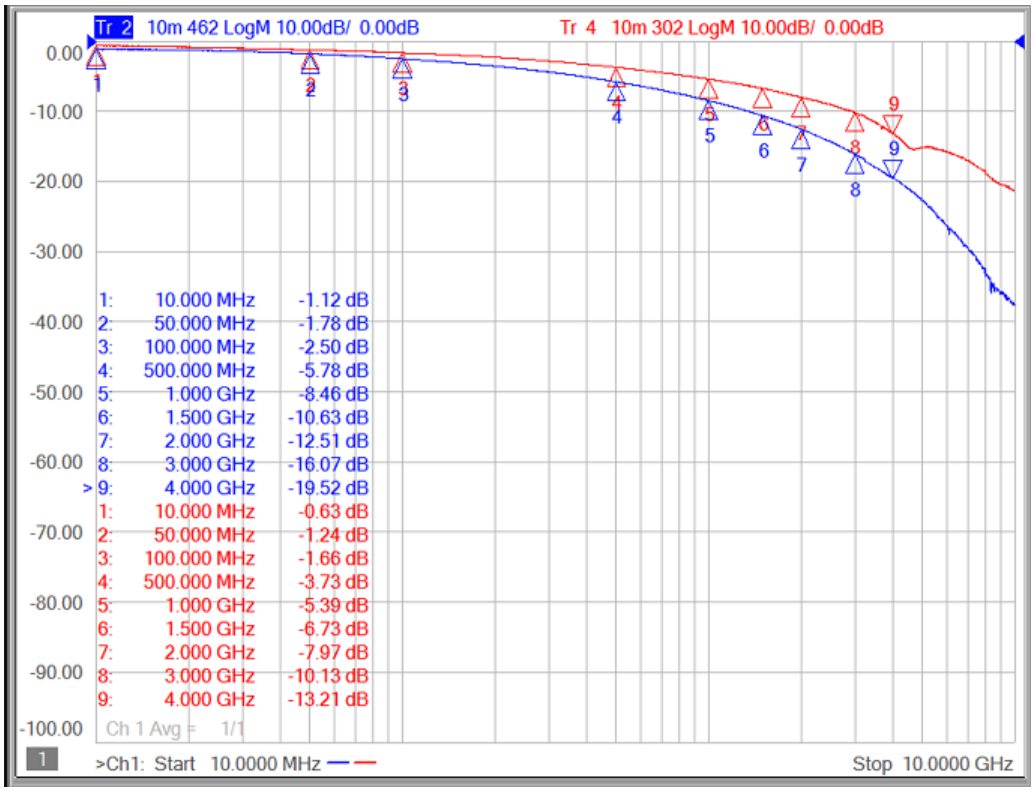

Figure 10. Insertion Loss for 10m Cables

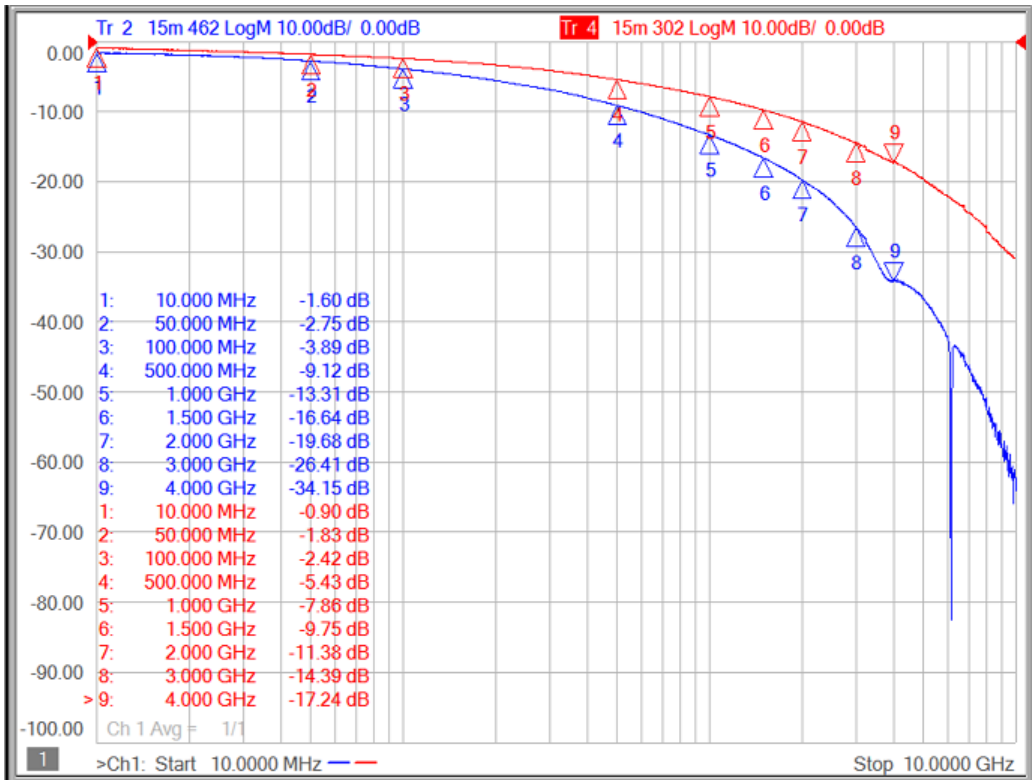

Figure 11. Insertion Loss for 15m Cables

Often, multiple cables will be used in combination. As shown in Figure 12, adding an additional cable will reduce the margin as a result of the added length and the additional interconnects. However, combining a DACAR 302 cable with a DACAR 462 cable can be used to achieve a greater margin than possible with a single DACAR 462 cable. For instance, Figure 13 shows the margin for a 15m DACAR 302 cable combined with DACAR 462 cables. Even in the case where the DACAR 302 cable is combined with two DACAR 462 cables for a total length of 19m, the margin is much greater than in the case of a single 15m DACAR 462 cable.

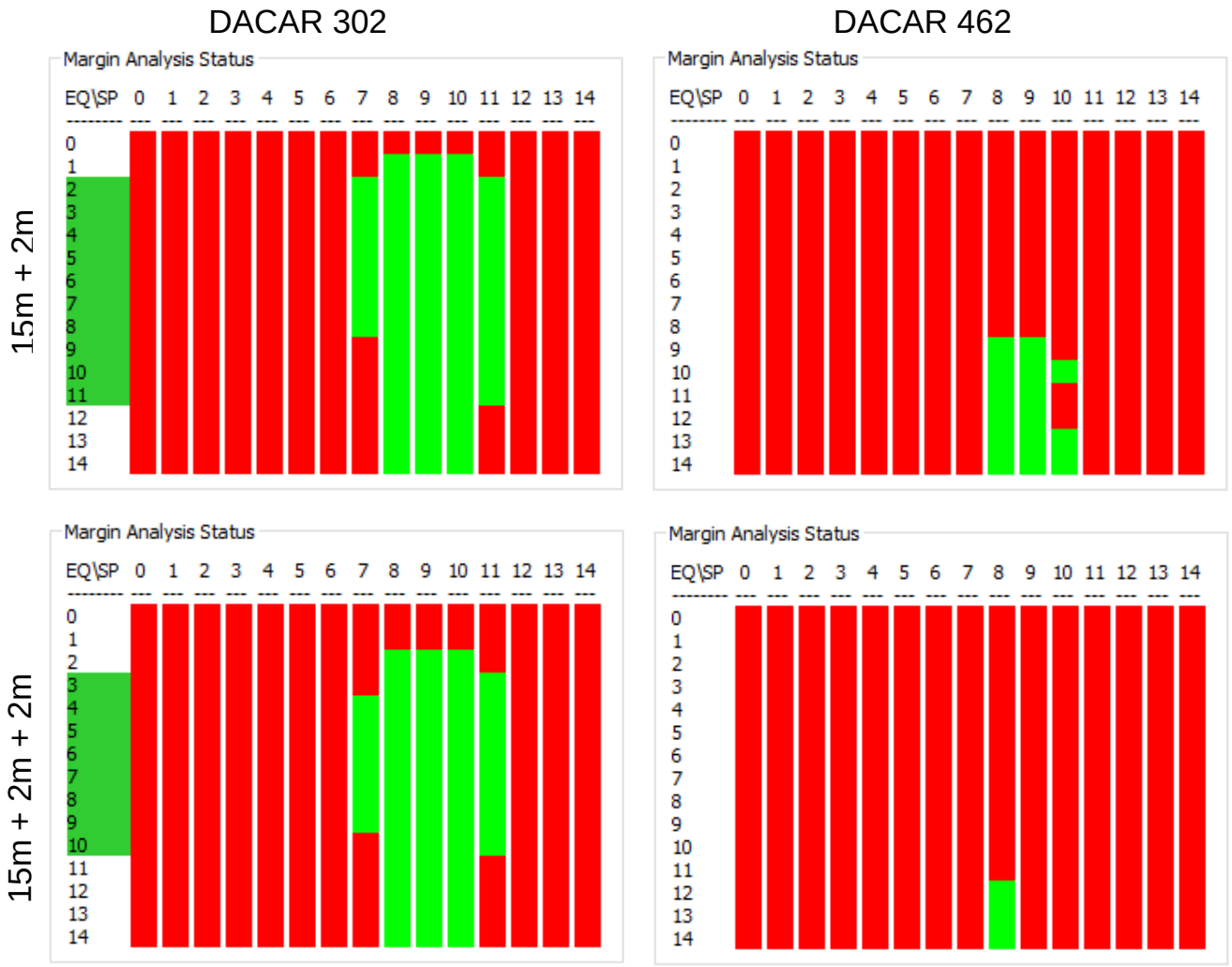

Figure 12. Margin Analysis Plots for Combined Cables With 0 Buffer Base Delay (1000-ms Dwell Time)

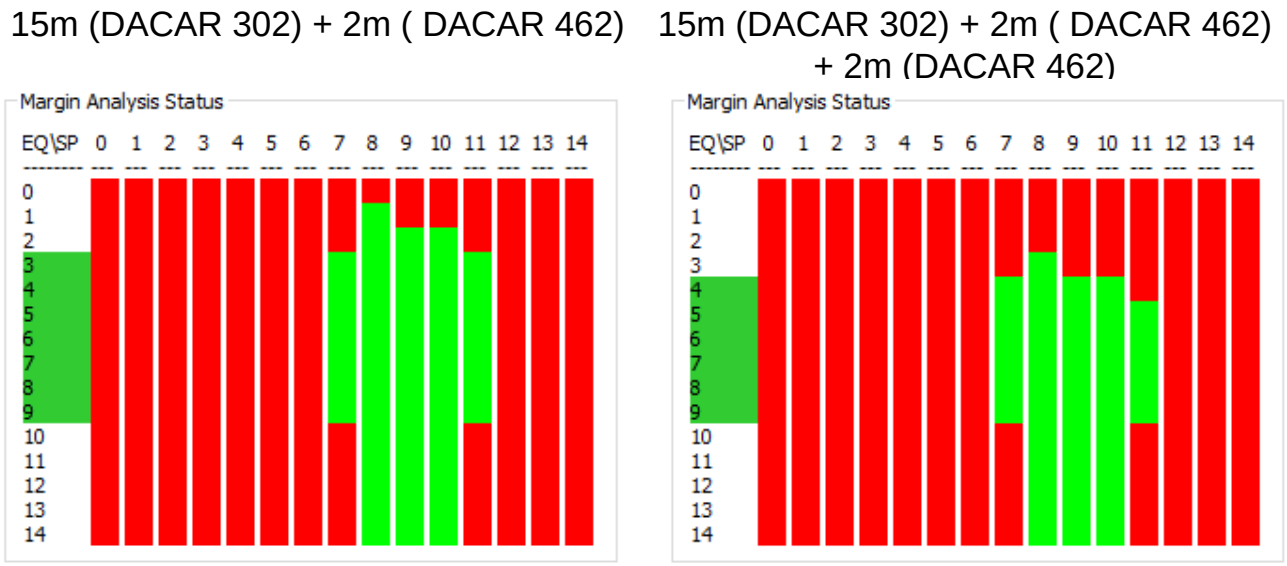

Figure 13. Margin Analysis Plots for Combined Cable Types With 0 Buffer Base Delay (1000-ms Dwell Time)

Figure 14 shows the margin analysis plots for six different DACAR 462 2m cables. The recommended EQ range and strobe position range is the same as for the original single DACAR 462 2m cable. However, if only Cable 6 is considered, Strobe Position 11 would also be included in the recommended range. Because results may vary from cable to cable, TI recommends testing multiple cables of the same length and type before setting the EQ level range and strobe position range.

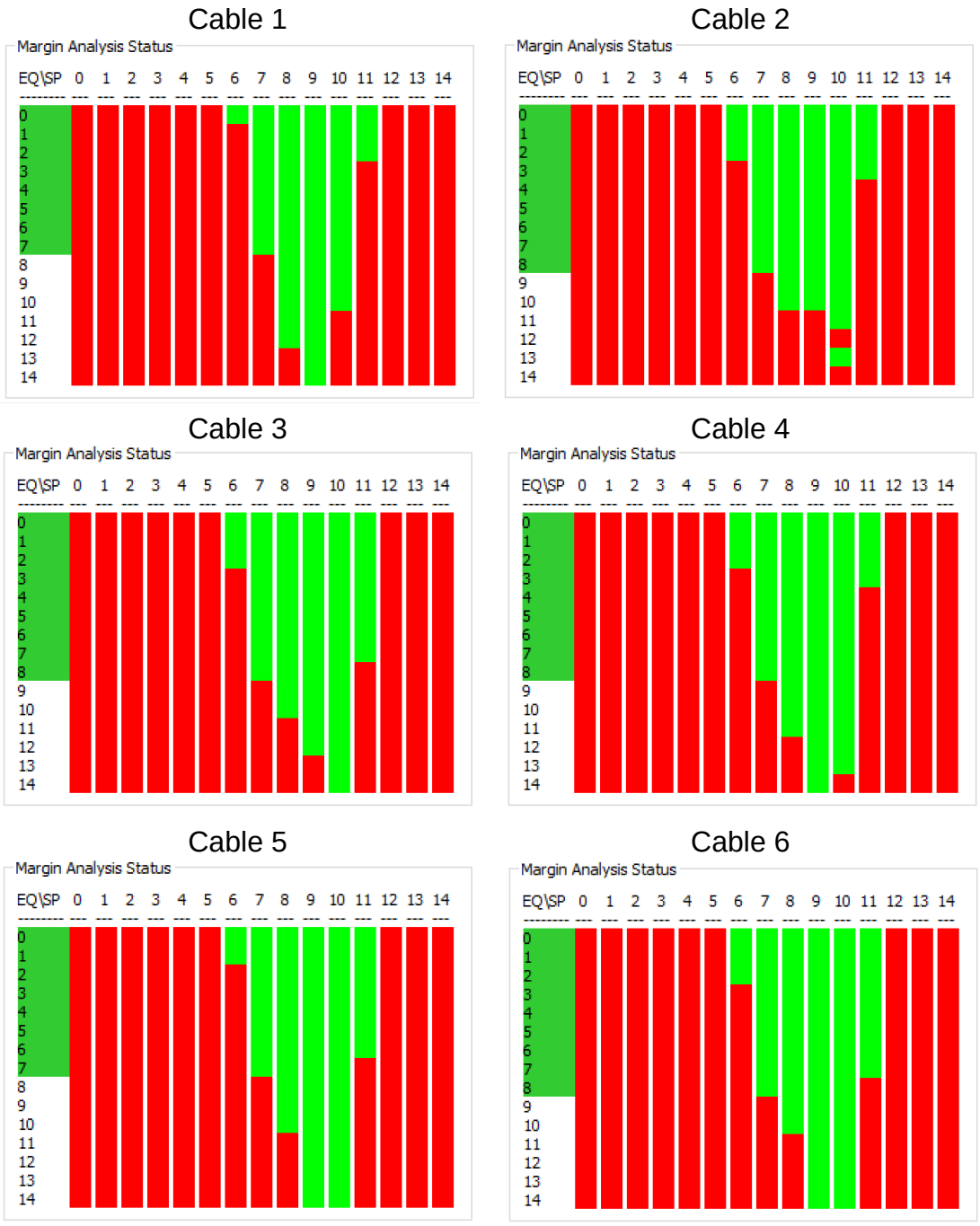

Figure 14. Margin Analysis Plots of Six Different 2m 462 Cables (Small Base Delay, 1000-ms Dwell Time)

These margin analysis plots may also be used as a debugging or design tool. For instance, Figure 15 shows the margin analysis plot for Cable 6 with a loose connection. In normal operation, the deserializer will still lock and operate properly, because there are still passing settings. However, there are far fewer passing settings than would be expected with a 2m cable. Seeing a small number of passing settings is an indicator that there is some issue within the system. This example was a loose connection, but it could also be a damaged cable, layout issues, and so forth. If a system is showing a small margin, but the cable insertion loss is good, this suggests that there may be an issue with the PCB layout. Similarly, a margin analysis plot with a large number of passing settings shows a more robust system and can be used as a simple and fast way to evaluate a system using only an I2C connection.

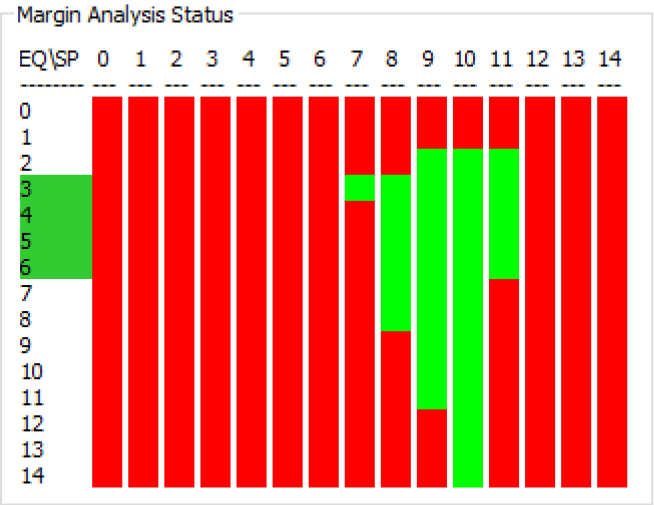

Figure 15. Cable 6 With Loose Connection

5 Strobe Position Registers

This section details the registers used to configure strobe operation and create eye diagrams. See the *DS90UB954-Q1 Datasheet* (SNLS570) or *DS90UB960-Q1 Datasheet* (SNLS589) for the full register map.

In the register definitions under the *TYPE* and *DEFAULT* heading, the following definitions apply:

- R = Read only access
- R/W = Read / Write access
- R/RC = Read only access, Read to Clear
- (R/W)/SC = Read / Write access, Self-Clearing bit
- (R/W)/S = Read / Write access, Set based on strap pin configuration at startup

5.1 Direct Access Registers

5.1.1 SFILTER_CFG Register

The SFilter configuration register controls the minimum and maximum values allow for the clock to data sample timing. TI recommends to program this register to 0xA9 during initialization for optimal startup time and to ensure consistent AEQ performance across different channel characteristics.

Table 7. SFILTER_CFG (Address 0x41)

BIT	FIELD	TYPE	954 DEFAULT	960 DEFAULT	DESCRIPTION
7:4	SFILTER_MAX	R/W	0xA	0xE	SFILTER Maximum Setting This field controls the maximum SFILTER setting. Allowed values are 0-14 with 7 being the mid point. These values are used for both AEQ adaption and dynamic SFILTER control. The maximum setting must be greater than or equal to the minimum setting. If AEQ_SFIL_ORDER is set in the AEQ_CTL register, the SFILTER_MAX value should not be set lower than 0x7.

Table 7. SFILTER_CFG (Address 0x41) (continued)

BIT	FIELD	TYPE	954 DEFAULT	960 DEFAULT	DESCRIPTION
3:0	SFILTER_MIN	R/W	0x7	0x0	SFILTER Minimum Setting This field controls the maximum SFILTER setting. Allowed values are 0-14, where 7 is the mid point. These values are used for both AEQ adaption and dynamic SFILTER control. The minimum setting must be less than or equal to the SFILTER_MAX. Recommended to set SFILTER_MIN = 0x9 for normal operation in typical system use cases. If AEQ_SFIL_ORDER is set in the AEQ_CTL register, the SFILTER_MIN value should not be set higher than 0x6.

5.1.2 AEQ_CTL1 Register

Table 8. AEQ_CTL1 (Address 0x42)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved
6:4	AEQ_ERR_CTL	R/W	0x7	AEQ Error Control Setting any bits in AEQ_ERR_CTL will enable FPD3 error checking during the Adaptive Equalization process. Errors are accumulated over 1/2 of the period of the timer set by the ADAPTIVE_EQ_RELOCK_TIME filed in the AEQ_CTL2 register. If the number of errors is greater than the programmed threshold (AEQ_ERR_THOLD), the AEQ will attempt to increase the EQ setting. The errors may also be checked as part of EQ setting validation if AEQ_2STEP_EN is set. The following errors are checked based on this three bit field: [6] FPD-Link III clock errors [5] Packet encoding errors [4] Parity errors
3	RESERVED	R/W	0x0	Reserved
2	AEQ_2STEP_EN	R/W	0x0	AEQ 2-step enable This bit enables a two-step operation as part of the Adaptive EQ algorithm. If disabled, the state machine will wait for a programmed period of time, then check status to determine if setting is valid. If enabled, the state machine will wait for 1/2 the programmed period, then check for errors over an additional 1/2 the programmed period. If errors occur during the 2nd step, the state machine will immediately move to the next setting. 0 : Wait for full programmed delay, then check instantaneous lock value 1 : Wait for 1/2 programmed time, then check for errors over 1/2 programmed time. The programmed time is controlled by the ADAPTIVE_EQ_RELOCK_TIME field in the AEQ_CTL2 register
1	AEQ_OUTER_LOOP	R/W	0x0	AEQ outer loop control This bit controls whether the Equalizer or SFILTER adaption is the outer loop when the AEQ adaption includes SFILTER adaption. 0 : AEQ is inner loop, SFILTER is outer loop 1 : AEQ is outer loop, SFILTER is inner loop
0	AEQ_SFILTER_EN	R/W	0x1	Enable SFILTER Adaption with AEQ Setting this bit allows SFILTER adaption as part of the Adaptive Equalizer algorithm.

5.1.3 RX_PORT_STS1 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Table 9. RX_PORT_STS1 (Address 0x4D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved

Table 9. RX_PORT_STS1 (Address 0x4D) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
6	RX_PORT_NUM	R	0x0	RX Port Number. This read-only field indicates the number of the currently selected RX read port.
5	BCC_CRC_ERROR	R/RC	0x0	Bi-directional Control Channel CRC Error Detected This bit indicates a CRC error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read.
4	LOCK_STS_CHG	R/RC	0x0	Lock Status Changed This bit is set if a change in receiver lock status has been detected since the last read of this register. Current lock status is available in the LOCK_STS bit of this register. This bit is cleared on read.
3	BCC_SEQ_ERROR	R/RC	0x0	Bi-directional Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read.
2	PARITY_ERROR	R	0x0	FPD-Link III parity errors detected This flag is set when the number of parity errors detected is greater than the threshold programmed in the PAR_ERR_THOLD registers. 1: Number of FPD-Link III parity errors detected is greater than the threshold 0: Number of FPD-Link III parity errors is below the threshold This bit is cleared when the RX_PAR_ERR_HI/LO registers are cleared.
1	PORT_PASS	R	0x0	Receiver PASS indication. This bit indicates the current status of the Receiver PASS indication. The requirements for setting the Receiver PASS indication are controlled by the PORT_PASS_CTL register. 1: Receive input has met PASS criteria 0: Receive input does not meet PASS criteria
0	LOCK_STS	R	0x0	FPD-Link III receiver is locked to incoming data 1: Receiver is locked to incoming data 0: Receiver is not locked

5.1.4 RX_PORT_STS2 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Table 10. RX_PORT_STS2 (Address 0x4E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	LINE_LEN _UNSTABLE	R/RC	0x0	Line Length Unstable If set, this bit indicates the line length was detected as unstable during a previous video frame. The line length is considered to be stable if all the lines in the video frame have the same length. This flag will remain set until read.
6	LINE_LEN_CHG	R/RC	0x0	Line Length Changed 1: Change of line length detected 0: Change of line length not detected This bit is cleared on read.
5	FPD3_ENCODE _ERROR	R/RC	0x0	FPD-Link III Encoder error detected If set, this flag indicates an error in the FPD-Link III encoding has been detected by the FPD-Link III receiver. This bit is cleared on read. Note, to detect FP3 Encoder errors, the LINK_ERROR_COUNT must be enabled with a LINK_ERR_THRESH value greater than 1. Otherwise, the loss of Receiver Lock will prevent detection of the Encoder error.
4	BUFFER_ERROR	R/RC	0x0	Packet buffer error detected. If this bit is set, an overflow condition has occurred on the packet buffer FIFO. 1: Packet Buffer error detected 0: No Packet Buffer errors detected This bit is cleared on read.

Table 10. RX_PORT_STS2 (Address 0x4E) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
3	CSI_ERROR	R	0x0	CSI Receive error detected. See the CSI_RX_STS register for details.
2	FREQ_STABLE	R	0x0	Frequency measurement stable
1	CABLE_FAULT	R	0x0	When link is expected to be operational, CABLE_FAULT would indicate open or short on the cable as no FPD-Link clock is detected at the deserializer Rx input.
0	LINE_CNT_CHG	R/RC	0x0	Line Count Changed 1: Change of line count detected 0: Change of line count not detected This bit is cleared on read.

5.1.5 LINK_ERROR_COUNT Register

Table 11. LINK_ERROR_COUNT (Address 0xB9)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	R	0x0	Reserved
5	LINK_SFIL_WAIT	R/W	0x1	During SFILTER adaption, setting this bit will cause the Lock detect circuit to ignore errors during the SFILTER wait period after the SFILTER control is updated. 1: Errors during SFILTER Wait period will be ignored 0: Errors during SFILTER Wait period will not be ignored and may cause loss of Lock
4	LINK_ERR _COUNT_EN	R/W	0x1	Enable serial link data integrity error count 1: Enable error count 0: DISABLE
3:0	LINK_ERR _THRESH	R/W	0x3	Link error count threshold. The Link Error Counter monitors the forward channel link and determines when link will be dropped. The link error counter is pixel clock based. FPD-Link parity, clock, and control are monitored for link errors. If the error counter is enabled, the deserializer will lose lock once the error counter reaches the LINK_ERR_THRESH value. If the link error counter is disabled, the deserializer will lose lock after one error.

Table 12. PORT_DEBUG (Address 0xD0)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	DIS_SFIL_MINMAX	RW	0	Disable SFILTER Min/Max This bit controls whether the Minimum and Maximum SFILTER settings in the SFILTER_CFG register will be used by the Dynamic SFILTER adaption routine. 0 : Use SFILTER Min/Max 1 : Use full range of SFILTER settings
6	RESERVED	R/W	0x0	Reserved
5	SER_BIST_ACT	R	0x0	Serializer BIST active This register indicates the Serializer is in BIST mode. When in BIST mode this flag can be checked to ensure BIST is activated in the serializer during the test. If the Deserializer is not in BIST mode, this could indicate an error condition.
4:2	RESERVED	R/W	0x0	Reserved
1	FORCE _BC_ERRORS	R/W	0x0	Setting this bit introduces continuous single bit errors into Back Channel Frames
0	FORCE _1_BC_ERROR	R/W	0x0	Setting this bit introduces a single bit error into one Back Channel Frame

5.1.6 AEQ_CTL2 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Table 13. AEQ_CTL2 (Address 0xD2)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	ADAPTIVE_EQ _RELOCK_TIME	R/W	0x4	Time to wait for lock before incrementing the EQ to next setting 000 : 164 µs 001 : 328 µs 010 : 655 µs 011 : 1.31 ms 100 : 2.62 ms 101 : 5.24 ms 110 : 10.5 ms 111 : 21.0 ms
4	AEQ_1ST_LOCK _MODE	R/W	0x1	AEQ First Lock Mode. This register bit controls the Adaptive Equalizer algorithm operation at initial Receiver Lock. 0 : Initial AEQ lock may occur at any value 1 : Initial Receiver lock will restart AEQ at 0, providing a more deterministic initial AEQ value
3	AEQ_RESTART	(R/W)/SC	0x0	Set high to restart AEQ adaptation from initial value. This bit is self clearing. Adaption is restarted.
2	SET_AEQ_FLOOR	R/W	0x1	AEQ adaptation starts from a pre-set floor value rather than from zero - good in long cable situations
1:0	RESERVED	R	0x0	Reserved

5.1.7 ADAPTIVE EQ BYPASS Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Table 14. ADAPTIVE EQ BYPASS (Address 0xD4)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	EQ_STAGE_1 _SELECT_VALUE	R/W	0x3	EQ select value [5:3] - Used if adaptive EQ is bypassed.
4	AEQ_LOCK_MODE	R/W	0x0	Adaptive Equalizer lock mode When set to a 1, Receiver Lock status requires the Adaptive Equalizer to complete adaption. When set to a 0, Receiver Lock is based only on the Lock circuit itself. AEQ may not have stabilized.
3:1	EQ_STAGE_2 _SELECT_VALUE	R/W	0x0	EQ select value [2:0] - Used if adaptive EQ is bypassed.
0	ADAPTIVE_EQ _BYPASS	R/W	0x0	1: Disable adaptive EQ 0: Enable adaptive EQ

5.1.8 AEQ_MIN_MAX Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Table 15. AEQ_MIN_MAX (Address 0xD5)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	AEQ_MAX	R/W	0xF	Adaptive Equalizer Maximum value This register sets the maximum value for the Adaptive EQ algorithm. Must be higher than ADAPTIVE_EQ_FLOOR_VALUE when SET_AEQ_FLOOR is enabled.

Table 15. AEQ_MIN_MAX (Address 0xD5) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
3:0	ADAPTIVE_EQ _FLOOR_VALUE	R/W	0x2	When AEQ floor is enabled by register 0xD2[2] the starting EQ gain setting for AEQ adaption is given by this register.

5.1.9 SFILTER_STS_0 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Table 16. SFILTER_STS_0 (Address 0xD6)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:3	RESERVED	R	0x0	Reserved
2:0	SFILTER_CDLY	R	0x0	SFILTER Clock Delay Current value of clock delay control to SFILTER circuit.

5.1.10 SFILTER_STS_1 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Table 17. SFILTER_STS_1 (Address 0xD7)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:3	RESERVED	R	0x0	Reserved
2:0	SFILTER_DDLY	R	0x0	SFILTER Data Delay Current value of data delay control to SFILTER circuit.

5.2 Indirect Access Registers

Several functional blocks include register sets contained in the Indirect Access map. Register access is provided through an indirect access mechanism through the Indirect Access registers (IND_ACC_CTL, IND_ACC_ADDR, and IND_ACC_DATA). These registers are located at offsets 0xB0-0xB2 in the main register space.

The indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register. In addition, an auto-increment function is provided in the control register to automatically increment the offset address following each read or write of the data register.

For writes, the process is as follows:

1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Write the data value to the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 will write additional data bytes to subsequent register offset locations

For reads, the process is as follows:

1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Read from the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 will read additional data bytes from subsequent register offset locations.

When working with strobe position settings, only a single indirect register is used, STROBE_SET. To access this register, IND_ACC_CTL should be set to 0x04 when working with Port 0 and set to 0x08 when working with Port 1. Refer to the *DS90UB954-Q1 Datasheet* (SNLS570) or *DS90UB960-Q1 Datasheet* (SNLS589) for a full description of indirect access registers.

5.2.1 STROBE_SET Register

RX port specific register. IND_ACC_CTL configures which unique RX port registers can be accessed by I2C read and write commands.

Table 18. STROBE_SET (Address 0x08)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	DDLY_CTRL _GROSS	RW	0	0: 6 extra buffer delay (default) 1: no extra buffer delay
6:4	DDLY_CTRL	RW	0x0	0: 0 extra buffer delay 1: 1 extra buffer delay 2: 2 extra buffer delay 3: 3 extra buffer delay 4: 4 extra buffer delay 5: 5 extra buffer delay 6: 6 extra buffer delay 7: 7 extra buffer delay Manual control should not be used unless other adaption modes are disabled (0x42[0] = 0 and 0x40[0] = 0).
3	CDLY_CTRL _GROSS	RW	0	0: 6 extra buffer delay (default) 1: no extra buffer delay
2:0	CDLY_CTRL	RW	0x0	0: 0 extra buffer delay 1: 1 extra buffer delay 2: 2 extra buffer delay 3: 3 extra buffer delay 4: 4 extra buffer delay 5: 5 extra buffer delay 6: 6 extra buffer delay 7: 7 extra buffer delay Manual control should not be used unless other adaption modes are disabled (0x42[0] = 0 and 0x40[0] = 0).

6 Glossary

- AEQ - The FPD-Link III receiver inputs incorporates an adaptive equalizer (AEQ), to compensate for signal degradation from the communications channel and interconnect components. Each RX port signal path continuously monitors cable characteristics for long-term cable aging and temperature changes. The AEQ is primarily intended to adapt and compensate for channel losses over the lifetime of a cable installed in an automobile. The AEQ attempts to optimize the equalization setting of the RX receiver. This adaption includes compensating insertion loss from temperature effects and aging degradation due to bending and flexion.
- Strobe Position - Also referred to in registers as "Sfilter". This refers to where in the signal eye the data is sampled and corresponds to the amount of either clock delay (sometimes referred to as cdly) or data delay (sometimes referred to as ddly). Increasing the amount of clock delay moves sampling later whereas increasing the amount of data delay moves sampling earlier.
- EQ Level - This refers to the equalization level.
- ALP - This refers to the software GUI used with FPD-Link parts, the Analog LaunchPad development kit.
- Margin Analysis - This refers to examining the size of the margin of the FPD-Link channel. In general, the margin refers to how likely it is that the channel would cause errors or loss of lock as a result of system parameters such as cable length, cable type, or layout. In particular, margin analysis is done by looking at all combinations of EQ levels and strobe positions. Systems with a greater number of passing settings have a larger margin.

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