Application Note

DP83TC811: Configuring for Open Alliance Specification Compliance

ABSTRACT

OA TC1 mandates different tests for 100Base-T1 PHY. This document describes the procedure to put the DP83TC811R/S in the required test mode to carry out these different tests.

The software and hardware configurations used during the DP83TC811's TC1 testing can be found in this document. This configuration has been tested across different OA compliance tests for IEEE conformance, EMI/EMC, and Interoperability, and should be treated as a minimum requirement. Further improvement based on the customer's system use-case is possible with additional hardware and software configuration.

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Trademarks

1 Introduction

The DP83TC811 was evaluated in accordance with the following OPEN Alliance (OA) specifications:

- OPEN Alliance 100BASE-T1 EMC Test Specification for Transceivers - Revision 1.0, by FTZ Zwickau e.V.
- OPEN Alliance 100BASE-T1 Interoperability Test Suite v1.0, by C&S Group, GmbH
- OPEN Alliance 100BASE-T1 test specifications for Physical Coding Sublayer (v. 1.0), PHY Control (v. 1.0) and Physical Media Attachment (v. 1.2) by University of New Hampshire (UNH) Inter-Operability Lab.

This application note provides the details of the unique hardware and software configuration used for all of the above tests.

This document also provides the required procedure details for these tests to assist customers implementing corresponding ECU level tests.

2 Hardware Configuration

2.1 Schematic

Schematics and the right components for MDI, reference clock, and power network are very critical for the performance of 100Base-T1 PHY. This section captures the recommended schematics and component values used during OA TC1 testing.

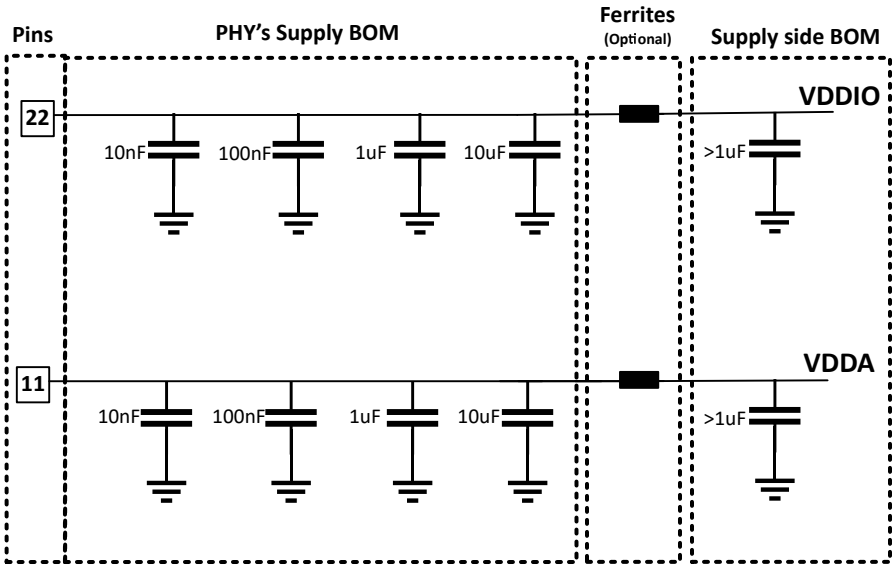

Figure 2-1. Power Supply Network

Table 2-1. Power Supply Parameters, Components and Values

Parameter/Component	Value
V_{DDIO}	1.8 V, 2.5 V, or 3.3 V
De-Coupling Capacitors V_{DDIO}	10 nF, 100 nF, 1uF, 10uF
(Optional) Ferrite Bead V_{DDIO}	1 kΩ at 100 MHz (BLM18AG102SH)
V_{DDA}	3.3 V
De-Coupling Capacitors V_{DDA}	10 nF, 100 nF, 1uF, 10uF
(Optional) Ferrite Bead V_{DDA}	1 kΩ at 100 MHz (BLM18AG102SH)

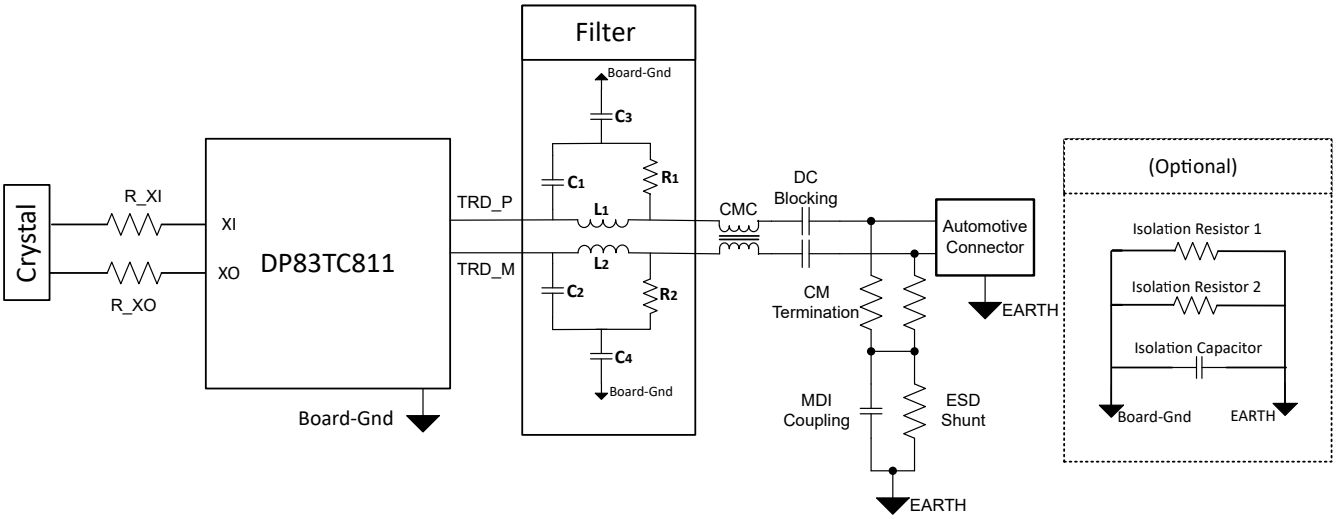

Figure 2-2. MDI and Crystal Schematic

Table 2-2. Crystal and MDI Parameters, Components and Values

Parameter/Component	Value
Filter - R_1, R_2 (1% accurate)	22 Ω
Filter - C_1, C_2 (2% accurate)	22pF
Filter - C_3, C_4 (2% accurate)	47pF
Filter - L_1, L_2 (2% accurate)	120nH
DC Blocking Capacitors (1% accurate, 100V)	0.1 µF
Common-Mode Choke	TDK: ACT1210L-201
	TDK: ACT45L-201
	Murata: DLW32MH201XK2
	Murata: DLW43MH201XK2L
	Pulse: AE2002
Common Mode Termination Resistors (1% accurate,0.75 W, Size: 2010)	1 kΩ
MDI Coupling Capacitor	4.7 nF
ESD Shunt (5% accurate, 0.125 W, Size: 0805)	100 kΩ
Isolation Resistor 1 (0.25 W, Size: 1206)	0 Ω
Isolation Resistor 2 (0.25 W, Size: 1206)	0 Ω
Isolation Capacitor	Not populated
Crystal	
R_XI	100 Ω
R_XO	200 Ω Adding series resistor is seen to make crystal oscillator more immune to board parasitics, noise and helps in quick startup. TI recommends to use a resistor of value 200 ohms. As this resistor controls the crystal wattage, its value should be chosen in consultation with the crystal vendor.

3 Software Configuration

This section contains the register settings of DP83TC811 used during tests in different OA compliance test houses. Most of these register settings are added to optimize performance during OA & EMC/EMI testing. It is recommended to implement these register settings as part for initialization for all DP83TC811 applications. Other application specific features offered by DP83TC811 can be adjusted via hardware or software configurations.

Table 3-1. Master Mode Configuration

MMD	Register	Optimized	Description
0x1F	0x0475	0x0008	To not let the PHY link-up until config is done
0x1F	0x0485	0x11FF	DSP settings for margins during OA, EMI tests
0x1F	0x0462	0x0600	Disable unused LED_1 on the board
0x1F	0x010F	0x0100	DSP settings for margins during OA, EMI tests
0x1F	0x0410	0x6000	DSP settings for margins during OA, EMI tests
0x1F	0x0479	0x0442	DSP settings for margins during OA, EMI tests
0x1F	0x0466	0x8000	DSP settings for margins during OA, EMI tests
0x1F	0x0107	0x2605	DSP settings for margins during OA, EMI tests
0x1F	0x0106	0xB8BB	DSP settings for margins during OA, EMI tests
0x1F	0x0116	0x03CA	DSP settings for margins during OA, EMI tests
0x1F	0x0114	0xC00A	DSP settings for margins during OA, EMI tests
0x1F	0x010B	0x0700	DSP settings for margins during OA, EMI tests
0x1F	0x0132	0x01EE	DSP settings for margins during OA, EMI tests
0x1F	0x04DE	0x03F0	DSP settings for margins during OA, EMI tests
0x1F	0x003E	0x000D	DSP settings for margins during OA, EMI tests
0x1F	0x0111	0x6009	DSP settings for margins during OA, EMI tests
0x1F	0x0129	0x009F	DSP settings for margins during OA, EMI tests
0x1F	0x04D5	0xFEA4	DSP settings for margins during OA, EMI tests
0x1F	0x04D6	0x0EA4	DSP settings for margins during OA, EMI tests
0x1F	0x0120	0x0067	DSP settings for margins during OA, EMI tests
0x1F	0x0125	0x7A56	DSP settings for margins during OA, EMI tests
0x1F	0x0461	0x0408	Tune IO impedance with board traces
0x1F	0x0400	0x1300	MDI termination optimization
0x1F	0x0403	0x0030	MDI transmission optimization
0x1F	0x0404	0x0008	MDI transmission optimization
0x1F	0x048A	0x0D02	DSP settings for margins during OA, EMI tests
0x1F	0x048B	0x350F	DSP settings for margins during OA, EMI tests
0x1F	0x048C	0x0033	DSP settings for margins during OA, EMI tests
0x1F	0x048D	0x010D	DSP settings for margins during OA, EMI tests
0x1F	0x0121	0x1500	DSP settings for margins during OA, EMI tests
0x1F	0x0122	0x1000	DSP settings for margins during OA, EMI tests
0x1F	0x04D4	0x7522	DSP settings for margins during OA, EMI tests
0x1F	0x0130	0xC720	DSP settings for margins during OA, EMI tests
0x1F	0x0126	0x0515	DSP settings for margins during OA, EMI tests
0x1F	0x0119	0x00A4	DSP settings for margins during OA, EMI tests
0x1F	0x0109	0x095D	DSP settings for margins during OA, EMI tests
0x1F	0x010E	0x3219	DSP settings for margins during OA, EMI tests
0x1F	0x010C	0x1996	DSP settings for margins during OA, EMI tests
0x1F	0x001F	0x4000	Soft reset
0x1F	0x0475	0x0000	Let the PHY link-up

Table 3-2. Slave Mode Configuration

MMD	Register	Optimized	Description
0x1F	0x0475	0x0008	To not let the PHY link-up until config is done
0x1F	0x0485	0x11FF	DSP settings for margins during OA, EMI tests
0x1F	0x0462	0x0600	Disable unused LED_1 on the board
0x1F	0x010F	0x0100	DSP settings for margins during OA, EMI tests
0x1F	0x0410	0x6000	DSP settings for margins during OA, EMI tests
0x1F	0x0479	0x0442	DSP settings for margins during OA, EMI tests
0x1F	0x0466	0x8000	DSP settings for margins during OA, EMI tests
0x1F	0x0107	0x2605	DSP settings for margins during OA, EMI tests
0x1F	0x0106	0xB8BB	DSP settings for margins during OA, EMI tests
0x1F	0x0116	0x03CA	DSP settings for margins during OA, EMI tests
0x1F	0x0114	0xC00A	DSP settings for margins during OA, EMI tests
0x1F	0x010B	0x0700	DSP settings for margins during OA, EMI tests
0x1F	0x0132	0x01EE	DSP settings for margins during OA, EMI tests
0x1F	0x04DE	0x03F0	DSP settings for margins during OA, EMI tests
0x1F	0x003E	0x000D	DSP settings for margins during OA, EMI tests
0x1F	0x0111	0x6009	DSP settings for margins during OA, EMI tests
0x1F	0x0129	0x009F	DSP settings for margins during OA, EMI tests
0x1F	0x04D5	0xFEA4	DSP settings for margins during OA, EMI tests
0x1F	0x04D6	0x0EA4	DSP settings for margins during OA, EMI tests
0x1F	0x0120	0x0067	DSP settings for margins during OA, EMI tests
0x1F	0x0125	0x7A56	DSP settings for margins during OA, EMI tests
0x1F	0x0461	0x0408	Tune IO impedance with board traces
0x1F	0x0400	0x1300	MDI termination optimization
0x1F	0x0403	0x0030	MDI transmission optimization
0x1F	0x0404	0x0008	MDI transmission optimization
0x1F	0x048A	0x0D02	DSP settings for margins during OA, EMI tests
0x1F	0x048B	0x350F	DSP settings for margins during OA, EMI tests
0x1F	0x048C	0x0033	DSP settings for margins during OA, EMI tests
0x1F	0x048D	0x010D	DSP settings for margins during OA, EMI tests
0x1F	0x0121	0x1500	DSP settings for margins during OA, EMI tests
0x1F	0x0122	0x1450	DSP settings for margins during OA, EMI tests
0x1F	0x04D4	0x7322	DSP settings for margins during OA, EMI tests
0x1F	0x0130	0xC780	DSP settings for margins during OA, EMI tests
0x1F	0x0126	0x0495	DSP settings for margins during OA, EMI tests
0x1F	0x0115	0x8AC8	DSP settings for margins during OA, EMI tests
0x1F	0x0109	0x095D	DSP settings for margins during OA, EMI tests
0x1F	0x010E	0xFAFB	DSP settings for margins during OA, EMI tests. Value can be changed to x7DFB if further reduction in link-up time is required
0x1F	0x010C	0x19FA	DSP settings for margins during OA, EMI tests
0x1F	0x0101	0x2082	DSP settings for margins during OA, EMI tests
0x1F	0x001F	0x4000	Soft reset
0x1F	0x0475	0x0000	Let the PHY link-up

Note

Sequence of above register writes is important. For both master and slave configuration all the DSP settings are in-between the writes to register 0x0475. This is to make sure that the link-up sequence does not start before the full configuration is written.

4 Testing PMA

OA TC1 specifies different electrical tests for 100Base-T1 PHY's front end. Different test modes have been specified in the standard document. In each test mode, PHY is supposed to generate patterns on MDI lines or expose internal clock signal on a pin for measurement of different electrical parameters.

DP83TC811 supports all these test modes. This section gives details of the required configuration to enter into each test mode.

Detailed PMA test report from UNH (OA compliance test house) with OA/IEEE compliant results are available on request.

4.1 PMA Testing Procedure

Note

- Before programming any of the test modes, DP83TC811 should be loaded with the respective initialization register configuration (master or slave) as described in earlier sections.
- SLAVE transmit jitter requires link to be established between DUT and link-partner, hence register [0x0001] should read as 0x0065 before running the test.

Table 4-1. Programming PMA Test Modes

Test Mode	Parameter Under Test	MMD	Register	Value
Test Mode 1	Transmit Droop	0x01	0x0904	0x2001
Test Mode 2	MASTER transmit jitter	0x01	0x0904	0x4001
Test Mode 4	Transmit Distortion	0x01	0x0904	0x8001
		0x1F	0x0462	0x0011
Test Mode 5	Transmit PSD	0x01	0x0904	0xA001
-	SLAVE transmit jitter	0x1F	0x0462	0x0011

TX_TCLK (66.66MHz) is needed for Trasnmit Distortion and SLAVE transmit jitter testing. The clock is programmed to be transmitted on LED_0 using the write reg<0x0462> = 0x0011.

5 Testing IOP: Link-up and Link-down

OA TC1 specifies different PHY level tests to test link-up time, link-down time and link stability. Similar ECU level tests have been highlighted in OA TC8. This section highlights the test sequence used for these IOP tests for PHY level testing and the same can be ported for ECU level tests.

TC1-interoperability tests are carried out by OA compliance test house C&S. To test interoperability of DP83TC811, C&S tests each of these parameters with DP83TC811 and other 100Base-T1 certified PHYs as its link-partners. Each of these parameters are tested for large number of iterations over different temperatures and cable lengths.

Detailed IOP test report from C&S with OA compliant results is available on request.

5.1 IOP Testing Procedure

Start of measurement:

For the IOP tests measuring link-up time either after power-up or after hardware reset, it is important to start the measurement of link-up time after the initialization configuration is loaded back into DP83TC811. As the configuration is loaded into the PHY by a controller, we recommend the controller to give an indication (a software bit or an IO state) after the last configuration register is written. This indicator going high is the start of measurement of link-up time.

Status to be poled:

Link-status is indicated by bit 14 of register 0x0133: 1 = link-up; 0 = link-down. This should be poled to indicate the event of link-up or link-down during these tests.

Note

If system desires no automatic link-up after power-up (link to only happen after writing the initialization script), managed mode of DP83TC811 should be used by using strap on pin LED_1.

6 Testing SQI

SQI gives the indication of signal quality on the copper cable.

OA TC-1 indicates that SQI values should decrease monotonically with increase in noise levels.

Detailed SQI test report from C&S with OA compliant results is available on request.

6.1 SQI Testing Procedure

When the DP83TC811 is active, the Signal Quality Indicator may be used to determine the quality of link based on SNR readings made by the device. Signal quality indication is accessible through bits[7:0] of SQI Register 0x0198 – Signal Quality Indication Register. SQI is continuously monitored by the DP83TC811 to allow for real-time link signal quality status.

6.2 SQI Mapping with Link Quality

The following table maps the read value of Register 0x198[7:0] (SQI 8-bit) with OA specified 3-bit SQI value and link quality.

Table 6-1. SQI Mapping from 8-bit to 3-bit

SQI 8-bit	SQI 3-bit	Link Quality
SQI < 0x28	0	*No link
0x28 ≤ SQI < 0x31	1	Bad
0x31 ≤ SQI < 0x3B	2	
0x3B ≤ SQI < 0x44	3	
0x44 ≤ SQI < 0x4B	4	
0x4B ≤ SQI < 0x58	5	Good
0x58 ≤ SQI < 0x64	6	Excellent
0x64 ≤ SQI	7	

7 Testing TDR

This section describes the procedure to test cable faults: open/short.

Detailed TDR test report from C&S with OA compliant results is available on request.

Note

OA TC1 tests done at C&S tests are for open and short cable fault test cases. Also TDR is usually run to find root-cause when there is no link. Test procedure described in next section has an extra step over compliance test procedure: to force link-down condition when possible (use if required).

7.1 TDR Testing Procedure

Table 7-1. TDR Run Procedure

Sequence	Description	Register Read/Write
Step 1: For DP83TC811 as master	Force the link-down by writing register and enable link-partner to go silent. Wait for ~1s after register write. In case of valid open and short cable faults, TDR will still work fine without step 1. For good cable case, TDR register 0x001E may show *Fail* on bypassing this step.	Write register[0x0475] = 0x0008
Step 1: For DP83TC811 as slave	Link-partner should be made silent. In case of valid open and short cable faults, TDR will still work fine without step 1. For good cable case, TDR register 0x001E may show *Fail* on bypassing this step.	If DP83TC811 is the link partner, then • Write register [0x0475] = 0x0008 Else, • Check with the PHY vendor about how to make link partner silent
Step 2	Start TDR	0x001E[15] = 1
Step 3	Wait for 100ms (should be sufficient for TDR to converge for maximum cable length)	
Step 4	Check wether TDR is completed successfully	Read 0x001E[1:0] = [TDR done : TDR fail]. • Value should be [1,0]. Fault type/ locations are valid only if this correct value is read. • Value other than [1,0] will mean that there is some noise/signal on the line which is causing TDR to fail.
Step 5	Fault type and location is read.	Read register 0x016B for fault status and fault type. • 0x016B[9] = 0 indicates that no fault is detected • If a valid fault is detected, then register 0x016B[9:8] = 'b11(short) or 'b10(open) • In this case, the fault location is read as 1.5 * decimal(0x016B[7:0])

8 Testing EMC/EMI

OA TC1 specifies conducted EMC/EMI tests. For DP83TC811, these tests were carried out in OA compliance test house FTZ and testing of emissions on MDI, emissions on each supply pin, immunity to RF signals are part of the test suite. The board was designed in accordance with OA specifications by FTZ.

Hardware and software configurations highlighted in the document were used for these conducted EMC/EMI tests. Configurations are available if further enhancement over TC1 specs are required for an application.

Detailed test report from FTZ with procedures and OA compliant results is available on request.

Other than OA EMC/EMI tests, DP83TC811 has also been tested for OEM-specific EMC standards. Detailed reports for these tests are also available upon request.

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