DP83TC811 Systems and Reference Schematics

The DP83TC811 is designed to support a wide range of applications with configurable MAC interfaces, features and modes of operation. This application note provides detailed information of possible applications for the DP83TC811 and suggested approaches to expedite the design process.

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Trademarks

1 Introduction

The DP83TC811 is an automotive 100 Mbps Ethernet Physical Layer Transceiver compliant to IEEE802.3bw (100BASE-T1). This device supports the following MAC interfaces: MII, RMII, RGMII and SGMII. To decrease time-to-market, this application note outlines various reference designs depending on the application requirements. Associated Altium schematics, layout and BOM will provided upon request and approval.

Table 1. Terminology

ACRONYM	DEFINITION
PHY	Physical Layer Transceiver
PMA	Physical Medium Attachment
TX	Transmit - Digital Pins
RX	Receive - Digital Pins
SGMII	Serial Gigabit Media Independent Interface
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
MII	Media Independent Interface
MAC	Media Access Controller
VDDIO	DP83TC811 Digital Supply Rail
CM	Common Mode
CMC	Common Mode Choke
ESD	Electrostatic Discharge
LPF	Low Pass Filter

2 MII Reference Design

This section provides a recommended schematic for connection to an MII MAC interface. External bootstraps have been added to allow for MII configuration at power-up/reset. This reference design is configured for PMA Slave mode since LED_0 (MS Strap) is pulled LOW internally by default.

Table 2. MII Bootstrap Configuration

PIN	BOOTSTRAP TYPE	MODE	DESCRIPTION
RX_DV	PHY_ID[0] PHY_ID[2]	1	PHY Address = 0x00
RX_ER	PHY_ID[1] PHY_ID[3]	1	
RX_D0	MAC[0] TEST[0]	4	MII Operation
RX_D1	MAC[1] TEST[1]	1	
RX_D2	MAC[2] TEST[2]	1	
LED_0	MS	1	Slave
LED_1	AUTO	1	Autonomous Operation

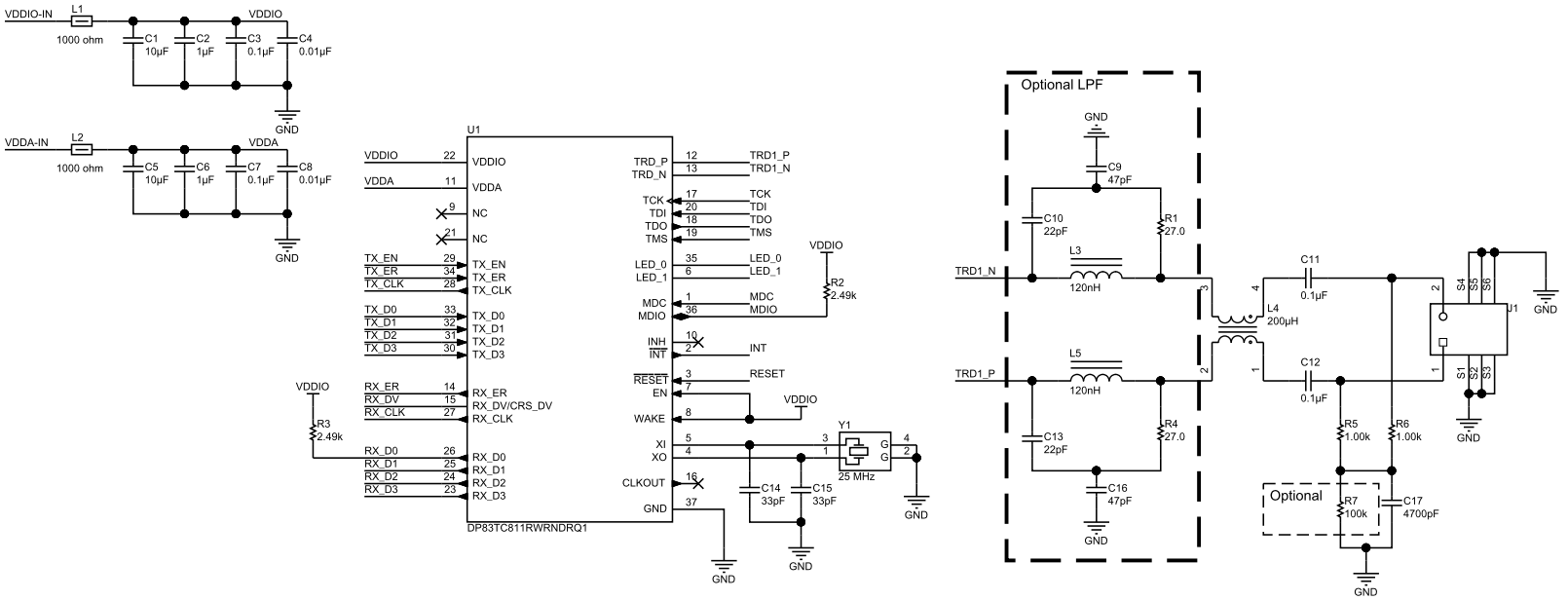

Figure 1. MII Schematic

2.1 MII Digital Pin Routing

When configured for MII operation, the PHY will output with a 25MHz reference clock on both the TX_CLK and RX_CLK pins.

For this excursive, we will assume use with FR4, which has a propagation delay of ~1n/15.24cm.

DP83TC811 allows for a minimum setup time of 10ns and hold time of 0ns.

DP83TC811 has a maximum data delay from clock of 25ns and a minimum of 15ns.

In order to maintain timing requirements, it is recommended that data-to-data and data-to-clock not exceed length mismatch of more than:

5 ns (margin) X 15.24 cm / 1 ns = 76.2 cm (1)

Note: Receive path mismatch will be determined by the minimum setup and hold time of the MAC.

Note: Digital pin groupings that should be length match in relation to each other:

- Group #1 (Receive Path)
  - RX_DV, RX_D[3:0], RX_ER, RX_CLK
- Group #2 (Transmit Path)
  - TX_EN, TX_D[3:0], TX_ER, TX_CLK
- Group #3 (SMI)
  - MDIO, MDC

Note: All group members should be routed with 50 Ω impedance to ground.

Note: When a pin is not used, it may be left unconnected (floating). Each digital pin has either an internal pull-up or pull-down. For additional pin pull-up and pull-down description, please see the DP83TC811 datasheet.

Note: For EMI/EMC concerns, it may be desirable to place a small capacitance on the RX_CLK and TX_CLK traces. It is recommended to start with a capacitance of 10pF on these signals.

3 RMII Reference Designs

This section provides recommended schematics for connection to an RMII MAC interface with either RMII Slave mode or RMII Master mode.

3.1 RMII Slave Reference Design

External bootstraps have been added to allow for RMII Slave configuration at power-up/reset. This reference design is configured for PMA Slave Mode since LED_0 (MS Strap) is pulled LOW internally by default.

Table 3. RMII Slave Bootstrap Configuration

PIN	BOOTSTRAP TYPE	MODE	DESCRIPTION
RX_DV	PHY_ID[0] PHY_ID[2]	1	PHY Address = 0x00
RX_ER	PHY_ID[1] PHY_ID[3]	1	
RX_D0	MAC[0] TEST[0]	1	RMII Slave Operation
RX_D1	MAC[1] TEST[1]	4	
RX_D2	MAC[2] TEST[2]	1	
LED_0	MS	1	Slave
LED_1	AUTO	1	Autonomous Operation

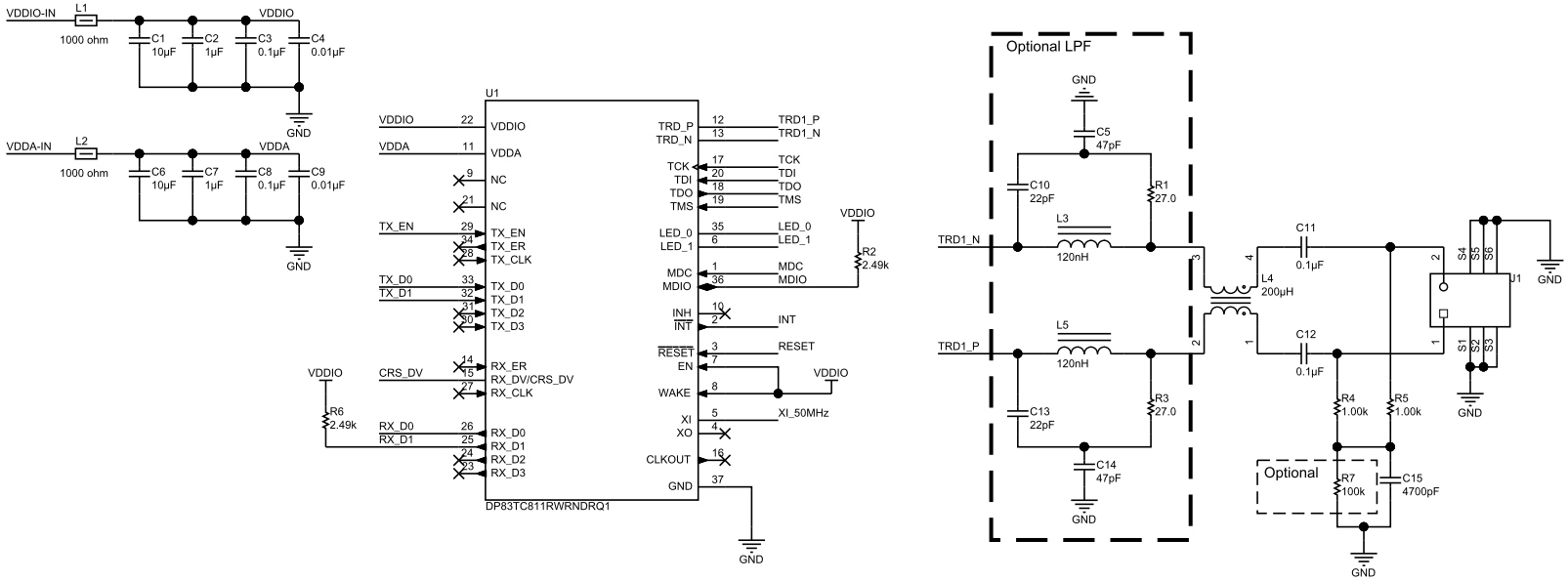

Figure 2. RMII Slave Schematic

A 50MHz CMOS-level oscillator must be shared between the MAC and PHY. This reference clock is used for both TX and RX data paths. CMOS-level of the oscillator must be the same as VDDIO supply rail.

Note: X0 pin should be left unconnected when using an external CMOS-level oscillator.

3.2 RMII Slave Digital Pin Routing

For this excursive, we will assume use with FR4, which has a propagation delay of ~1n/15.24cm.

DP83TC811 allows for a minimum setup time of 4ns and hold time of 2ns.

DP83TC811 has a maximum data delay from clock of 12ns and a minimum of 4ns.

In order to maintain timing requirements, it is recommended that data-to-data and data-to-clock not exceed length mismatch of more than:

2 ns (margin) X 15.24 cm / 1 ns = 30.48 cm (2)

Note: Receive path mismatch will be determined by the minimum setup and hold time of the MAC.

Note: Digital pin groupings that should be length match in relation to each other:

- Group #1
  - TX_D[1:0], TX_EN, RX_D[1:0], CRS_DV, 50MHz Reference Clock (XI pin)
- Group #2 (SMI)
  - MDIO, MDC

Note: All group members should be routed with 50 Ω impedance to ground.

Note: When a pin is not used, it may be left unconnected (floating). Each digital pin has either an internal pull-up or pull-down. For additional pin pull-up and pull-down description, please see the DP83TC811 datasheet.

3.3 RMII Master Reference Design

External bootstraps have been added to allow for RMII Master configuration at power-up/reset. This reference design is configured for PMA Slave Mode since LED_0 (MS Strap) is pulled LOW internally by default.

Table 4. RMII Master Bootstrap Configuration

PIN	BOOTSTRAP TYPE	MODE	DESCRIPTION
RX_DV	PHY_ID[0] PHY_ID[2]	1	PHY Address = 0x00
RX_ER	PHY_ID[1] PHY_ID[3]	1	
RX_D0	MAC[0] TEST[0]	4	RMII Slave Operation
RX_D1	MAC[1] TEST[1]	4	
RX_D2	MAC[2] TEST[2]	1	
LED_0	MS	1	Slave
LED_1	AUTO	1	Autonomous Operation

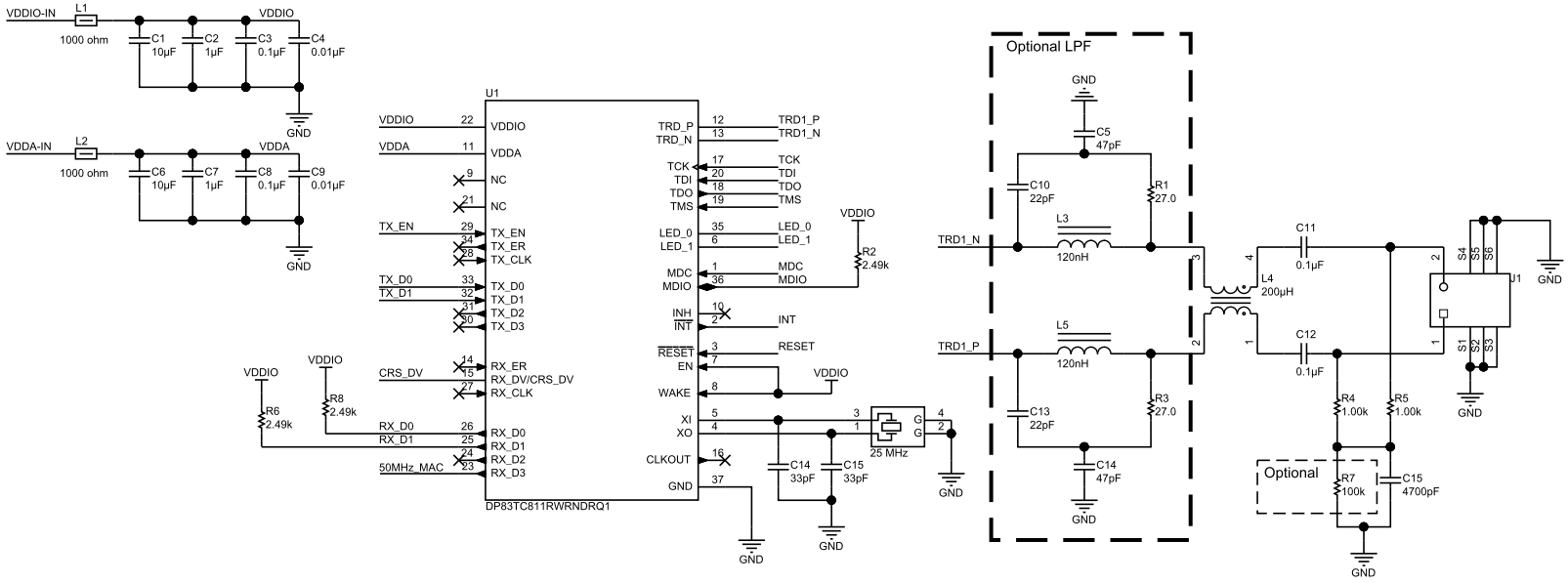

Figure 3. RMII Master Schematic

A 50MHz CMOS-level clock is outputted on RX_D3 when operating in RMII Master mode. This clock reference should be provided to the MAC since it is the reference for both RX and TX data paths.

3.4 RMII Master Digital Pin Routing

When in RMII Master mode, the PHY operates from a 25MHz reference clock. The reference clock can be either a 25MHz (+/-100ppm) crystal connected across XI and XO pins with the appropriate load capacitance or a 25MHz (+/-100ppm) CMOS-level oscillator. The CMOS-level oscillator must operate at the same supply level as VDDIO supply rail.

For this excursive, we will assume use with FR4, which has a propagation delay of ~1n/15.24cm.

DP83TC811 allows for a minimum setup time of 4ns and hold time of 2ns.

DP83TC811 has a maximum data delay from clock of 12ns and a minimum of 4ns.

In order to maintain timing requirements, it is recommended that data-to-data and data-to-clock not exceed length mismatch of more than:

2 ns (margin) X 15.24 cm / 1 ns = 30.48 cm (3)

Note: Receive path mismatch will be determined by the minimum setup and hold time of the MAC.

Note: Digital pin groupings that should be length match in relation to each other:

- Group #1
  - TX_D[1:0], TX_EN, RX_D[1:0], CRS_DV, 50MHz Reference Clock (RX_D3)
- Group #2 (SMI)
  - MDIO, MDC

Note: All group members should be routed with 50 Ω impedance to ground.

Note:: When a pin is not used, it may be left unconnected (floating). Each digital pin has either an internal pull-up or pull-down. For additional pin pull-up and pull-down description, please see the DP83TC811 datasheet.

4 RGMII Reference Designs

This section provides recommended schematics for connection to an RGMII MAC interface: RGMII Align, RX Shift, TX Shift, TX and RX Shift.

4.1 RGMII Align Reference Design

In this design, no skew is introduced between the RGMII clock and data by the DP83TC811. The required delay between the clock and data must be implemented internal to the MAC, or done through PCB routing. External bootstraps have been added to allow for RGMII Align configuration at power-up/reset. This reference design is configured for PMA Slave Mode since LED_0 (MS Strap) is pulled LOW internally by default.

Table 5. RGMII Align Bootstrap Configuration

PIN	BOOTSTRAP TYPE	MODE	DESCRIPTION
RX_DV	PHY_ID[0] PHY_ID[2]	1	PHY Address = 0x00
RX_ER	PHY_ID[1] PHY_ID[3]	1	
RX_D0	MAC[0] TEST[0]	1	RGMII Align Operation
RX_D1	MAC[1] TEST[1]	1	
RX_D2	MAC[2] TEST[2]	4	
LED_0	MS	1	Slave
LED_1	AUTO	1	Autonomous Operation

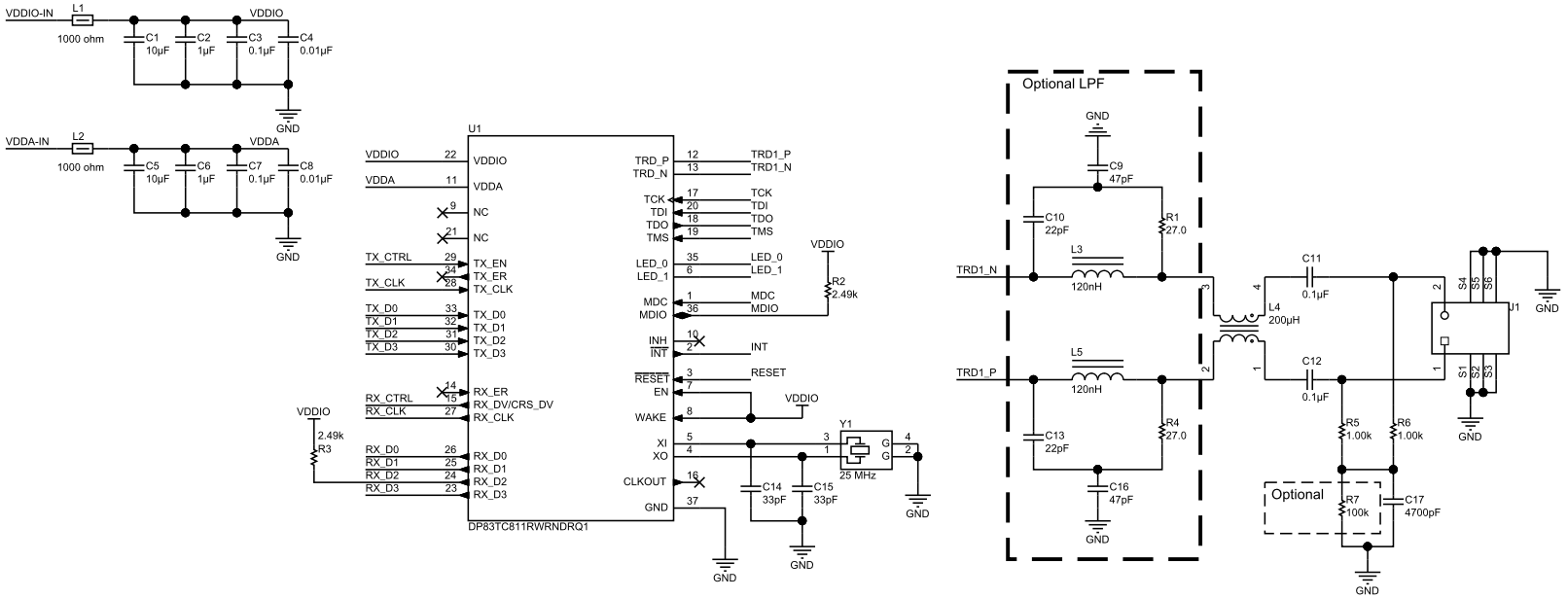

Figure 4. RGMII Align Schematic

4.2 RGMII RX Shift Reference Design

In this design, skew is introduced between the RGMII RX_CLK and RX_data by the DP83TC811. The required delay between the TX_CLK and TX_data must be implemented internal to the MAC, or done through PCB routing. External bootstraps have been added to allow for RGMII RX Shift configuration at power-up/reset. This reference design is configured for PMA Slave Mode since LED_0 (MS Strap) is pulled LOW internally by default.

Table 6. RGMII RX Shift Bootstrap Configuration

PIN	BOOTSTRAP TYPE	MODE	DESCRIPTION
RX_DV	PHY_ID[0] PHY_ID[2]	1	PHY Address = 0x00
RX_ER	PHY_ID[1] PHY_ID[3]	1	
RX_D0	MAC[0] TEST[0]	4	RGMII RX Shift Operation
RX_D1	MAC[1] TEST[1]	4	
RX_D2	MAC[2] TEST[2]	4	
LED_0	MS	1	Slave
LED_1	AUTO	1	Autonomous Operation

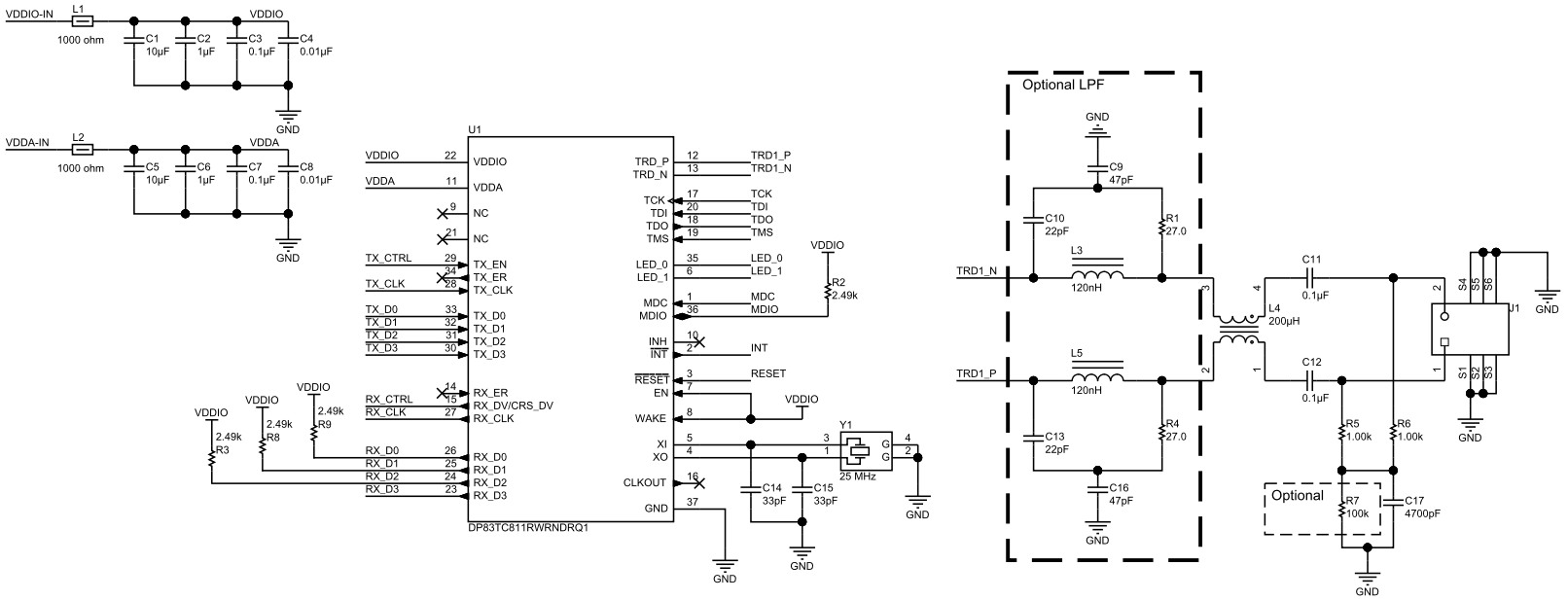

Figure 5. RGMII RX Shift Schematic

4.3 RGMII TX Shift Reference Design

In this design, skew is introduced between the RGMII TX_CLK and TX_data by the DP83TC811. The required delay between the RX_CLK and RX_data must be implemented internal to the MAC, or done through PCB routing. External bootstraps have been added to allow for RGMII TX Shift configuration at power-up/reset. This reference design is configured for PMA Slave Mode since LED_0 (MS Strap) is pulled LOW internally by default.

Table 7. RGMII TX Shift Bootstrap Configuration

PIN	BOOTSTRAP TYPE	MODE	DESCRIPTION
RX_DV	PHY_ID[0] PHY_ID[2]	1	PHY Address = 0x00
RX_ER	PHY_ID[1] PHY_ID[3]	1	
RX_D0	MAC[0] TEST[0]	4	RGMII TX Shift Operation
RX_D1	MAC[1] TEST[1]	1	
RX_D2	MAC[2] TEST[2]	4	
LED_0	MS	1	Slave
LED_1	AUTO	1	Autonomous Operation

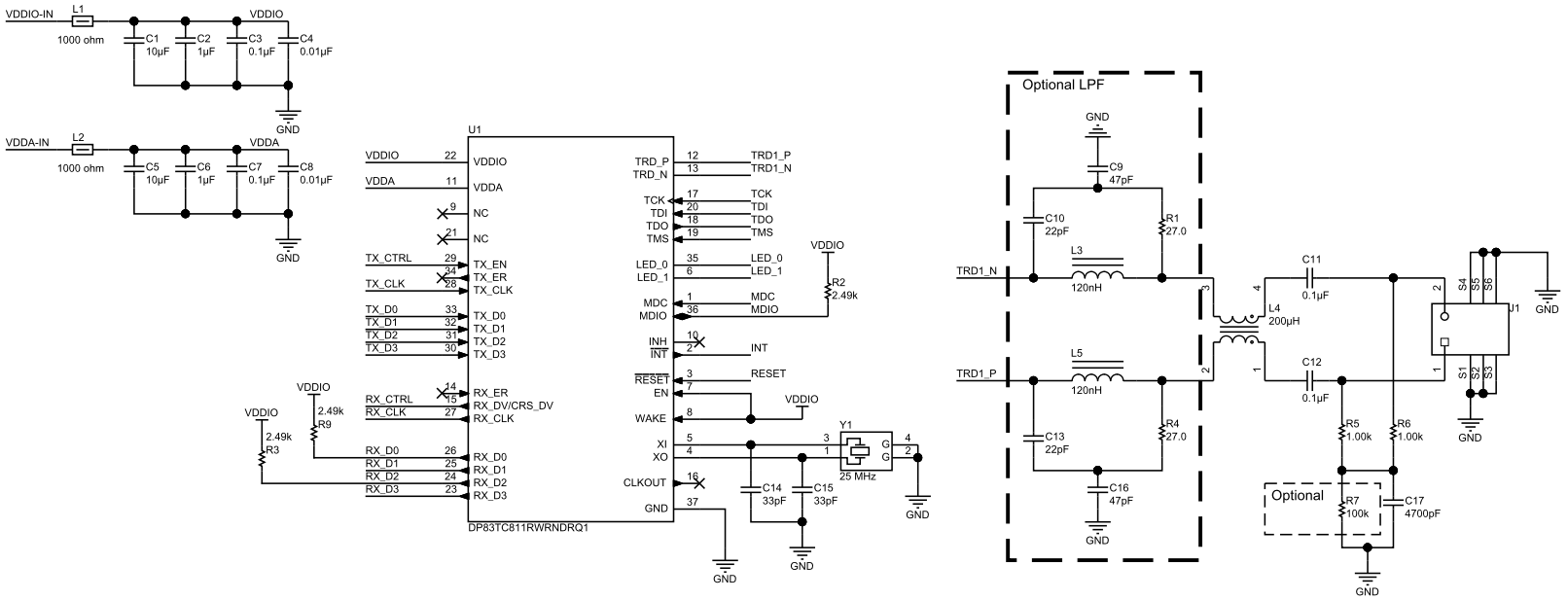

Figure 6. RGMII TX Shift Schematic

4.4 RGMII TX and RX Shift Reference Design

In this design, skew is introduced between the RGMII TX_CLK and TX_data, as well as the RX_CLK and RX_data, by the DP83TC811. No further delay should be implemented on PCB or in the MAC layer. External bootstraps have been added to allow for RGMII TX and RX Shift configuration at power-up/reset. This reference design is configured for PMA Slave Mode since LED_0 (MS Strap) is pulled LOW internally by default.

Table 8. RGMII TX and RX Shift Bootstrap Configuration

PIN	BOOTSTRAP TYPE	MODE	DESCRIPTION
RX_DV	PHY_ID[0] PHY_ID[2]	1	PHY Address = 0x00
RX_ER	PHY_ID[1] PHY_ID[3]	1	
RX_D0	MAC[0] TEST[0]	1	RGMII TX and RX Shift Operation
RX_D1	MAC[1] TEST[1]	4	
RX_D2	MAC[2] TEST[2]	4	
LED_0	MS	1	Slave
LED_1	AUTO	1	Autonomous Operation

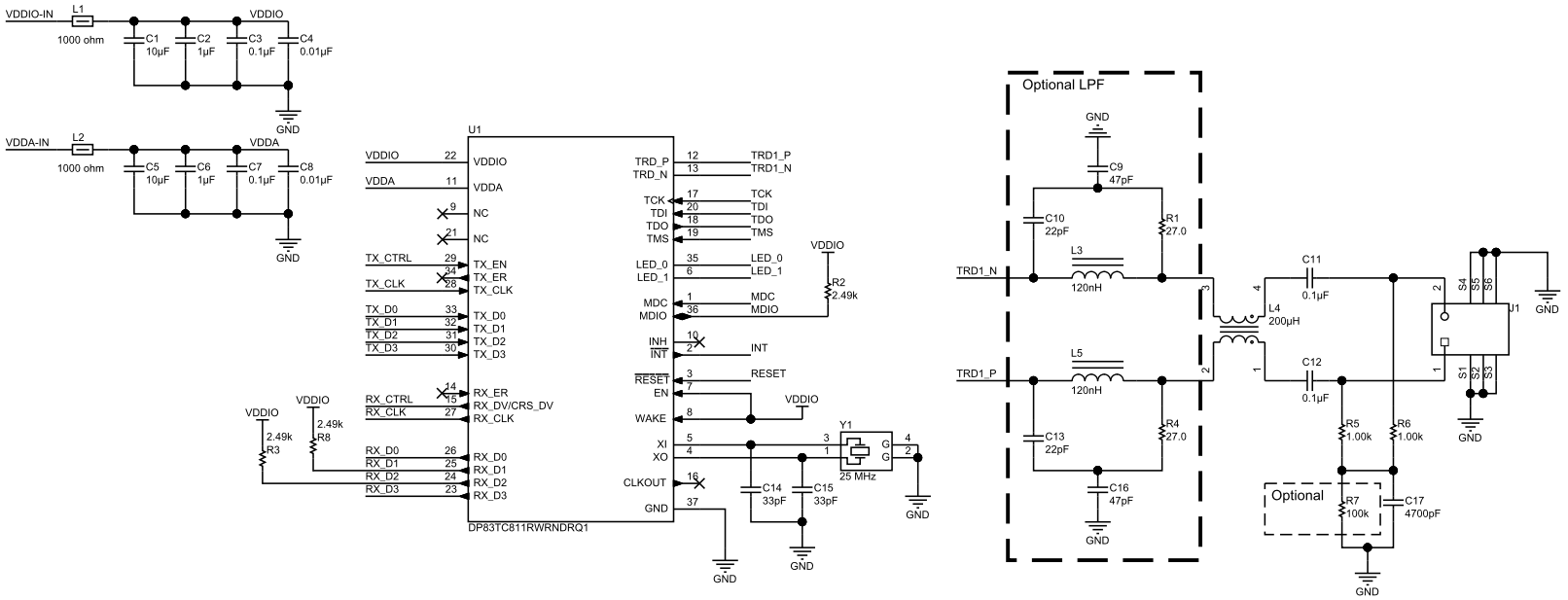

Figure 7. RGMII TX and RX Shift Schematic

4.5 RGMII Digital Pin Routing

The DP83TC811 is a fixed 100Mbps device. Since RGMII is a 1Gbps rated interface, RX_CLK and TX_CLK will always operate at 25MHz for this device; TX_CLK is provided by the attached MAC. Additionally, when in 100Mbps, DDR operation is disabled and thus data is only latched-in on the rising edge of the reference clock.

When operating in Align mode, no internal delay on either transmit or receive path is enabled within the DP83TC811. Delay between clock and data must be provided by either the MAC internal delay or through trace delay routing.

When operating in RX shift mode, the receive clock (RX_CLK) is delayed by 3.5ns with respect to the data pins (RX_D[3:0], RX_DV and RX_ER). The transmit path will remain in align mode and thus the MAC internal delay or trace delay routing are required to establish the proper setup and hold.

When operating in TX shift mode, the transmit clock (TX_CLK) is delayed by 3.5ns with respect to the data pins (TX_D[3:0], TX_EN and TX_ER). The receive path will remain in align mode and thus the MAC internal delay or trace delay routing are required to establish the proper delay.

When operating in TX and RX shift mode, the receive clock (RX_CLK) is delayed by 3.5ns with respect to the data pins (RX_D[3:0], RX_DV and RX_ER). Additionally, the transmit clock (TX_CLK) is delayed by 3.5ns with respect to the data pins (TX_D[3:0], TX_EN and TX_ER). Depending on setup and hold requirements of the MAC, additional trace delay routing or MAC internal delay might not be necessary.

DP83TC811 allows for a minimum setup time of 1ns and hold time of 1ns.

Note: Digital pin groupings that should be length match in relation to each other. TX_CLK and RX_CLK are not included in the groups because these will need to be delayed in order to establish the proper setup and hold.

- Group #1 (Receive Path)
  - RX_CLK, RX_D[3:0], RX_CTRL
- Group #2 (Transmit Path)
  - TX_CLK, TX_D[3:0], TX_CTRL
- Group #3 (SMI)
  - MDIO, MDC

Note: All group members should be routed with 50 Ω impedance to ground.

Note: When a pin is not used, it may be left unconnected (floating). Each digital pin has either an internal pull-up or pull-down. For additional pin pull-up and pull-down description, please see the DP83TC811 datasheet.

5 SGMII Reference Designs

This section provides recommended schematics for connection to an SGMII MAC interface: 4-wire and 6-wire configurations. For SGMII, DC blocking capacitors are required. Ceramic 0.1µF capacitors are recommended for the required isolation.

5.1 SGMII 4-Wire Reference Design

External bootstraps are not necessary for SGMII 4-wire configuration. Internal pull-down resistors will configure the PHY for 4-wire SGMII at power-up/reset. This reference design is configured for PMA Slave Mode since LED_0 (MS Strap) is pulled LOW internally by default.

Table 9. SGMII 4-Wire Bootstrap Configuration

PIN	BOOTSTRAP TYPE	MODE	DESCRIPTION
RX_DV	PHY_ID[0] PHY_ID[2]	1	PHY Address = 0x00
RX_ER	PHY_ID[1] PHY_ID[3]	1	

Table 9. SGMII 4-Wire Bootstrap Configuration (continued)

PIN	BOOTSTRAP TYPE	MODE	DESCRIPTION
RX_D0	MAC[0] TEST[0]	1	SGMII 4-Wire Operation
RX_D1	MAC[1] TEST[1]	1	
RX_D2	MAC[2] TEST[2]	1	
LED_0	MS	1	Slave
LED_1	AUTO	1	Autonomous Operation

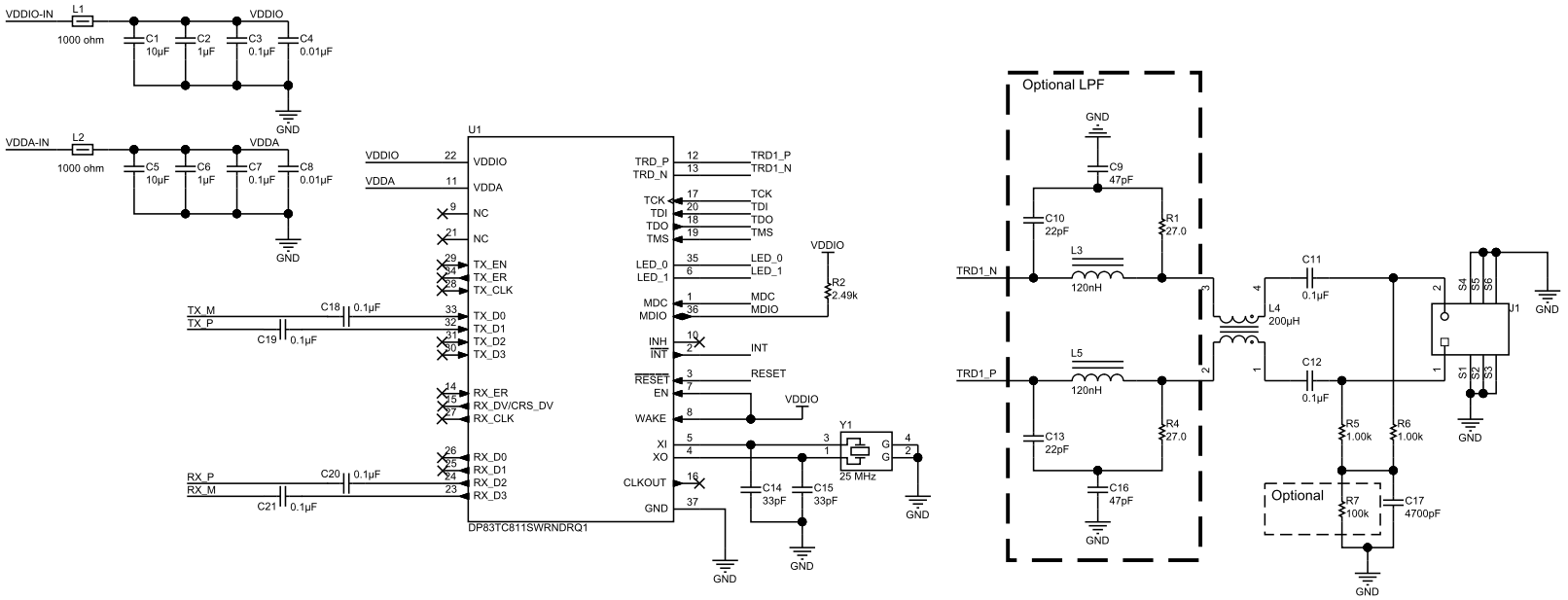

Figure 8. SGMII 4-Wire Schematic

5.2 SGMII 6-Wire Reference Design

6-wire SGMII operation includes an optional 625 MHz clock, synchronous to RX data, provided to the MAC. This extra clock is for use by MACs that do not implement clock recovery from the data.

This reference design is configured for PMA Slave Mode since LED_0 (MS Strap) is pulled LOW internally by default

Note: Register configuration is required to enter into 6-wire operation. Upon power-up/reset, the device will enter into 4-wire operation.

Table 10. SGMII 4-Wire Bootstrap Configuration

PIN	BOOTSTRAP TYPE	MODE	DESCRIPTION
RX_DV	PHY_ID[0] PHY_ID[2]	1	PHY Address = 0x00
RX_ER	PHY_ID[1] PHY_ID[3]	1	
RX_D0	MAC[0] TEST[0]	1	SGMII 4-Wire Operation
RX_D1	MAC[1] TEST[1]	1	
RX_D2	MAC[2] TEST[2]	1	
LED_0	MS	1	Slave
LED_1	AUTO	1	Autonomous Operation

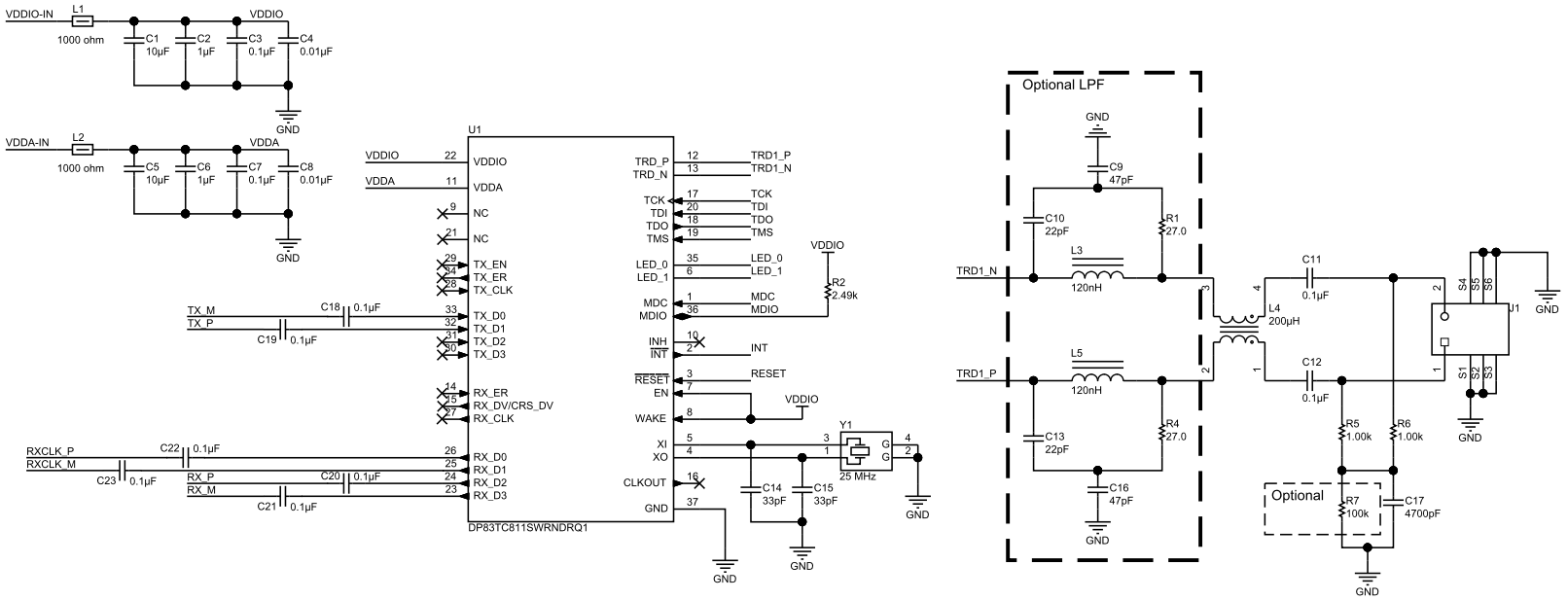

Figure 9. SGMII 6-Wire Schematic

6 PMA Recommendations

The DP83TC811 is designed with integrated filtering to reduce external passive components and thus reduce BOM cost. below provides a low cost and low component count solution for the PMA.

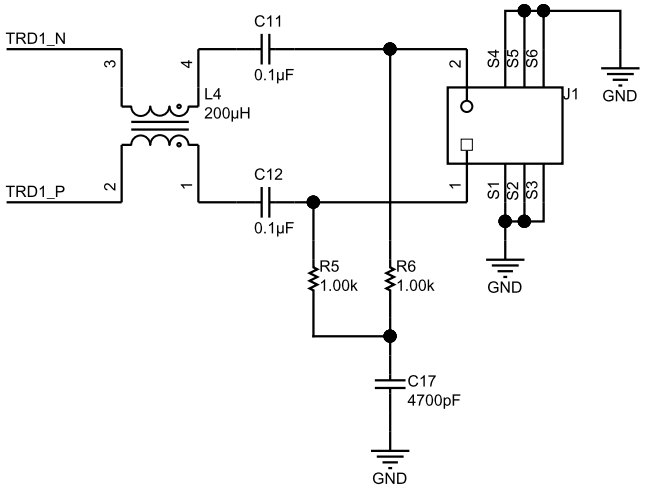

Figure 10. PMA Schematic

Note:TRD_N and TRD_P must be routed with 100 Ω differential impedance control.

To reduce common mode noise and improve both return loss and mode conversion, the following components and associated values are recommended.

Table 11. PMA Component Requirements

COMPONENT	VALUE	TOLERANCE	RATING
DC Blocking Capacitor (C11, C12)	0.1 µF	+/-10%	50 V
CM Termination (R5, R6)	1 kΩ	+/-1%	0.75 W
ESD Shunt (R7)	100 kΩ	+/-5%	0.125 W
CM Coupling Capacitor (C17)	4.7 nF	+/-10%	2 kV

A 100kΩ shunt resistor may optionally be placed in parallel with the 4.7nF de-coupling capacitor to provide a current return path for ESD events, shown in below.

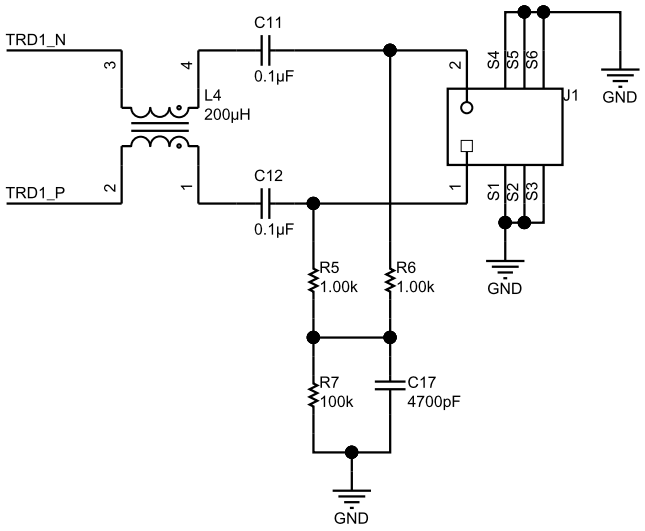

Figure 11. PMA Schematic with ESD Shunt

6.1 CMC Recommendations

The following CMCs have been evaluated with the DP83TC811 using the DP83TC811EVM:

Table 12. CMC Recommendations

PART NUMBER	MANUFACTURER	CM TERMINATION RECOMMENDATION
AE2002	Pulse Electronics	1.5 kΩ
ACT45L-201	TDK	2 kΩ
ACT1210L-201		
DLW43MH	Murata	1 kΩ

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