Application Report

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DP83TC811 Diagnostic Toolkit

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ABSTRACT

In-field failures can not only cripple electronic control units (ECU) but can render an automobile immobile. ECUs must be able to detect failures and even predict failures, allowing for service professionals to address potential problems before they result in a complete failure. The DP83TC811 Ethernet physical layer transceiver (PHY) provides advanced tools to predict and detect faults. This application note will discuss the built-in diagnostic tools in the DP83TC811, how to configure the tools, and how to interpret the results.

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1 Introduction

The DP83TC811 Automotive Ethernet PHY is IEEE 802.3bw compliant, 100BASE-T1. The DP83TC811's Diagnostic Tool Kit provides system designers detailed information to assist in both in-system use as well as system debug/bring-up.

There are seven main diagnostic tools within the DP83TC811:

- Real-time SNR monitor
- Time Domain Reflectometer (TDR)
- Voltage sensor
- Temperature sensor
- ElectroStatic Discharge (ESD) sensors
- Pseudo-Random Binary Sequence (PRBS) generator and checker
- Datapath loopback modes

The following sections will discuss each of these diagnostic tools, except for PRBS or loopback modes. Each section discusses the relevance of the tool in the automotive context and the registers that are used to configure the tool and retrieve data. Example scripts are also provided that can be used with TI's USB-2-MDIO software tool that is used with the MSP430 LaunchPad to communicate with the DP83TC811 through the MDIO serial management interface. The USB-2-MDIO software can be found in the DP83TC811 product folder on ti.com. For information regarding the PRBS and loopback modes, please see our DP83TC811 Compliance and Debug application note.

In the following sections, register access examples use the following conventions:

- For a register write: <address> <value>
- For a register read: <address>

These conventions are based on TI's USB2MDIO graphical user interface that supports the DP83TC811. This tool simplifies register access by automating the actual register access protocol. For users that are developing custom firmware for the DP83TC811, please refer to the programming section of the data sheet for the specific protocol requirements.

Table 1. Terminology

Acronym	Definition
DUT	Device Under Test
LP	Link Partner
ESD	Electrostatic Discharge
SMI	Serial Management Interface
PCS	Physical Coding Sublayer
PMA	Physical medium attachment
PHY	Physical layer transceiver
SQI	Signal Quality Indicator
SNR	Signal to Noise Ratio
SQS	Signal Quality Status
TDR	Time-Domain Reflectometry
MII	Media Independent Interface
MDI	Medium Dependent Interface

2 Real-Time SNR Monitor

2.1 Application Need

A physical link between nodes in automotive Ethernet uses unshielded twisted pair cable. Cable quality, connector contact and PHY operational state all contribute to the health of a link. Each of these components represents an opportunity for a failure mode. It is essential that these failure modes be accounted for and/or predicted. The DP83TC811 includes a real-time SNR monitoring tool. It provides an ECU with a way to determine link quality between a PHY and link partner (LP). During normal vehicle lifecycle, the SNR monitor provides a way to see the degradation of cable quality and connector contact, allowing a service provider to identify any links needing additional servicing prior to release.

Trends over the lifetime of a vehicle may also be tracked if the SNR value is recorded at discrete points. For example, slow degradation of a connector when it is exposed to water may show a slow 1 dB/year decline.

Qualification tests like BCI and vehicle level testing purposely induce noise and other stresses into the system. The SNR monitor provides a system designer a way to see the effects of these external stresses on a link. SNR can also be used to evaluate BER margin remaining when testing channel immunity to interfering signals.

2.2 Configuration Procedure

When the DP83TC811 has an active link, the SNR tool autonomously monitors link quality on a periodic basis. The SNR readout is found in the Signal-to-Noise Ratio Results Register (SNR, register 0x0197, bits [8:0]). It is a 9-bit value that uses units of dB with a tenth dB resolution (xx.x dB). Additionally, the DP83TC811 provides a 0 to 100 interpretation of the SNR called signal quality indication (SQI). This SQI value is also mapped to a 2-bit signal quality status (SQS) flag, which quickly identifies if a link is excellent, good, poor or lost. SQI and SQS are located in the Signal Quality Indication Register (SQIR, register 0x0198, bits [7:0] and [9:8], respectively). These signal quality monitoring functions run autonomously and do not require any configuration.

Below is a script for reading the SQI, SNR, and SQS monitor that can be used with TI's USB2MDIO tool:

```
begin
//read SQI and SQS registers
0198
//read SNR register
0197
end
```

2.3 Analysis

To convert the SNR readout (register 0x0197, bits [8:0]) from hexadecimal to dB, follow these steps:

1. Convert SNR hexadecimal readout to decimal
2. Divide decimal by 10
3. Result is in dB

SQI can be directly converted into decimal form from the hexadecimal readout. It is important to note that SNR, SQI and SQS are all real-time monitors valid only during an active link. There is no storage of the values and the fields are updated each scan cycle, which is every 15.7 ms.

3 Time-Domain Reflectometry

3.1 Application Need

The IEEE 802.3bw clause 96 definition of the 100BASE-T1 PMA requires a PHY to tolerate open and short circuit conditions without suffering damage, up to a certain electric potential. The Open Alliance specification takes this a step further and mandates the open and short conditions be detected by a 100BASE-T1 PHY and reported to the system. The DP83TC811's TDR function detects open and short conditions on the Medium Dependent Interface (MDI) , and also indicates the distance to the fault in the cabling.

Note: TDR *cannot* be performed on an active link. The TDR function injects pulses into the channel and the reflected waves are measured to determine fault type and location. Active links disrupt the pulse as well as impede the receiver, corrupting the measurement.

3.2 Configuration Procedure

TDR operation is enabled in the Time Domain Reflectometry Register (TDR, register 0x001E). The DP83TC811 also implements a TDR auto-run feature, found in register 0x0009. When TDR auto-run is enabled, the PHY will automatically preform a TDR measurement and record the results when an active link is dropped for any reason. If the system has deliberately torn down the link, the TDR results can be ignored.

Below is a script for running the TDR on demand.

```
begin
//start TDR single run
001E 8000
end
```

Below is a script for configuring the TDR to auto-run when the link goes down.

```
begin
//enable TDR auto-run
0009 0100
end
```

Below is a script for reading the results of the TDR operation.

```
begin
//TDR status register
001E
//TDR fault type and location
016B
end
```

3.3 Analysis

Note that starting the TDR measurement and checking its status involves writing and reading register 0x001E. The status returned indicates the state of the measurement (bit[1]: 1 = complete, 0 = in progress), and integrity of the measurement (bit[0]: 1 = measurement failure, 0 = valid measurement). After the successful execution of TDR, the results are stored in the TDR Results Register (TDRR, register 0x016B). Fault status, fault type and fault location are all stored in this register. Bit[9] indicates fault status (1 = fault detected, 0 = no fault). Bit [8] indicates OPEN (0) or SHORT(1), and Bits[7:0] indicate fault location in meters. To locate the fault, bits[7:0] must be converted to decimal form and then multiplied by 1.5.

4 Voltage Monitor

4.1 Application Need

Current draw of a PHY changes during a normal operational profile. Current draw spikes can occur when channel utilization rates change and temperature fluctuates. Supply rails must be able to provide voltage levels within the recommended operating conditions of the PHY during these spikes of current consumption to ensure proper function. The DP83TC811 includes a voltage monitor on both the IO supply rail (VDDIO) and core supply rail (VDDA). These monitors periodically sample the voltage and update the readout field within the PHY's register map. System designers can also enable an undervoltage or overvoltage interrupt that will indicate the voltage rail has exceeded the upper or lower operational limits of the DP83TC811. This level of visibility is useful because it helps eliminate the need for additional external monitors, scaling back on total system solution size, complexity and cost.

4.2 Configuration Procedure

When enabled, voltage monitoring is always active during normal PHY operation, and runs periodically. By default, the voltage monitor cycle time is 32 ms. Cycle time can be adjusted in the range of 16 ms to 240 ms using the Monitor Configuration Register #1 (MON_CFG1, register 0x0480). Bits[3:0], when set to 0b1111 result in a 240 ms cycle while a 0b0001 results in a 16 ms cycle time. 0b0000 is not a valid cycle time setting. Additionally, period monitoring can be disabled using Monitor Configuration Register #2 (MON_CFG2, register 0x481).

Below is a script for configuring the cycle time of the voltage monitor, and reading the result of the monitor.

```
begin
//set monitor cycle time to 144ms
0480 1001
//pause 144ms or greater to allow at least one cycle to complete
//readout voltage monitor
0484
end
```

4.3 Analysis

Voltage monitoring results are located in Monitor Status Register #2 (MON_STAT2, register 0x0484). Because periodic monitoring is enabled by default and set to 32 ms, the value within register 0x0484 will be updated accordingly. The monitor provides an independent readout range for both VDDIO and VDDA. There are eight discrete ranges covering the entire recommended operating voltage range of the DP83TC811.

Overvoltage and undervoltage interrupts may be enabled using the Interrupt Status Register #2 (INT_STAT2, register 0x0013). Additionally, Monitor Configuration Register #3 (MON_CFG3, register 0x0482) controls the overvoltage and undervoltage thresholds.

Below is a script for configuring the voltage monitor threshold trigger and configuring an interrupt to be generated when the trigger occurs.

```
begin
//enable undervoltage and overvoltage interrupt
0013 00C0
//set undervoltage threshold between +1.5% and +9% and overvoltage to > +9%
0482 1000
end
```

5 Temperature Monitor

5.1 Application Need

Not all ECUs include temperature control by passive ventilation, fan airflow or thermal heat sinks. Some active components will experience more significant temperature rise than others depending on the thermal characteristics of the packaging, solder contact, PCB layout, PCB material and component power consumption. Unintended thermal hotspots can occur. The DP83TC811 has a built-in temperature monitor that enables a system engineer to analyze the temperature level at the PHY and thus determine if it is within the target parameters.

5.2 Configuration Procedure

When enabled, periodic temperature monitoring is always active during normal PHY operation. By default, the temperature monitor cycle time is 32 ms. Cycle time can be adjusted in the range of 16 ms to 240 ms using the Monitor Configuration Register #1 (MON_CFG1, register 0x0480). Bits[3:0], of MON_CFG1, when set to 0b1111 result in a 240 ms cycle, while 0b0001 results in a 16 ms cycle time. 0b0000 is not a valid cycle time setting. Additionally, period monitoring can be disabled using Monitor Configuration Register #2 (MON_CFG2, register 0x0481).

Below is a script for configuring the cycle time of the temperature monitor, and reading the result of the monitor.

```
begin
//setting cycle time to 144ms
0480 1001
//pause 144ms or greater to allow cycle to complete
//readout temperature monitor
0483
end
```

5.3 Analysis

Temperature monitoring results are located in Monitor Status Register #1 (MON_STAT1, register 0x0483). Because periodic monitoring is enabled by default and set to 32 ms, the value within register 0x0483 will be updated accordingly. The monitor provides a temperature readout range and not an exact value. There are eight discrete ranges covering the entire recommended operating temperature range of the DP83TC811.

An overtemperature interrupt may be enabled using the Interrupt Status Register #2 (INT_STAT2, register 0x0013). If the temperature exceeds the overtemperature threshold, the INT pin will transition to indicate the condition occurred, which can be routed to a controller. This is useful in that it eliminates the need for firmware to continually read the monitor results while it is still within an acceptable temperature level determined by the implementer. Monitor Configuration Register #3 (MON_CFG3, register 0x0482) bits[3:0] control the overtemperature threshold.

Below is a script for configuring the temperature monitor threshold trigger and configuring an interrupt to be generated when the trigger occurs.

```
begin
//enable overtemperature interrupt
0013 0008
//set overtemperature threshold level between +70oC and +100oC
0482 0004
end
```

6 ESD Sensor

6.1 Application Need

Electrostatic discharge events are not predictable and they can cause serious system issues that include service disruption and even ECU damage. The common method to address ESD strikes is adding more suppression components and higher rated components. The drawback is that it increases cost, system complexity and solution size. Instead of using the maximum available suppression, the DP83TC811's integrated ESD sensor can be used during system development and qualification to provide the designer an understanding into where the energy is propagating to and how often. There are independent xMII and MDI ESD sensors within the DP83TC811. These sensors count the total number of ESD events on their respective pins during a power up period of the PHY.

The ESD sensor can also be used during normal vehicle operation. It can be used as a service tool to understand when and where ESD events are occurring. The tool includes an option to provide an interrupt to a connected controller when an ESD event is detected.

6.2 Configuration Procedure

There is no configuration needed for ESD sensing, the ESD sensor is always active. The sensor can only be cleared by device power-cycling.

Below is a script for reading out the results of the ESD sensor and configuring an interrupt to be generated when the sensor detects an ESD event.

```
begin
//readout ESD sensor
0448
//enable ESD interrupt
0012 0008
end
```

6.3 Analysis

ESD sensor results are located in Electrostatic Discharge Status Register (ESDS, register 0x0448). The xMII event counter is located in ESDS register bits[13:8] and the MDI event counter is located in bits[5:0].

An ESD interrupt may be enabled using the Interrupt Status Register #1 (INT_STAT1, register 0x0012). This is useful in that it eliminates the need for firmware to continually read the counter when there is no change.

7 Conclusion

ECUs are continuing to increase their monitoring capabilities as more complex systems are added to a vehicle ecosystem. The DP83TC811 provides an extensive diagnostic tool kit which addresses many of the potential faults an automotive Ethernet system could experience during its lifetime, enabling enhanced monitoring by the ECU. For additional information regarding the Diagnostic Tool Kit, please see the DP83TC811R-Q1 datasheet and the Diagnostic Tool Kit Demo.

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