Selection and specification of crystals for Texas Instruments ethernet physical layer transceivers

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ABSTRACT

To comply with the IEEE 802.3 standard, each Ethernet node must have a reference clock with accuracy of ±100 parts per million (ppm). For Texas Instruments Ethernet Physical Layer transceivers, TI recommends that the clock be derived from an external crystal. An accurate clock requires careful selection of the crystal as well as external loading capacitors. This application report describes details of crystal specifications, recommendations for loading capacitor selection, and board layout guidelines.

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1 Introduction

Texas Instruments' Ethernet Physical Layer (PHY) transceivers require an external 25-MHz clock source to provide the reference for the internal circuitry that generates all the clocks required by the device for data transmission and reception. TI PHYs support either an external crystal resonator connected across the XI and XO pins, or an external CMOS-level oscillator connected to XI pin only. TI recommends using a crystal as the clock source for low-cost system design.

The frequency generated by the external reference clock must have a total accuracy better than ±100 ppm for the PHY to function properly, per IEEE 802.3 requirements. This tolerance includes all sources of error associated with either the crystal or the supporting circuitry. Excessive variations in the reference clock can result in data corruption on Medium Dependent Interface (MDI) or Media Independent Interface (xMII). In this application note, we will examine definitions of crystal specifications, the sources of frequency error, tips for measuring crystal frequency, design guidelines, and layout recommendations.

2 Crystal Oscillator Model

A crystal-based oscillator is formed by placing a crystal in the feedback loop of an oscillator circuit that provides sufficient gain and phase shift around the loop to start and sustain stable oscillations. A detailed explanation of crystal oscillator operation will not be covered here. However, to support the reader's interpretation of the guidance and recommendations contained in this app note, some essential aspects of the crystal oscillator circuit model are presented and explained here.

A simple model of a crystal is shown in Figure 1. It has R-L-C series components, called motional resistance, motional capacitance, and motional inductance. The capacitor in parallel, C0, is called the shunt capacitance, and models the package capacitance. Figure 2 illustrates a simple oscillator model, consisting of an inverting amplifier and crystal, and its equivalent circuit model.

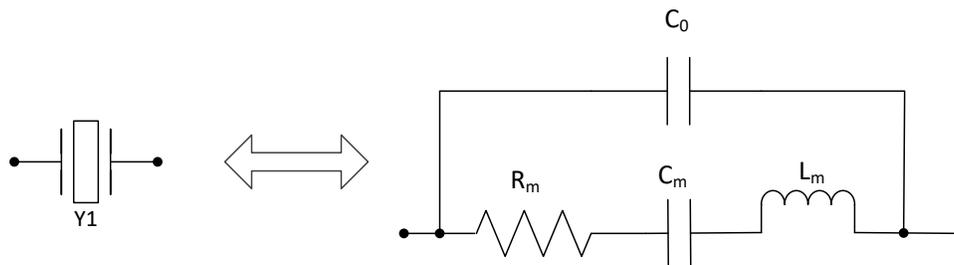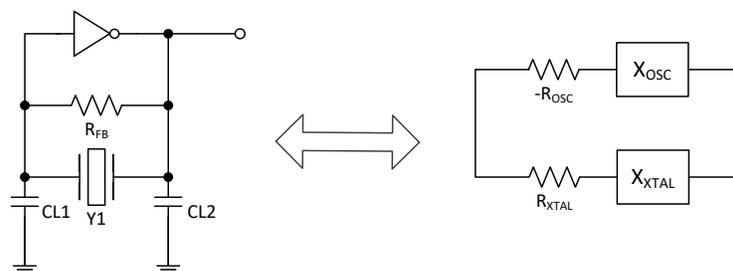**Figure 1. Crystal Model**

Figure 2. Crystal Oscillator Model

The circuit model in Figure 2 is useful for understanding the necessary conditions for oscillation. These are:

$$X_{XTAL} + X_{OSC} = 0$$

$$R_{XTAL} + R_{OSC} = 0$$

Where:

X_{XTAL} = the imaginary part of the impedance represented by the crystal.

R_{XTAL} = the real part of the impedance represented by the crystal.

X_{OSC} = the imaginary part of the impedance represented by the oscillator.

R_{OSC} = the real part of the impedance represented by the oscillator.

Mathematically, R_{OSC} is a negative resistance. It represents a circuit that supplies power rather than dissipating power, e.g., an amplifier. Consequently, a simple interpretation is that the amplifier must have enough gain to compensate for the losses represented by the crystal. The concept of negative resistance is important to crystal oscillator design and will be revisited later in this app note.

3   Crystal Specifications

3.1   Crystal Frequency

TI PHYs use a standard crystal frequency of 25MHz. This is a common frequency and is readily available in automotive versions, covering a variety of package types and sizes.

> **NOTE:**   Some TI PHYs support RMII Slave operation that requires a 50-MHz CMOS-level oscillator connected to the XI pin with the XO pin floating.

3.2   Crystal Oscillation Mode

The oscillation mode of operation for the crystal must be specified as fundamental mode. Some crystals operate in overtone mode to achieve higher frequencies, typically above 30 MHz. This is because as frequency increases, the size of the crystal needed to operate in fundamental mode decreases, and at some point becomes more difficult to handle during the manufacturing process. So, fundamental mode crystals at high frequencies are more expensive.

3.3   Crystal Circuit Type

The selected crystal must operate in parallel resonance mode to be compatible with TI's PHYs. A parallel resonant crystal is designed to operate with a specified load capacitance in the oscillator feedback loop. A parallel mode crystal is the same as a series mode crystal, but operates in a different region on its frequency vs. impedance curve.

3.4   Frequency Tolerance

Frequency tolerance is the initial maximum deviation from the nominal crystal frequency at a specified temperature, usually 25°C. This tolerance specification accounts for normal variations in the crystal fabrication and assembly. Many crystal vendors offer a fixed selection of tolerance values when ordering a crystal. For example, the set of orderable values may be +/- 20 ppm, +/- 50 ppm, and +/- 100 ppm.

3.5   Frequency Stability

Frequency stability refers to the maximum deviation from nominal crystal frequency over a specified temperature range. This deviation is measured with reference to the nominal frequency at 25°C. The crystal vendor may also offer a range of values to choose from when ordering the crystal. For example, common ranges may include +/- 50ppm, and +/- 100ppm over a specified temperature range. For automotive crystals specified to operate over a temperature range of -40C to +125C, with +/- 50 ppm, the deviation per degree C is 1.64 ppm.

3.6 Aging (Long-Term Stability)

Aging refers to the cumulative change in frequency of oscillation experienced by a crystal over time. There are many causes of crystal aging, including excessive drive level, various thermal effects, and stress relief or buildup on the mechanical structures. Aging is typically specified in units of ppm per year. Typical values for long term stability may range between ±3 ppm to ±5 ppm per year.

3.7 Load Capacitance

Load capacitance refers to total capacitance in the oscillator feedback loop. It is equal to the amount of capacitance seen between the crystal terminals. For parallel resonant mode circuit, the correct load capacitance is necessary to ensure the oscillation frequency of the crystal is within the expected range. Figure 3 illustrates a typical crystal oscillator circuit and sources of load capacitance. The total load capacitance includes discrete load capacitors (C_{L1} and C_{L2}) , device pin capacitance and stray board capacitance. It is important to account for all sources of capacitance when calculating value for the discrete capacitor components, C_{L1} and C_{L2}, in Equation 1 for a specific board design.
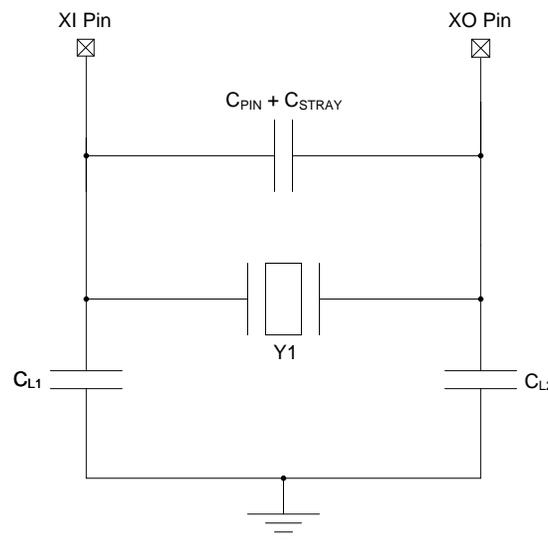
XI Pin   XO Pin

$C_{PIN} + C_{STRAY}$

Y1

C_{L1} C_{L2}

Figure 3. Simplified Crystal Equivalent Load Capacitance Circuit

$$C_{Load} = (C_{L1} \times C_{L2}) / (C_{L1} + C_{L2}) + C_{PIN} + C_{STRAY}$$

(1)

where

- C_{PIN} is the capacitance of the XI and XO pins of the integrated circuit and its packaging. Most PHY data sheets will specify the pin capacitance. For example, the capacitance of the XI and XO pins of the DP83TC811R-Q1 is 1 pF for each pin.
- C_{STRAY} is the stray capacitance of the printed-circuit board (PCB) traces connected to the crystal terminals.
- C_{L1} and C_{L2} are the discrete load capacitors. C_{L1} and C_{L2} must be selected to make the total load capacitance seen by crystal circuit close to the load capacitance specified by the crystal manufacturer.

Typically, $C_{PIN} + C_{STRAY}$ ranges from 2 pF to 5 pF, depending on the board layout design. By placing the crystal as close as possible to the XI/XO pins of the PHY, thereby achieving short traces, the stray capacitance can be minimized.

In most cases, $C_{L1} = C_{L2}$. In this case, the equation for C_{LOAD} simplifies to:

$C_{LOAD} = C_{L1}/2 + C_{PIN} + C_{STRAY}$

Consequently, designing the circuit in Figure 3, is a two-step process:

1. Determine C_{PIN} and C_{STRAY}

2. Calculate the values of $C_{L1} = C_{L2} = 2*(C_{LOAD} - C_{PIN} - C_{STRAY})$

If the actual load capacitance is less than that specified by the crystal specification, the oscillation frequency of the crystal will increase. If the actual load capacitance is greater than that specified by the crystal specification, the oscillation frequency of the crystal will decrease. However, the variation in load capacitance is typically the smallest source of error in the oscillator frequency when compared to frequency tolerance, stability and aging. For example, a +/- 10% variation in C_{LOAD} (= $C_{L1}/2$ +C_{PIN} + C_{STRAY}) would contribute less than +/- 8 ppm deviation in the oscillator frequency for a specified C_{LOAD} = 18 pF, and nominal C_{L1} = C_{L2} = 30 pF, C_{PIN} = 1 pF, and C_{STRAY} = 2 pF.

3.8 Equivalent Series Resistance

Equivalent Series Resistance (ESR) is the resistance the crystal exhibits at the series resonant frequency. ESR must not be confused with motional resistance (R_M) of the crystal equivalent circuit. ESR is related to R_M by the following equation:

$$ESR = R_M * (1 + C_0/C_L)^2$$

ESR is typically specified as a maximum resistance value in ohms. ESR is significant for two reasons:

1. Is proportional to the loop gain needed for the oscillator to start up and sustain oscillation.

2. It is proportional to the power dissipated in the crystal, also called drive level. This will be covered in the next sub-section.

In section 2 the concept of negative resistance was introduced, and described as the amount of power that must be supplied by the oscillator to compensate for the losses in the crystal. Its value is given by:

$$R_{NEG} = \frac{-g_M}{\omega^2 * C_{L1} * C_{L2}}$$

(2)

Where:

g_M = the transconductance of the small signal model of the MOS transistors used to form the amplifier.

(omega symbol) = resonant frequency of the oscillator.

C_{L1} = C_{L2} = the load capacitors from Figure 3.

The general rule of thumb is that the magnitude of the negative resistance of the oscillator must be ≥ 5*ESR to ensure that the circuit will start up and sustain oscillation. In other words:

|RNEG | ≥ 5 * ESR

Note that R_{NEG} is inversely proportional to the load capacitance. As load capacitance increases, R_{NEG} decreases, that is, the oscillator's ability to overcome the crystal losses and reach stable oscillation is degraded. The conclusion to be drawn is that the load capacitance and ESR of the crystal selected for use with any of TI's DP83xxx PHYs must be carefully chosen to meet the criteria above. The graph in Figure 4 illustrates the value of negative resistance for TI's DP83xxx Ethernet PHY oscillator circuits corresponding to a range of load capacitance, for temperatures of 125C and 85C. On the same graph is plotted a set of horizontal lines that represent various values of crystal ESR, with a 5x multiplier. For any given ESR value, the intersection point between its representative line and the R_{NEG} curves represents the maximum recommended load capacitance for a crystal with that ESR value. For example, a crystal with an ESR of 30 ohms must use a load capacitance of no larger than approximately 19 pF if the expected worst case operating temperature is 125C. Any higher load capacitance would cause the negative resistance to fall below the recommended 5x margin.
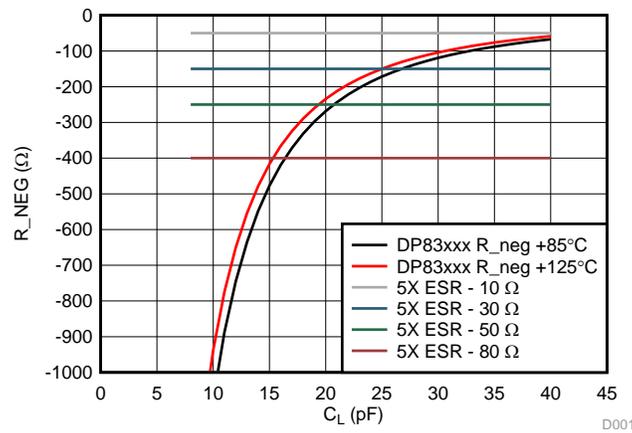
Figure 4. Negative Resistance vs Capacitive Load

3.9 *Crystal Drive Level*

Crystal drive level represents the power that is dissipated by the crystal. The maximum acceptable value will appear on the crystal data sheet. Exceeding the maximum drive level of the crystal can cause degraded performance and shorten the crystal's operating life. TI's DP83xxx PHYs can work with crystals that have a maximum drive level as low as 100 µW. It is recommended that a series resistor, R_S, be inserted in the circuit, as shown in Figure 5. The combination of R_S and C_{L2} becomes a voltage divider, such that the amplitude of the voltage at the input to the crystal is reduced. A starting value for R_S can be found using the following equation:

$$\left| Z_{CL2} \right| = \left| \frac{1}{\omega * C_{L2}} \right|$$

(3)

This equation says that R_S must be set equal to the magnitude of the impedance of C_{L2} at the crystal resonant frequency, or, $R_S = |Z_{CL2}|$. For example, if C_{L2} = 16 pF, at a crystal frequency of 25 MHz, R_S = 398 ohms.
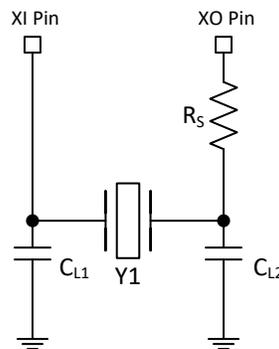

Figure 5. Crystal Oscillator Circuit With Series resistor

4   Crystal Selection Based On System Requirements And Crystal Specifications

Given that automotive Ethernet requires a total accuracy of +/- 100 ppm, selection of crystal specifications must be done to meet this total accuracy. Total accuracy is the sum of frequency tolerance, stability, aging, and component tolerance, all covered previously. In other words:

Accuracy = tolerance + stability + aging + component tolerance ≤ +/- 100 ppm.

Assume that the +/- 100 ppm requirement covers the temperature range of -40C to +125C, and the expected operating life of the host system is 5 years, with an aging spec of 3 ppm per year. Using the example from paragraph 2.7, assume that the error due to component tolerances is 8 ppm. The accuracy equation can then be rearranged to place a bound on the combined tolerance and stability:

100 – 8 – (5x3) = +/- 77 ppm for the sum tolerance + stability

+/- 77 ppm is the budget for tolerance and stability. As an example, to meet this budget, a crystal with tolerance = +/- 20 ppm, and a stability of +/- 50 ppm would be selected.

5   Layout Recommendations

The layout of the crystal circuit is important to ensure the correct oscillation frequency, minimize the noise introduced into the PLL, and reduce any emission from the circuit.

- The crystal and load capacitors must be placed as close as possible to the PHY XI and XO pins to minimize the trace length. Short traces help reduce parasitic inductance and stray capacitance and can decrease the amount of noise coupling.

- Avoid routing any other signal traces directly underneath the crystal or the XI and XO traces, and especially they must not run parallel with the clock traces. Keep all other signal traces away from the XI and XO traces. If signal routing under the crystal is required for the application, the use of a ground plane between the crystal circuit and other signal traces is required.

- Do not use the crystal output to drive any other device. The crystal oscillator is designed to drive the crystal in a direct feedback loop. Any extra branching or loading may affect the normal operation of the oscillator.
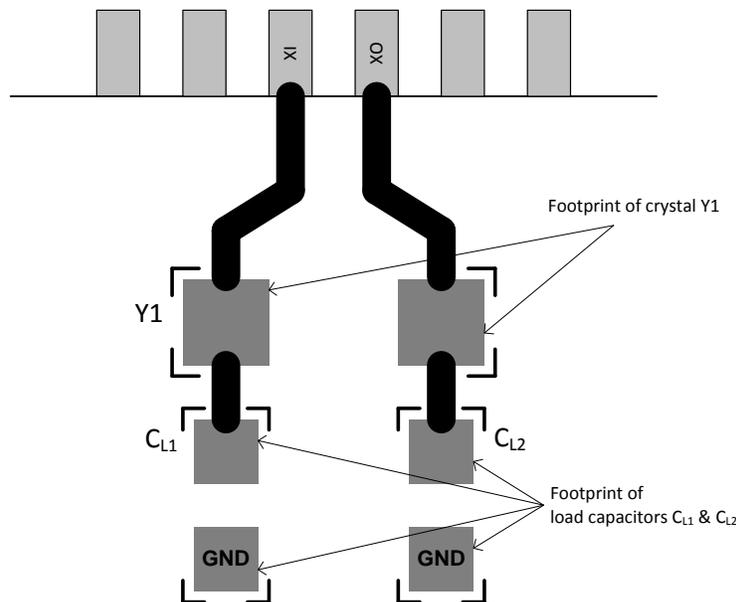

Figure 6. Crystal Circuit Layout

6   Common Problems and Tips

6.1   Measuring the Crystal frequency

*   The crystal frequency must not be measured directly with an oscilloscope because the measurement resolution is typically not sufficient calculate the frequency deviation to within a few ppm. A spectrum analyzer or frequency counter, with either using a stable 10 MHz reference, must be used to measure frequency.

*   Crystal frequency must not be measured by directly probing either the XI or XO pin. Loading these pins in any way may not only change the frequency, but can also stop an oscillating crystal. The frequency must always be measured by looking at a derived clock signal such as the CLKOUT pin. For example, on the DP83TC811-Q1, this is pin 16. One can also measure the frequency drift by using the IEEE test mode 2, which is a good representation of the local clock.

6.2   Load Capacitor Fine-Tuning

The discrete load capacitors C_{L1} and C_{L2} must be optimized for each new board design, as the layout for crystal circuit is different from board to board, which will primarily effect the C_{STRAY} value. The process described in Section 4 can be use to select the initial values for the discrete load capacitors. Once the circuit is assembled on the board, the actual crystal frequency must be measured. If the measured frequency is higher than expected or required, increase the value of the discrete load capacitance. Likewise, if the frequency is lower than required, decrease the discrete load capacitance.

6.3   Large Frequency Deviation

Sometimes the oscillator frequency is found to be at a very large deviation from the expected value. Small deviations are primarily fixed by fine tuning the load capacitance as discussed above. Large deviations are can be caused by accidental use of a non-fundamental mode crystal. These crystals operate at overtone frequencies, which is usually necessary to achieve higher frequencies. However, this is typically clear from a careful reading of the crystal data sheet, so selection of an overtone crystal is not likely.

7   Summary

Summary recommendations for crystal selection for TI Ethernet Physical Layer Devices:

*   Crystal frequency: 25 MHz
*   Crystal mode of operation: fundamental
*   Crystal circuit type: parallel resonance
*   Frequency tolerance at 25°C: ≤ ±50 ppm
*   Frequency stability over temperature: ≤ ±50 ppm
*   Aging (long-term stability): ≤ ±5 ppm per year
*   Load capacitance: 8 pF ≤ C_{LOAD} ≤ 20 pF
*   Maximum equivalent series resistance: ≤ 50 Ω

8   References

*   Selection and specification of crystal for Texas Instruments IEEE 1394 physical layers by Burke Henehan (SLLA051)
*   Abracon Manufacturer web page www.abracon.com
*   IEEE Standard 802.3-2012

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