

DP83TC811 IEEE 802.3bw Compliance and Debug

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ABSTRACT

The DP83TC811 is a 100BASE-T1 automotive Ethernet PHY designed to exceed the IEEE 802.3bw standard; however, board design variation and passive component selection can alter the MDI electrical characteristics. IEEE compliance is generally a top priority when verifying a new layout because it provides a quantitative representation for layout quality. IEEE compliance also helps ensure proper operation of the PHY when debugging board and system issues. This application report discusses how to configure the DP83TC811 device for various Ethernet compliance tests, identifies common system level mistakes, and presents solutions to those mistakes.

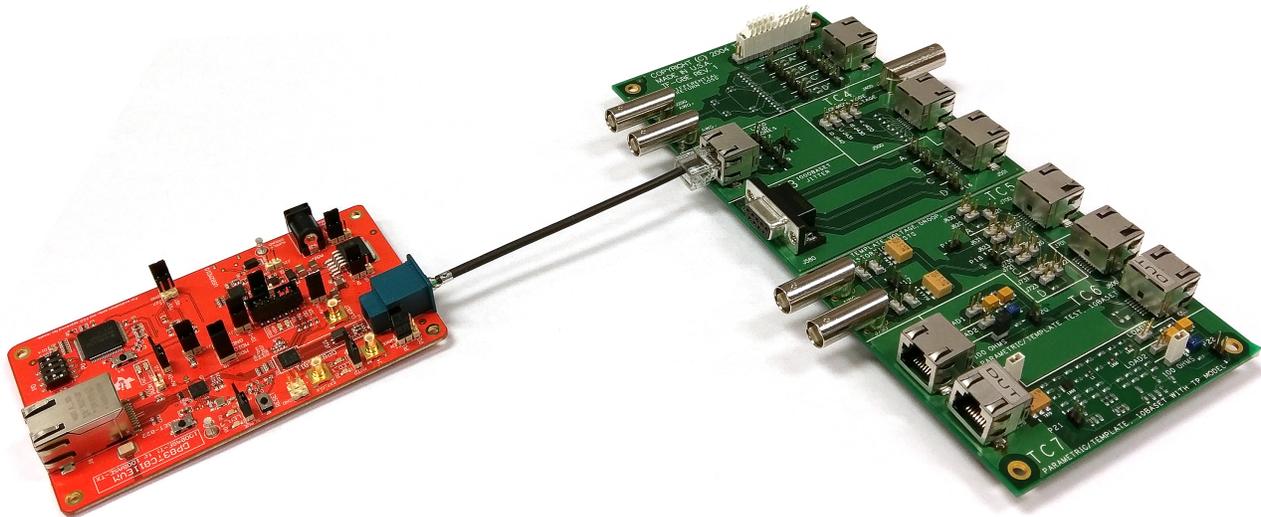


Figure 1. DP83TC811EVM Connected to a Test Fixture

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1 Introduction

The DP83TC811 automotive Ethernet PHY is IEEE 802.3bw compliant, 100BASE-T1. The device supports all the required test modes within the standard for assessing PHY compliance. Additionally, the device supports test mode configuration using hardware bootstraps. This serves as an alternative method if the SMI is not connected.

There are three main compliance aspects to the IEEE 802.3bw specification: PHY Control, PCS, and PMA. PHY Control and PCS are concerned with state machine flow and PCS operation within the PHY. These two fields do not require any special test mode, however, they do require specific test equipment. This application report does not discuss PHY Control and PCS testing. For information regarding those fields, visit the University of New Hampshire Interoperability Laboratory website ([UNH-IOL Test Suites](#)).

Table 1. Terminology

Acronym	Definition
SMI	Serial management interface
IPG	Interpacket gap
BIST	Built-in self-test
PCS	PHY control sublayer
PMA	Physical medium attachment
PHY	Physical layer transceiver
VNA	Vector network analyzer
MII	Media independent interface
MDI	Medium dependent interface
PSD	Power Spectral Density

2 Standards and System Requirements

2.1 Standards

The following standards serve as references for the tests described in this document:

- IEEE standard 802.3-2015
 - Amendment: IEEE standard 802.3bw-2015

2.2 Test Equipment Suppliers

The following test equipment suppliers are known to offer IEEE 802.3bw (100BASE-T1 and OPEN Alliance Broad-R Reach) compliance test equipment:

- Keysight
- Rohde and Schwarz
- Tektronix
- Teledyne LeCroy

2.3 Test Equipment Requirements

For this application note, the following hardware and software was used.

- > 1-GHz bandwidth oscilloscope
 - Tektronix BRR (100BASE-T1) PMA compliance software
 - > 1-GHz differential probe
 - Signal generator (for distortion testing)
 - TF-GBE-BTP or TF-BRR-CFD test fixtures
- 1 MHz to 1 GHz Vector-network analyzer
- TI USB-2-MDIO tool with PC (not required for testing)
 - [USB-2-MDIO download](#)
 - MSP430™ LaunchPad™ MSP-EXP430F5529LP (onboard EVM)
- Micro USB cable
- MatENET B-type – RJ45 connector
- 5 to 20 V DC power supply (if not using USB-based supply)

3 Physical Medium Attachment – Compliance Testing

3.1 Standard Test Setup and Procedures

For PMA compliance testing, the PHY is managed through SMI or hardware bootstraps to enable any of four test modes. Test results are determined and recorded by the Ethernet compliance software of the oscilloscope (for example, the 100BASE-T1 PMA compliance software from Tektronix).

When running through the PMA test modes, it may be necessary to change board connections and add external equipment. The following steps serve as a foundation for running through the test modes efficiently to minimize setup time and device configuration.

NOTE: If configuration through hardware bootstrap is desired, before starting Step 1, the EVM must be configured with the appropriate resistor bootstrap found in the DP83TC811 data sheet.

1. Connect the 5 to 20 V DC supply to the EVM through the barrel jack (or connect to the 5-V USB through the micro USB cable). For detailed power supply options, see the DP83TC811EVM User's Guide.
2. Connect the EVM to the test fixture according to the setup outlined in the test fixture/software manual, see [Figure 1](#).

NOTE: If using hardware bootstraps for test mode configuration, Step 4 can be skipped.

3. Configure the registers of the PHY for the specific test. The SMI can be managed through the MSP430 LaunchPad with the USB-2-MDIO tool from TI. Register configurations are outlined in [Appendix A](#). All test mode configuration scripts can be copied and used directly with the USB-2-MDIO tool.
4. Launch and configure the Ethernet testing software of the oscilloscope (see software user's manual).
5. Run the test and store the results (using the Ethernet compliance testing software).
6. Determine if the test passed or failed according to IEEE standards.
7. Change test parameters or EVM configuration and repeat.

3.2 Test Specifics and Pass Criterion

3.2.1 Transmitter Output Droop

Purpose: During data transmission, a long sequence of ones or zeros can cause baseline wander to occur. This test verifies that the PHY along with its connected DC blocking capacitors, common mode termination and common mode choke do not cause the transmitter output level to exceed the maximum specified limit (see [Equation 1](#) and [Equation 2](#)).

Pass Condition: Peak voltage (V_{pk}) and the voltage 500 ns after the peak (V_{delay}) difference does not exceed 45.0%.

$$V_d = V_{pk} - V_{delay} \quad (1)$$

$$\text{Droop} = (V_d / V_{pk}) * 100\% \quad (2)$$

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to test mode 1, found in [Appendix A](#). For this test mode, the PHY will output a repeating pattern of at least 40 +1 symbols followed by at least 40 –1 symbols continuously.

3.2.2 Transmitter Output Distortion

Purpose: To ensure that the transmitted waveform does not have significant overshoot or undershoot while it is in a defined symbol state of +1, 0 or -1.

Pass Condition: The transmitter waveform least mean squared error must be less than 15 mV. Least mean squared error is the peak error between the ideal reference and the observed symbols.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to test mode 4, found in [Appendix A](#). For this test, the EVM is configured to output the transmitter clock on LED_1 (J4, SMB connector) because a disturber signal is injected. The disturber must be frequency locked to the transmitter clock (TX_TCLK).

3.2.3 Transmitter Jitter

3.2.3.1 Transmitter MDI Master Jitter

Purpose: To ensure that the transmitter does not exceed the maximum jitter specification, enabling the receiver to recover the transmitted waveform and lock onto its scrambled serial stream.

Pass Condition: RMS TIE jitter shall be less than 50 ps over an integration time interval of at least 1 ms.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to test mode 2, found in [Appendix A](#). For this test mode, the PHY outputs a continuous 66.667-MHz signal.

3.2.3.2 Transmitter MDI Slave Jitter

Purpose: To ensure that the MDI Slave transmitter jitter is within the maximum specified limit, enabling the MDI Master receiver to recover the locked scrambled serial stream.

Pass Condition: RMS TIE jitter shall be less than 150 ps over an integration time interval of at least 1 ms.

Specific Test Setup: Configure PHY to slave mode, found in [Appendix A](#). For this test, the EVM is configured to output the transmitter clock on LED_1 (J4, SMB connector) because TX_TCLK must be measured by the test equipment. The EVM must be connected to a compliant 100BASE-T1 PHY operating in master mode.

3.2.4 Transmitter Power Spectral Density

Purpose: To ensure that the transmitter output power will provide enough margin over expected noise levels.

Pass Condition: When in test mode 5, the transmitter PSD shall be within the defined PSD mask (see [Appendix C](#)).

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to test mode 5, found in [Appendix A](#).

3.2.5 Transmitter Clock Frequency

Purpose: To ensure that the transmitter clock frequency is within the specified limits.

Pass Condition: The transmitter clock frequency shall be 66.667 MHz \pm 100 ppm.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to test mode 2, found in [Appendix A](#).

3.2.6 MDI Return Loss

Purpose: To ensure that the return loss measured at the MDI is within the specified limits.

Pass Condition: The return loss measured at the MDI shall:

$$RL(f) = \left\{ \begin{array}{l} 20 \text{ dB for } 1 \text{ MHz} \leq f \leq 30 \text{ MHz} \\ 20 - 20 \times \log_{10} \left(\frac{f}{30} \right) \text{ dB for } 30 \text{ MHz} \leq f \leq 66 \text{ MHz} \end{array} \right\} \quad (3)$$

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to slave mode, found in [Appendix A](#).

NOTE: A spectrum analyzer may be needed depending on Ethernet compliance software.

3.2.7 MDI Mode Conversion

Purpose: To ensure that the mode conversion measured at the MDI is within the specified limits.

Pass Condition: The return loss measured at the MDI shall:

$$TCL(f) = \left\{ \begin{array}{l} 60 \text{ dB for } 1 \text{ MHz} \leq f \leq 22 \text{ MHz} \\ 60 - \left(\frac{13}{\log_{10} \frac{100}{22}} \right) \times \log_{10} \left(\frac{f}{22} \right) \text{ dB for } 22 \text{ MHz} \leq f \leq 100 \text{ MHz} \\ 47 - \left(\frac{10}{\log_{10} \frac{200}{100}} \right) \times \log_{10} \left(\frac{f}{100} \right) \text{ dB for } 100 \text{ MHz} \leq f \leq 200 \text{ MHz} \end{array} \right\} \quad (4)$$

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to slave mode, found in [Appendix A](#).

NOTE: A spectrum analyzer may be needed depending on Ethernet compliance software.

3.2.8 Bit Error Rate Verification

Purpose: Verify that the DUT can maintain a BER less than 10^{-10} .

Pass Condition: No more than 7 errors are allowed in 3×10^{10} bits (equivalent to 2,470,356 frames of length 1518 bytes).

Specific Test Setup: Configure PHY to Reverse Loopback, found in [Appendix B](#). For a computer-based packet error-rate tester, see the DP83TC811EVM Demo Application Report.

4 Debug Test Methods

The DP83TC811 device includes various debug tools within the device to identify issues within a system or improper implementation of the device. The following subsections are ordered in the sequence that debug should proceed if operation is abnormal.

4.1 Common System Issues

This list serves as a common check to ensure that the DP83TC811 device is properly implemented:

- Are VDDA and VDDIO supply rails at their expected levels?
 - Is VDDA operating at 3.3 V +/-10%?
 - Is VDDIO operating at either 1.8 V, 2.5 V or 3.3 V +/-10%?
- Is the reference clock at the correct frequency?
 - If using a crystal, is the load capacitance properly selected?
- Does MDIO have a pull-up resistor as specified in the datasheet?
- Do the LED_0 and LED_1 pins have parallel pull-up or pull-down resistors in relation to the LED and current limiting resistor?
- Are RESET_N and EN pulled to a low state?
- Are bootstraps latching to the expected state?
 - Read Strap Latch-in register 1 (SOR1, address 0x467h)
- Are register settings being correctly executed?
 - Is the device configured properly as MDI Master or MDI Slave?
 - Is the device xMII configuration correct?
 - Are the registers in MMD1F, MMD1 or MMD3 and are you using the correct extended register access method as described in the datasheet?
- Are the xMII traces 50-Ω impedance controlled with reference to ground?
- Are the MDI traces 100-Ω impedance controlled to each other and 50-Ω with reference to ground?

4.2 Loopback Modes

There are four internal loopback paths within the DP83TC811. Each loopback serves a unique purpose in the debug process and system verification. The following subsections detail the most common loopback modes used and the possible case scenarios for why they may be implemented. For additional loopbacks, please reference the DP83TC811 datasheet.

4.2.1 xMII Loopback

xMII Loopback is the shallowest loop through the DP83TC811. When in xMII loopback, data transmitted from a connected MAC on the TX path is internally looped back in the DP83TC811 to the RX pins where it can be checked by the MAC. This loopback mode is enabled by setting bit [14] in the Basic Mode Control register (BMCR, address 0x0h).

Purpose: xMII Loopback is typically used to identify issues along the digital transmit and receive paths. This shallow loopback can isolate and help identify issues with routing errors, cut traces and unconnected pins.

Register Setting: See xMII Loopback in [Appendix B](#).

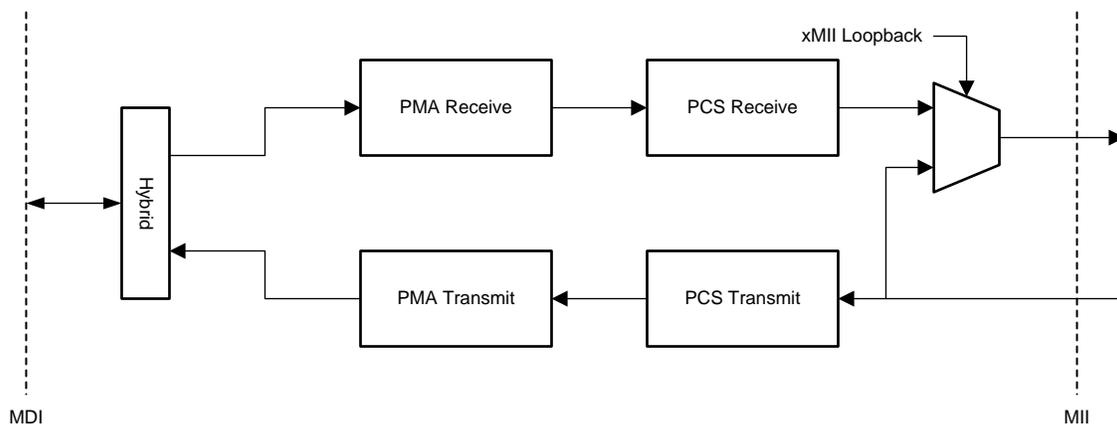


Figure 2. xMII Loopback

4.2.2 Reverse Loopback

Reverse Loopback is the deepest loopback within the DP83TC811 when looking into the PHY from the MDI. Data received on the MDI (TRD_P/M pins) is internally routed through all blocks within the receive path, where it is then routed back to the transmit block before being outputted on the xMII pins. The data is then transmitted back out on the MDI to the link partner. This loopback is enabled by setting bit [4] in the BIST Control register (BISCR, address 0x16h).

Purpose: Reverse Loopback is used to check the MDI when connected to a link partner. It also helps when running packet error-rate tests when a local MAC is not yet configured during prototyping.

Register Setting: See Reverse Loopback in [Appendix B](#).

NOTE: Data received still appears on the xMII interface when Reverse Loopback is enabled, unless the isolation is set using bit [10] in the BMCR.

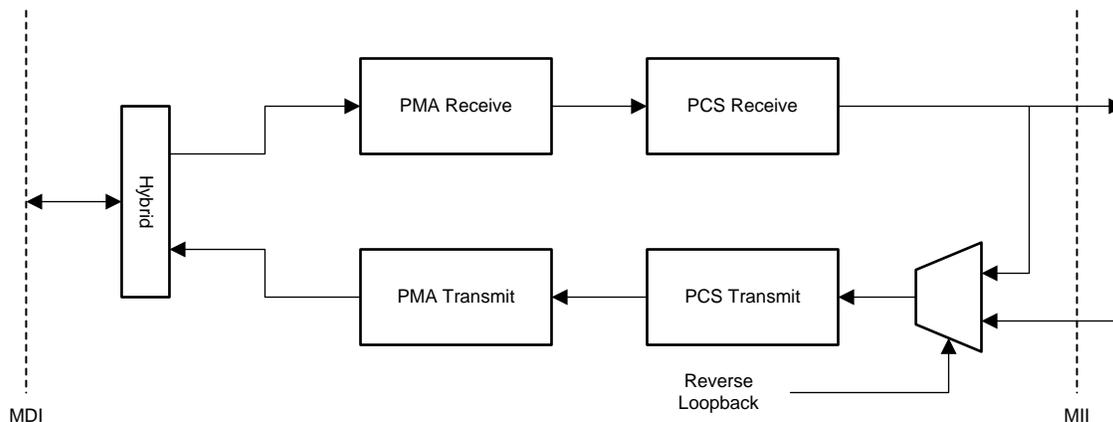


Figure 3. Reverse Loopback

4.3 Built-In Self-Test

The DP83TC811 has an internal built-in self-test (BIST) that allows for onboard testing without the need for a connected MAC. The DP83TC811 BIST is controlled using the BISCR, BIST Control and Status register 1 (BICSR1, address 0x1Bh), as well as the BIST Control and Status register 2 (BICSR2, address 0x1Ch). Bits [7:0] in BICSR1 defines the IPG in bytes. Bits [10:0] in BICSR2 defines the packet length in bytes.

BIST can be used with any loopback mode for customizable testing and debugging scenarios.

IEEE 802.3bw Compliance Testing Scripts for the DP83TC811

A.1 Test Mode 1

```
begin
// enabling test mode 1
000D 0001
000E 0836
000D 4001
000E 2000
end
```

A.2 Test Mode 2

```
begin
// enabling test mode 2
000D 0001
000E 0836
000D 4001
000E 4000
end
```

A.3 Slave Jitter

```
begin
// setting for LED_0 TX_TCLK
000D 001F
000E 0462
000D 401F
000E 0011
end
```

A.4 Test Mode 4

```
begin
// enabling test mode 4
000D 0001
000E 0836
000D 4001
000E 8000
end
```

A.5 Test Mode 5

```
begin
// enabling test mode 5
000D 0001
000E 0836
000D 4001
000E A000
end
```

Loopback and BIST Mode Scripts for the DP83TC811

B.1 xMII Loopback

```
begin
0000 6100    //enables xMII Loopback
end
```

B.2 Reverse Loopback

```
begin
0016 0110    //enables reverse loopback mode
end
```

B.3 BIST Script

```
begin
001B 007D    //bits[7:0] determine IPG, default 0x7D is equal to 500 bytes (125 * 4 bytes)
001C 05EE    //bits[10:0] determine packet length, default 0x5EE is equal to 1514 bytes
0016 7100    //enable continuous error check BIST mode
end
```

B.4 BIST With Reverse Loopback

```
begin
001B 007D    //bits[7:0] determine IPG, default 0x7D is equal to 500 bytes (125 * 4 bytes)
001C 05EE    //bits[10:0] determine packet length, default 0x5EE is equal to 1514 bytes
0016 7110    //enable continuous error check BIST mode with reverse loopback mode
end
```

B.5 BIST Status and Error Count

```
begin
0016          //reads address 0x0016, bits[11:9] show packet generator and checker status
001B 807D    //writes bit[15] to '1', sets bits[7:0] for 500 bytes (125 * 4 bytes) IPG
001B          //reads address 0x001B, bits[15:8] show BIST Error Count
end
```

PHY Test Mode Waveforms

C.1 Transmitter Output Droop

Figure 4 and Figure 5 show graphs of the transmitter output positive and negative droop, respectively.

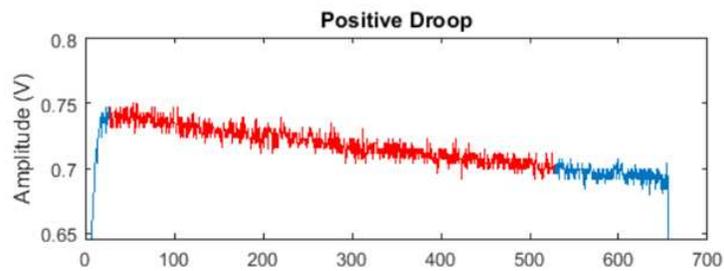


Figure 4. Transmitter Output Droop (Positive)

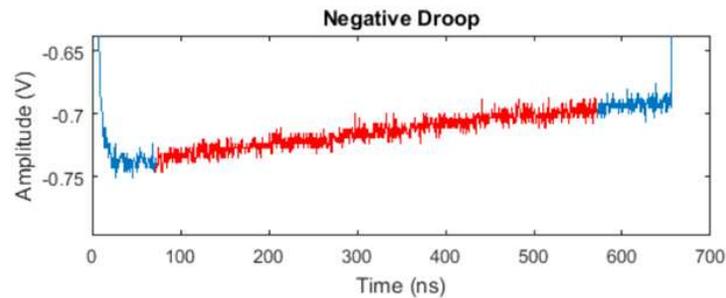


Figure 5. Transmitter Output Droop (Negative)

Figure 6 shows a graph of the transmitter distortion.

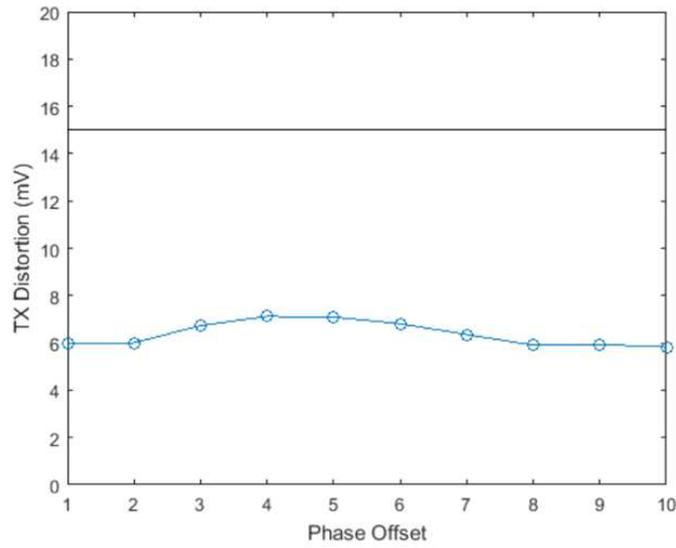


Figure 6. Transmitter Distortion

Figure 7 shows a graph of the PSD mask.

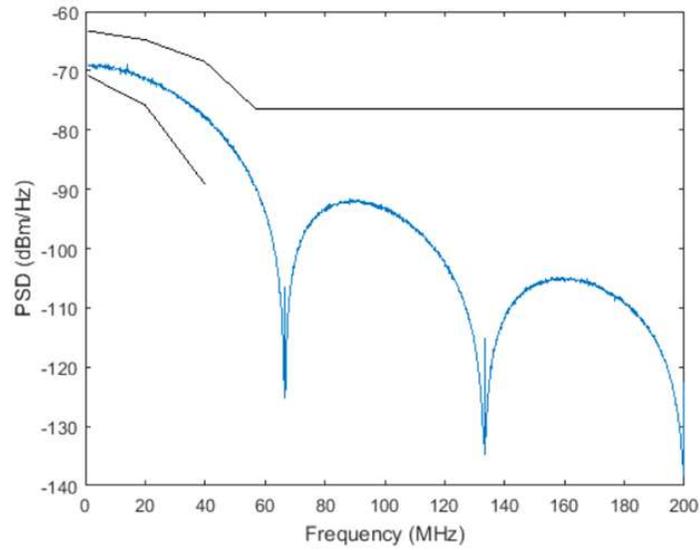


Figure 7. PSD Mask

Figure 8 shows a graph of the MDI return loss.

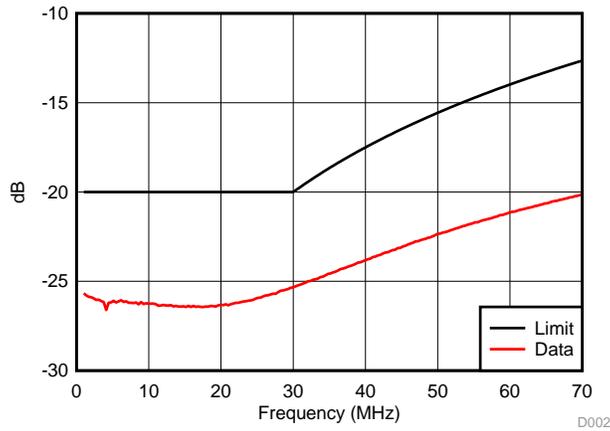


Figure 8. MDI Return Loss

Figure 9 shows a graph of the MDI mode conversion.

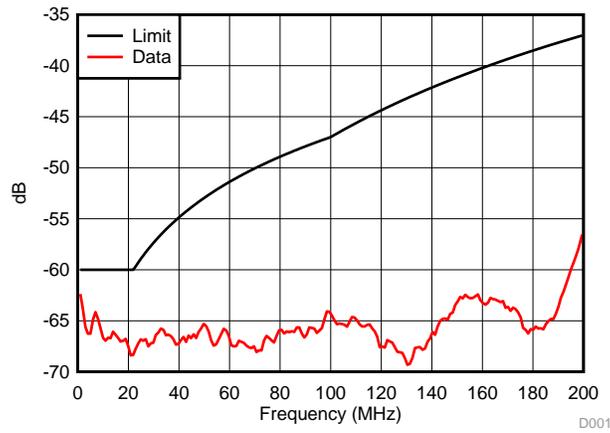


Figure 9. MDI Mode Conversion

Figure 10 shows a graph of the MDI IDLE stream.

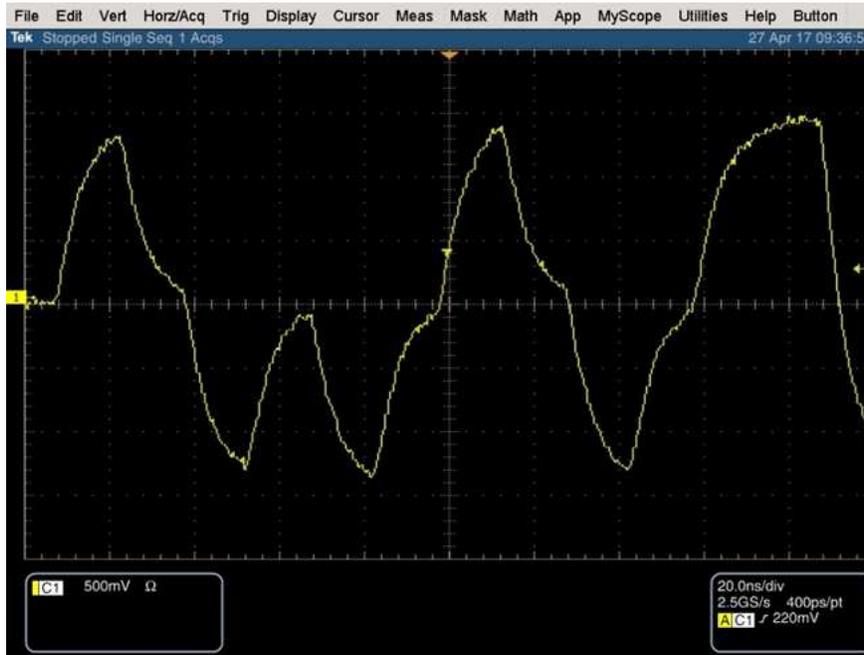


Figure 10. MDI IDLE Stream

Figure 11 shows a graph of the MDI IDLE stream with variable persistence.

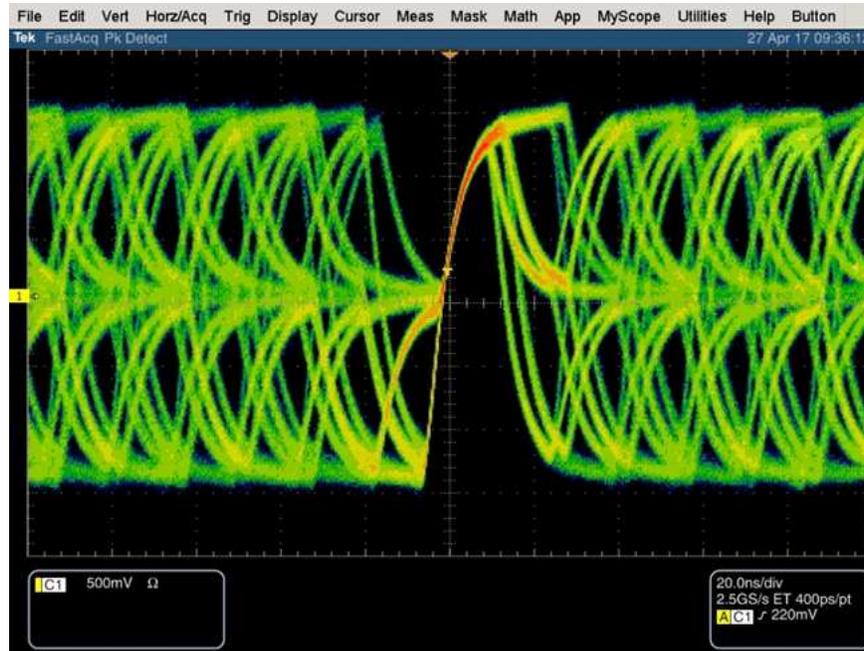


Figure 11. MDI IDLE Stream With Variable Persistence

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