Application Report
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DP83TC811 Low-Power Operation

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ABSTRACT

The DP83TC811-Q1 automotive Ethernet PHY supports multiple low power modes, as well as Wake-on-LAN (WoL), which are described in this application note. The Low Power State Machine (LPSM) operation is described, and a schematic example is provided.

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1 Introduction

The DP83TC811 is an automotive Ethernet PHY designed to operate at 100Mbps speed and support IEEE802.3bw, 100BASE-T1. Ethernet was originally designed for data sharing between computer workstations and for sending data to laser printers. Ethernet has evolved and now provides a standardized way for a wide range of applications to share information.

Automotive Ethernet is a new branch within the IEEE standard that focuses on increasing networking deployment within the vehicle, lowering radiated emissions (high emissions seen in multi-twisted pair Ethernet such as10BASE-T, 100BASE-TX and 1000BASE-T), as well as reducing vehicle weight by supporting full-duplex operation over unshielded single twisted pair (UTP). IEEE802.3bw defines this new automotive specification to meet all three critical items.

Another key objective of Ethernet deployment in automotive applications is low power consumption. One challenge with the current Ethernet solutions is the need for a constant IDLE stream to help point-to-point applications maintain link; and all associated sub-processes to achieve link. Because MDIs are always active, power dissipation, even when network utilization is zero, is higher than desired for most automotive applications. To prevent unwanted power consumption during low-utilization periods and when data transfer is not needed (i.e. car parked and ignition is off), the DP83TC811's low power state machine (LPSM) is used to transition the PHY and connected link-partner from an active/normal state through a series of intermediate steps until a low-power sleep state is achieved.

Additionally, the DP83TC811 supports an alternative method where the PHY is active but the connected processor is in a low-power state, using Wake-on-LAN (WoL).

This application note details the following:

- Low-power state machine
  - Possibly PHY states
  - State transitions
  - Associated PHY pins and usage
  - Example schematic for system implementation of the LPSM
- Wake-on-LAN
  - Principles behind WoL operation
  - Magic packet detection and custom packet detection
  - WoL implementation
  - Examples of how to use WoL

Table 1. Terminology

Acronym	Definition
DUT	Device under test
ED	Energy detect
EN	Enable (device pin)
INH	Inhibit (device pin)
IPG	Inter-frame packet gap
LPS	Low-power sleep
LPSM	Low-power state machine
MDI	Medium dependent interface
MII	Media independent interface
PCS	PHY control sublayer
PHY	Physical layer transceiver
PMA	Physical medium attachment
POR	Power-on-RESET
SMI	Serial management interface
WAKE	Wake (device pin)
WoL	Wake-on-LAN
WUR	Wake-up request

2 Low-Power State Machine

The LPSM defines the states and associated transitions supported by the DP83TC811 to achieve the most power efficient operation. Both PHYs must have the LPSM to transition into Silent and Sleep states. When not connected to an LSPM capable PHY, the DP83TC811 operates normally and not affect quality of link or other functional operations.

To enable the LPSM operation, the following register values must be set.

Table 2. Registers for Enabling Low Power State Machine Operation

Register name	Register address	Bit field and value	Notes	
AUTO_PHY	0x018B	bit[1] = 1	Use of Sleep mode enabled	
PWRM	0x018C	bit[1] = 1	Enables transmission of LPS code groups	
LPS_CTRL3	0x0493	bit[5:4] 00 = 0.4 ms 01 = 1 ms (default) 10 = 4 ms 11 = 8 ms	Sleep request timer settings	
LPS_CTRL2	0x0487	bit[0] = 1	Enables LPS code groups	
LPS_CFG	0x04E5	bit[9:8] = [11]	Enables Sdn[1] scrambled stream for LPS code groups	

2.1 PHY States

There are five defined digital states within the DP83TC811 and three additional states outside of the digital domain. For information regarding device behavior in each of the three additional states, see *DP83TC811 Data Sheet* and *DP83TC811S*.

This application note details the five states within the digital domain: Standby, Normal, Sleep Request, Silent, and Sleep. Figure 1 illustrates these PHY states and their relationship to one another. The state change conditions are described in subsequent sections of this application note, and in the data sheet.

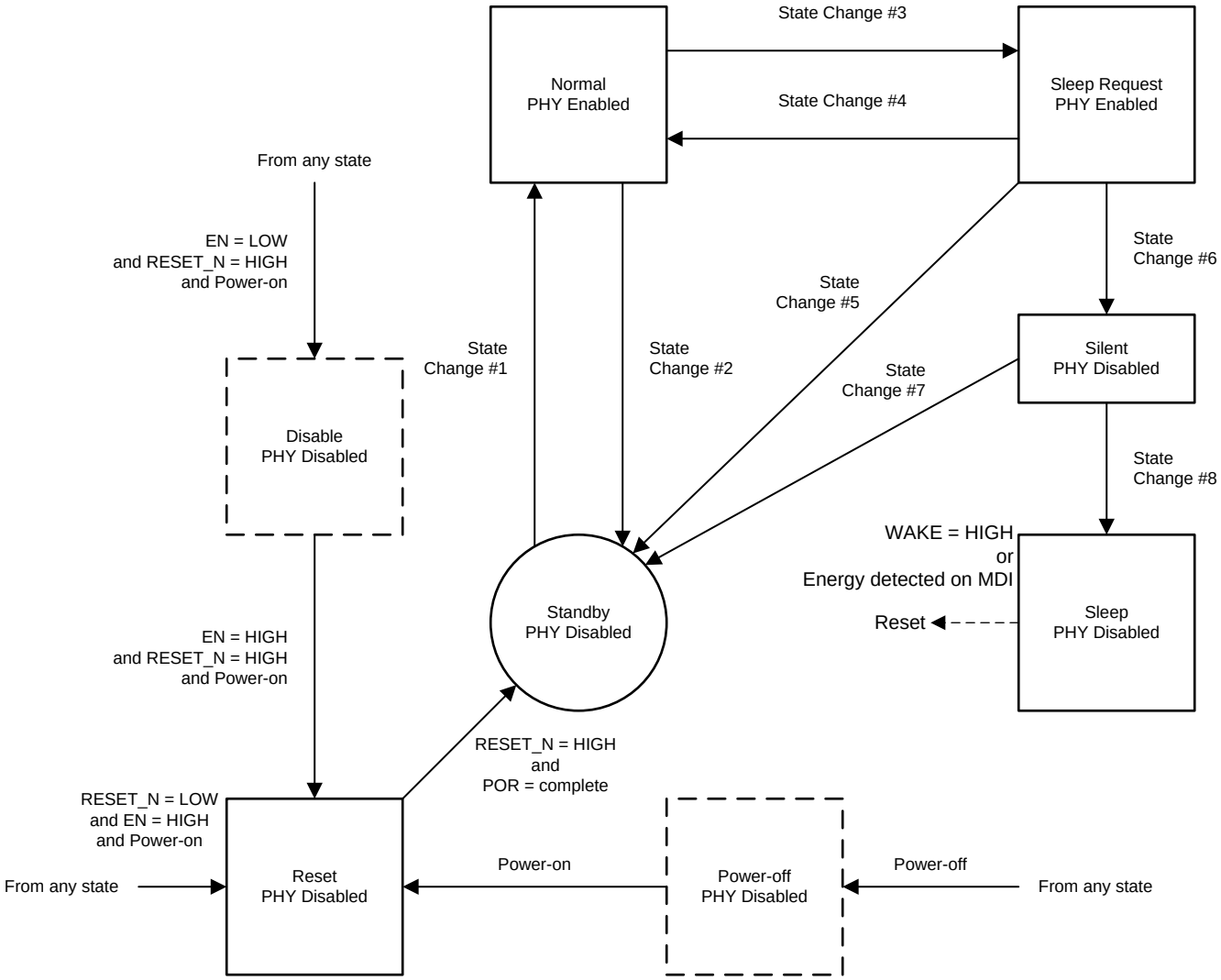

Figure 1. Low-Power State Machine

2.1.1 Standby

When configured in Master or Slave mode, the PHY automatically enters the Standby state after completing power-on reset (POR) if both EN and WAKE are in the active-HIGH state and the device is configured for Managed operation. The power consumption in Standby state is slightly lower when compared to the Normal state. For example, if VDDIO is 3.3V and the MAC interface is configured as MII, the supply current for the digital block is reduced from 31 mA to 24 mA (typical). Refer to the Electrical Characteristics table in the data sheet for a complete specification of Standby, Normal and Sleep currents for each VDDIO value and MAC interface format.

NOTE: Managed operation prevents the PHY from entering into Normal operation post POR and, requiring SMI register access to allow the device to exit Standby. Autonomous operation allows the PHY to automatically transition from POR to normal operation without user intervention. Managed and Autonomous operations are further described in *DP83TC811 Data Sheet*.

In Standby, all PHY functions are operational except for PCS and PMA blocks. The PHY is not able to establish a link when in Standby and cannot transmit or receive data on the MDI. SMI functions are operational when in Standby.

2.1.2 Normal

Normal state is reached through two methods: Autonomous or Managed. When Autonomous operation is enabled, the PHY automatically attempts to establish a link with a valid partner after POR.

In Managed operation, SMI access is required to allow the device to exit Standby. To force the device into Normal state, bit[0] in the Power Mode Register (PWRM, address 0x018C) must be set. This bit will self-clear once the device moves into Normal state.

Additionally, Autonomous operation can be configured through the SMI by setting bit[6] in the Low-Power Sleep Control Register (AUTO_PHY, address 0x018B).

2.1.3 Sleep Request

Sleep Request is an intermediate state that is entered when transitioning from Normal state to Sleep state. This intermediate state is used along with Silent state to provide a smooth transition out of an active operation to a low-power state. When in Sleep Request state, the PHY transmits low power sleep (LPS) code-groups to inform the link-partner that sleep is requested.

PHY sleep_rqst_timer begins once the PHY enters into Sleep Request state. The link partner decodes the LPS code groups and triggers the LPS_RECEIVED interrupt once confirmed. After the PHY sleep_rqst_timer expires, the PHY transitions to Silent state prior to entering Sleep.

During Sleep Request, any frame received on the MDI or MII terminates the sleep_rqst_timer and transitions the PHY out of Sleep Request and into Normal state. No data transmitted or received is lost during the transition.

2.1.3.1 Low-Power Sleep Code Groups

LPS code groups are used by the PHY to notify the link partner that it is requesting to enter into Sleep. The DP83TC811 encodes the LPS code-groups within the Sdn[1] scrambled stream.

Transmit and receive paths within the DP83TC811 are configured by default to use the same LPS code-group mechanism when enabled. The PHY immediately sends LPS code groups once it enters Sleep Request state. LPS code groups are sent until the sleep_rqst_timer expires or the PHY transitions out of Sleep Request into another state.

To transmit LPS code groups and decode received LPS code groups, bit[0] in the LPS Control Register #2 (LPS_CTRL2, address 0x0487) must be set, and

bits[9:8] in the LPS Configuration register (LPS_CFG, address 0x04E5) are set to [1,1], as shown in Table 3 .

Table 3. LPS Code Group Configuration, Reg. 0x04E5

Bit[9]	Bit[8]	Description
0	0	Reserved
0	1	Reserved
1	0	Reserved
1	1	Sdn[1]

If configured for programmable mode, TX LPS CODES Register (TX_LPS_CODES, address 0x4E1) and RX LPS CODES Register (RX_LPS_CODES, address 0x4E3) define the code groups for LPS transmission and reception. By default, the programmable LPS code groups consist of the vector sequence (0, 0), (0, 0), (1, -1), (1, -1).

2.1.4 Silent

Silent state is entered once the sleep_rqst_timer expires, or when the PHY detects that the link partner TX mode = SEND_Z, where vectors of ternary symbols defined by (0, 0) are received on the MDI, indicating that the link partner has already moved to Silent state. The silent_timer begins counting down once in Silent state. After the timer expires, the PHY transitions to Sleep state. However, if nonzero ternary symbols are detected on the MDI after silent_timer expiration, the PHY enters Standby.

2.1.5 Sleep

Sleep state is the lowest power mode of the DP83TC811. To enter Sleep, the PHY must have sleep_en set using bit[1] in the LPS_CTRL register and have the silent_timer expire. If sleep_en is not set, the PHY will transition to Standby once silent_timer expires. When in Sleep, all PHY blocks are disabled except for energy detection circuit. All register configurations are lost in Sleep state. No link can be established, data cannot be transmitted or received, and the SMI is disabled. When in Sleep, INH is asserted HIGH; his pin will be LOW in all other states. The current consumption of the digital block drops into the low uA range. For example, if VDDIO is 3.3V, and the MAC interface is MII mode, IDDIO drops to 14 uA.

The PHY will exit Sleep state and reconfigure (POR) after any of the conditions listed in Table 4 occur:

Table 4. Autonomous Mode Configuration

PHY Mode	Wake-up Method
Slave	Energy detected on MDI
	EN pin de-asserted and then reasserted
	RESET_N pin de-asserted and then reasserted
Master	Energy detected on MDI
	EN pin de-asserted and then reasserted
	RESET_N pin de-asserted and then reasserted
	WAKE pin asserted

2.2 State Transitions

This section details the specific events and conditions that cause the PHY to transition between states while operating with the LPSM.

2.2.1 State Transition #1

Standby → Normal

Autonomous Operation

The PHY automatically transitions to Normal state upon POR completion when configured for autonomous operation.

Autonomous operation can be configured by the methods listed in Table 5:

Table 5. Autonomous Mode Configuration

Method	Description
Hardware bootstrap	Set AUTO bootstrap to Mode 1 on LED_1
Register access	Set bit[6] in AUTO_PHY register (0x018B)

Managed Operation

The PHY transitions to Normal and out of Standby if any of the methods listed in Table 6 occurs:

Table 6. Managed Mode State Transition

Method	Description
Energy detection	When in slave mode and energy is detected on the MDI
Register access	Autonomous configuration by setting bit[6] in AUTO_PHY register (0x018B)
	Forcing Normal state by setting bit[0] in PWRM register (0x018C)

2.2.2 State Transition #2

Normal → Standby

The PHY cannot directly transition from the Normal state to the Standby state. It must first pass through the Sleep Request state and Silent state to enter Standby.

2.2.3 State Transition #3

Normal → Sleep Request

The PHY enters Sleep Request state from any of the methods listed in Table 7:

Table 7. State Transition #3

Method	Description
Register access	Forcing Sleep Request state by setting bit[1] in PWRM Register (0x018C)
LPS received	sleep is enabled by setting bit[1] in the AUTO_PHY Register (0x018B) *and* valid LPS code-groups are received on the MDI from the link-partner

2.2.4 State Transition #4

Sleep Request → Normal

The PHY exits Sleep Request state and enters Normal state when any of the methods listed in Table 8 occurs:

Table 8. State Transition #4

Method	Description
Register access	Forcing Normal state by setting bit[0] in PWRM Register (0x018C)
Frame detection	A valid frame is transmitted or received before sleep_rqst_timer expires
Invalid LPS	A valid frame is received, but no valid LPS code-groups are received on MDI prior to sleep_rqst_timer expiration

2.2.5 State Transition #5

Sleep Request → Standby

The PHY cannot directly transition from the Sleep Request state to the Standby state. It must first pass through the Silent state to enter Standby.

2.2.6 State Transition #6

Sleep Request → Silent

The PHY exits Sleep Request state and enters Silent state when any of the following methods listed in Table 9 occurs:

Table 9. State Transition #6

Method	Description
Confirmed LPS	Valid LPS code-groups are received on the MDI *and* sleep_rqst timer has expired
Quiet MDI	SEND_Z [ternary symbol vectors of (0,0)] are detected on theMDI

2.2.7 State Transition #7

Silent → Standby

The PHY exits Silent state and enters Standby state when any of the following occurs:

Table 10. State Transition #7

Method	Description
Sleep disabled	sleep_en is disabled by setting bit[1] = 0 in PWRM Register (0x018C) *and* silent_timer expiration
MDI detection	Non-SEND_Z code-groups are detected on MDI prior to silent_timer expiration

2.2.8 State Transition #8

Silent → Sleep

The PHY exits Silent state and enters Sleep state once the silent_timer expires and no activity is detected on the transmitter or receiver.

2.2.9 Hardware Settings

To enable the use of the LPSM, the following hardware settings are required:

- • The WAKE pin on a Master PHY cannot be tied to VDD. It must be actively controlled. If WAKE is tied to VDD without a way to pull the pin LOW, the PHY will never be able to enter into Sleep.
- • The WAKE pin for a Slave PHY is a DON”T CARE.

2.3 Master and Slave LPS Exchange Flow

To better understand the exchange flow between Master and Slave PHYs, see Figure 2.

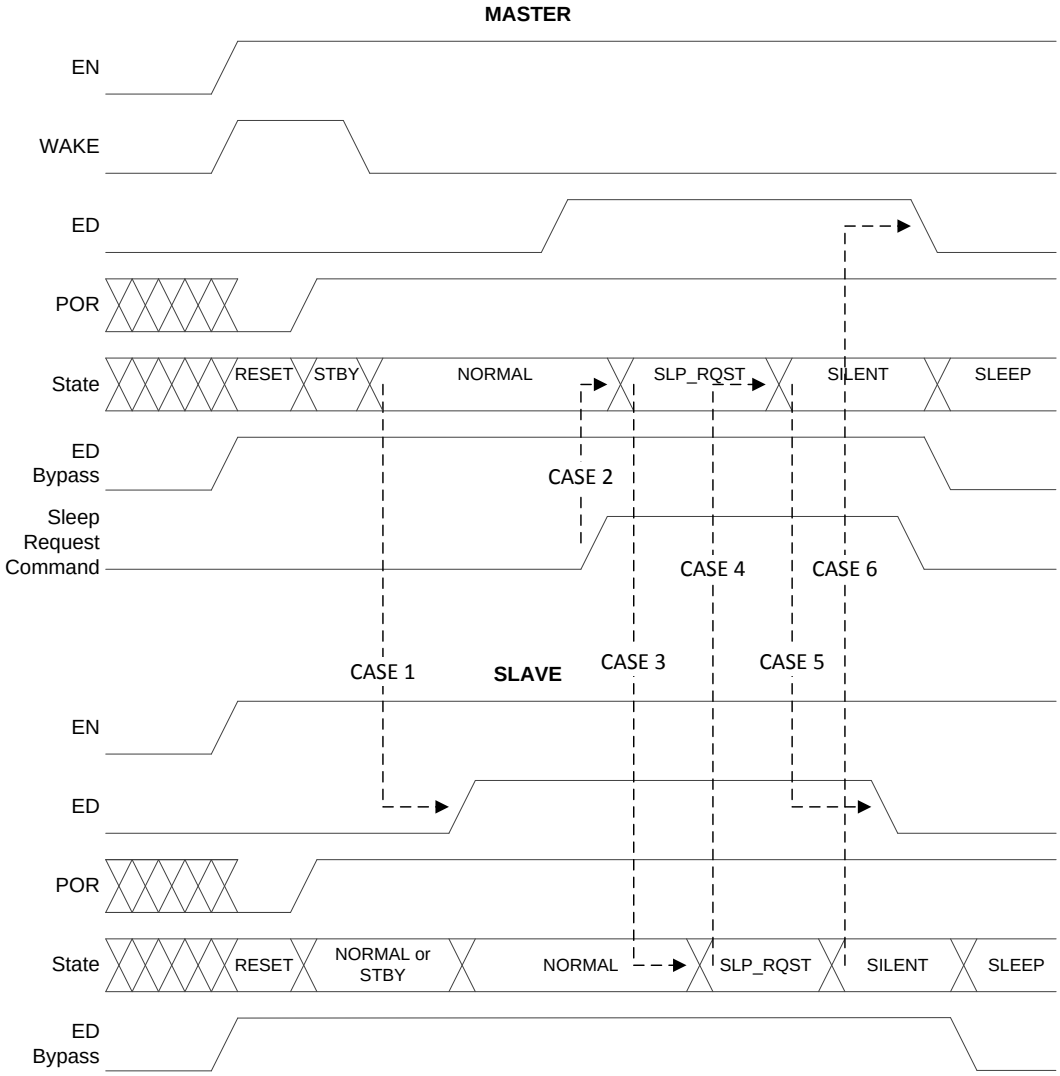

Figure 2. LPS Exchange Flow

The exchange flow shown in Figure 2 can be broken down to the following events:

1. The Master and Slave are powered-up. POR executes with both PHYs enabled by pulling EN pin HIGH.
2. The WAKE pin of the Master is toggled for min_wake_timer duration.
3. The Master PHY is awakened and begins to transmit SEND_I (IDLEs).

   Case 1: Slave detects SEND_I of the Master.
   1. The internal energy detect (ED) signal of the Slave goes HIGH.
   2. The Slave transitions to Normal state.

   Case 2: The Master receives Sleep Request command from either MDI or SMI.
4. The Master transitions to Sleep Request and transmits LPS code groups.

   Case 3: The Slave receives LPS code groups.
   1. The Slave transitions to Sleep Request state.
   2. The Slave transmits LPS code-groups.

   Case 4: The Master receives the Slave LPS code groups.
5. The Master sleep_rqst_timer expires.
   1. The Master transitions to Silent.
   2. The Master transmitter switches to TX mode = SEND_Z.

   Case 5: The Slave no longer detects energy on the MDI.
   1. The Slave ED signal goes LOW.
6. The Slave sleep_rqst_timer expires.
   1. The Slave transitions to Silent.
   2. The Slave transmitter switches to TX mode = SEND_Z.

   Case 6: The Master no longer detects energy on the MDI.
   1. The Master ED signal goes LOW.
7. The Master and Slave silent_timer expires.
   1. The Master and Slave are now in Sleep state.
   2. The INH pin is set HIGH for both devices.

2.4 Implementing LPSM PHY

This section details how to implement a DP83TC811 for applications using the LPSM feature.

2.4.1 High-Level Description

When using the LPSM, there are some critical signals that must be used to enable seamless transitions from one state to another.

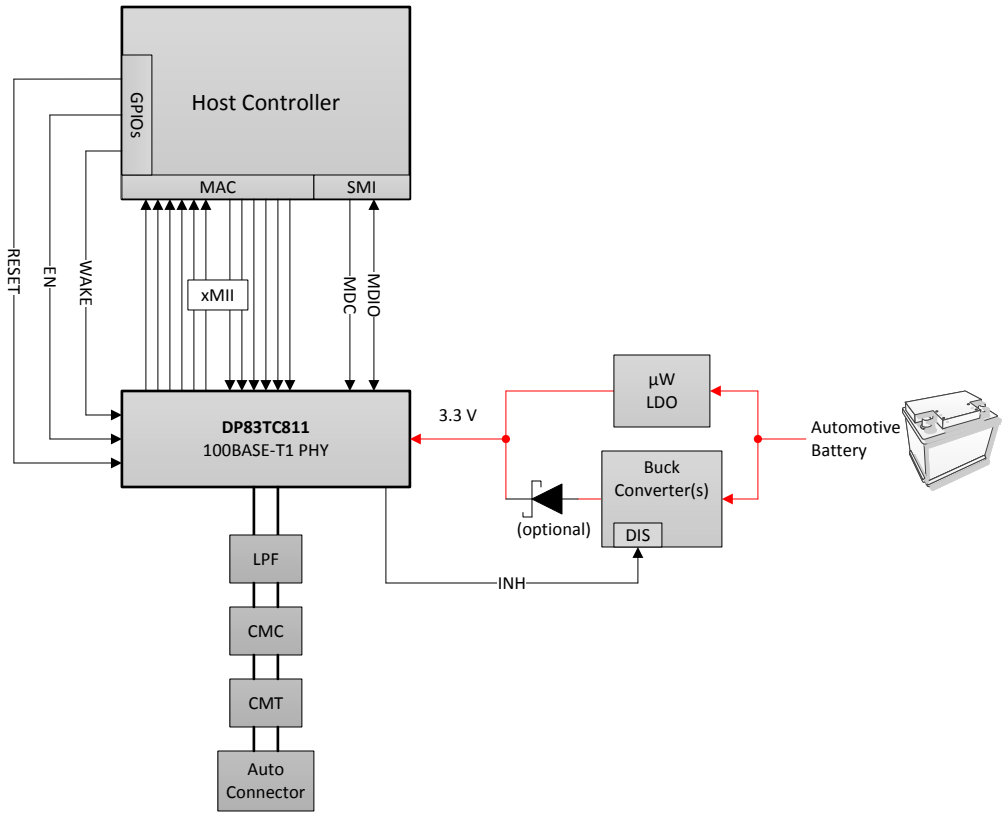

Figure 3. High-Level Implementation

This implementation (shown in Figure 3) applies to both the Master and Slave PHY, except there is no need to route WAKE with the Slave because this pin is a do not care. During operation, data is exchanged between the MAC/SMI and the DP83TC811 of the host controller over an xMII connection. The INH pin from the DP83TC811 is routed to the DISABLE pin of the buck converter. A µW LDO, always ON, is in parallel to the buck converter. To prevent back-driving into the buck converter, a Schottky diode is used and the µW LDO is set to a slightly lower voltage than the buck converter. Note that this implementation assumes that the µW LDO appears as open when back driven.

Once the DP83TC811 enters into Sleep, INH will be asserted HIGH, disabling the buck converter. As the voltage on the line begins to drop, the µW LDO begins to regulate the line, providing an uninterrupted supply to the DP83TC811.

When the PHY wakes up, INH will de-assert and go LOW, enabling the buck converter. As the buck converter stabilizes and supplies the line, the µW LDO will again disable because its output is lower than that of the buck converter.

2.4.2 Schematic Example

Figure 4 provides a more detailed example for using two parallel LDOs for the DP83TC811-Q1 when using the LPSM. In this example, another option is shown for the primary voltage source, the TL1963A-Q1 low noise LDO. The output of both LDOs can be connected to supply pins of the DP83TC811-Q1; in this case, both VDDA and VDDIO. The Schottky diode is not shown in this schematic, but must be included if required by the primary LDO or voltage source.

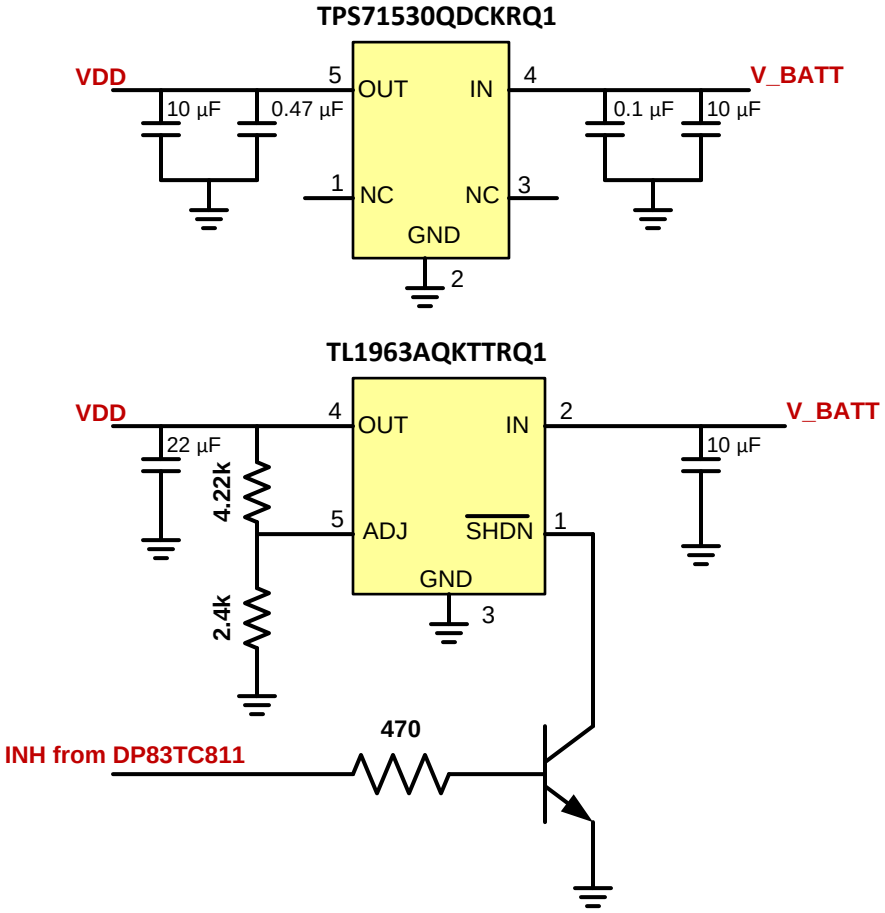

Figure 4. Voltage Supply Schematic for LPSM Implementation

The INH pin of the DP83TC811-Q1 is routed to an external switch that pulls the SHDN_N pin LOW on the TL1963A when the DP83TC811-Q1 enters into Sleep state. The TL1963A will be disabled, but with the TPS71530 always on, the DP83TC811-Q1 remains in sleep and does not completely power down.

For more detailed and complete reference schematics, see application note SNLA292, which contains multiple examples of xMII connections for the DP83TC811-Q1. The power supply connections shown in Figure 4 can be used with any of the examples in the application note.

3 Wake-on-LAN

This section discusses the principles behind WoL and implementation of WoL.

3.1 WoL Principles of Operation

WoL is a mechanism that maintains full function of the PHY, but allows for specific frame detection based on the mode of operation desired. By using WoL, backend equipment (i.e. FPGAs, processors, ASICs, MCUs) can be powered down until the PHY receives information that passes the specific frame detection criteria. An active link with a link partner is maintained while operating with WoL enabled. When a qualifying frame is received, the DP83TC811 will either assert a level change or pulse indicates on any of the three GPIOs that can be configured through register access. Additionally, the DP83TC811 allows for interrupt configuration on the INT pin with polarity specification as active-HIGH or active-LOW.

There are three main WoL functions supported by the DP83TC811 to allow for user flexibility and security:

- Magic Packet Detection
- Magic Packet Detection with Secure-ON
- Custom Pattern Detection

The DP83TC811 offers features that allow for a range of security options. Magic Packet structure is vulnerable to hacks because it only requires one to know the MAC address of the node connected. Magic Packet Detection with Secure-ON adds an additional 6-byte user defined password for added protection. Additionally, the DP83TC811 supports a Secure-ON Hack Flag, which is triggered if a Magic Packet arrives with an invalid Secure-ON password. The DP83TC811 WoL feature goes a step further by providing custom user definable 64-byte sequence frame detection.

3.1.1 Magic Packet Detection

When configured for Magic Packet Detection, the PHY scans all incoming frames addressed to the node for a specific data sequence. This sequence identifies the frame as a Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which may be the IEEE address of the receiving station or a BROADCAST ADDRESS), and CRC.

The specific Magic Packet sequence consists of 16 duplications of the MAC address of this node with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6-bytes of 0xFF.

3.1.2 Magic Packet Detection with Secure-ON

The DP83TC811 also offers Magic Packet Detection with Secure-ON for increased security. Secure-ON is a 6-byte user configurable password through register access.

A Magic Packet frame with Secure-ON must also meet the basic requirements detailed in Section 3.1.1.

The specific Magic Packet sequence with Secure-ON consists of 16 duplications of the MAC address of this node with no breaks or interruptions, followed by Secure-ON 6-byte password. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6-bytes of 0xFF. Figure 5 shows a Magic Packet structure.

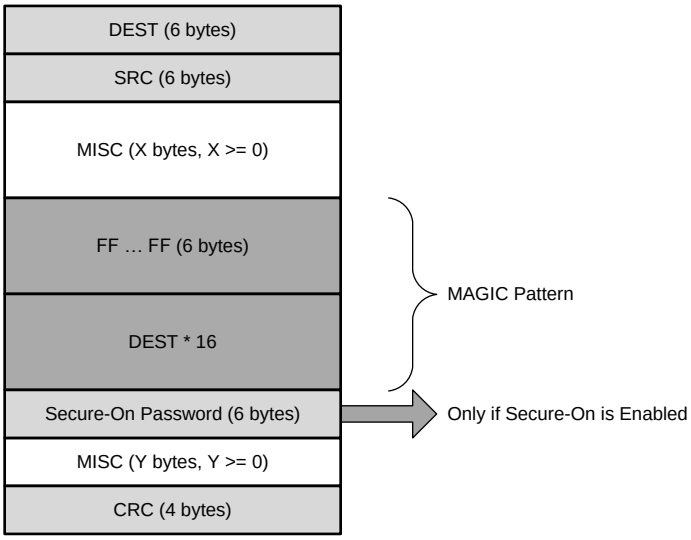

Figure 5. Magic Packet Structure

3.1.3 Custom Pattern Detection

When configured for Custom Pattern Detection, the PHY scans all incoming frames addressed to the node for a specific data sequence. This sequence identifies the frame as a Custom Pattern frame.

A Custom Pattern frame does not need to adhere to the basic requirements for LAN technology.

The Custom Pattern frame can be up to a 64-byte sequence that is defined by the user in registers. An optional Byte Mask register within the DP83TC811 provides more customization by allowing the user to selectively mask the incoming sequence to specify a smaller sequence in the range of 1-byte to 64-byte.

3.2 Implementing WoL

WoL must be enabled through register configuration using the SMI. All WoL registers are located in the vendor specific register map, which requires the vendor specific DEVAD [4:0] = ‘11111’ (0x1F).

3.2.1 Implementing of Magic Packet Detection

WoL Magic Packet detection requires use of the following registers:

- Receive Configuration Register (RXFCFG, address 0x04A0)
- Receive Status Register (RXFS, address 0x04A1)
- MAC Destination Address Register 1 to 3 (MACDA, address 0x04A2 to 0x04A4)

Two examples below are intended to display various configuration options when using Magic Packet detection in the DP83TC811.

3.2.1.1 Example #1 – Pulse Mode Indication on LED_0

MAC ADDRESS = 00:17:83:E2:FC:73

To enable Magic Packet detection with pulse (32 clock cycles) indication on LED_0, use the register configurations listed in Table 11.

Table 11. Magic Packet with Pulse Mode Indication

Step	Register	Value	Description
1	0x04A2	0x1700	MAC address bytes 5 and 4
2	0x04A3	0xE283	MAC address bytes 3 and 2
3	0x04A4	0x74FC	MAC address bytes 1 and 0
4	0x0462	0x0002	Configures LED_0 for WoL indication
5	0x04A0	0x0481	WoL enabled, pulse indication, 32 clock cycles

3.2.1.2 Level Change Indication on LED_1

MAC ADDRESS = 00:17:83:B2:F7:45

To enable Magic Packet detection with level change indication on LED_1, use the register configurations listed in Table 12.

Table 12. Magic Packet with Level Change Indication

Step	Register	Value	Description
1	0x04A2	0x1700	MAC address bytes 5 and 4
2	0x04A3	0xB283	MAC address bytes 3 and 2
3	0x04A4	0x45F7	MAC address bytes 1 and 0
4	0x0462	0x0200	Configures LED_0 for WoL indication
5	0x04A0	0x0981	WoL enabled, level change
6	0x04A0	0x0981	WoL enabled, level change, clear one level

NOTE: For level change mode, bit[11] in register 0x04A0 must be set to 0 to clear the level change indication.

3.2.2 Implementing Magic Packet Detection with Secure-ON

WoL Magic Packet detection with Secure-ON requires use of the following registers:

- Receive Configuration Register (RXFCFG, address 0x04A0)
- Receive Status Register (RXFS, address 0x04A1)
- MAC Destination Address Register 1 to 3 (MACDA, address 0x04A2 to 0x04A4)
- Receive Secure-ON Password Registers 1 to 3 (RXFSOP, address 0x04A5 to 0x04A7)

Two examples below are intended to display various configuration options when using Magic Packet detection with Secure-ON in the DP83TC811.

3.2.2.1 Secure-ON, Pulse Mode Indication on LED_0

MAC ADDRESS = 00:17:83:F3:A1:38

Secure-ON Password = 3C-41-9D-44-BB-5E

To enable Magic Packet detection with Secure-ON and pulse (64 clock cycles) indication on LED_0, use the register configurations listed in Table 13.

Table 13. Magic Packet with Secure-ON and Pulse Mode Indication

Step	Register	Value	Description
1	0x04A2	0x1700	MAC address bytes 5 and 4
2	0x04A3	0xF383	MAC address bytes 3 and 2
3	0x04A4	0x38A1	MAC address bytes 1 and 0
4	0x04A5	0x413C	Secure-ON bytes 0 and 1
5	0x04A6	0x449D	Secure-ON bytes 2 and 3
6	0x04A7	0x5EBB	Secure-ON bytes 4 and 5
7	0x0462	0x0002	Configures LED_0 for WoL indication
8	0x04A0	0x06A1	WoL enabled, pulse indication, 64 clock cycles

3.2.2.2 Secure-ON, Level Change Indication on LED_1

MAC ADDRESS = 00:17:83:DD:23:79

Secure-ON Password = DF-CB-85-68-17-05

To enable Magic Packet detection with Secure-ON and level change indication on LED_1, use the register configurations listed in Table 14.

Table 14. Magic Packet with Secure-ON and Level Change Indication

Step	Register	Value	Description
1	0x04A2	0x1700	MAC address bytes 5 and 4
2	0x04A3	0xDD83	MAC address bytes 3 and 2
3	0x04A4	0x7923	MAC address bytes 1 and 0
4	0x04A5	0xCBDF	Secure-ON bytes 0 and 1
5	0x04A6	0x6885	Secure-ON bytes 2 and 3
6	0x04A7	0x0517	Secure-ON bytes 4 and 5
7	0x0462	0x0200	Configures LED_1 for WoL indication
8	0x04A0	0x01A1	WoL enabled, level change
9	0x04A0	0x09A1	WoL enabled, level change, clear level change

NOTE: For level change mode, bit[11] in register 0x04A0 must be set to 0 to clear the level change indication.

3.2.3 Implementing Custom Pattern Detection

WoL Custom Pattern detection requires use of the following registers:

- Receive Configuration Register (RXFCFG, address 0x04A0)
- Receive Status Register (RXFS, address 0x04A1)
- Receive Pattern Register 1 to 32 (RXFPAT, address 0x04A8 to 0x04C7)
- Receive Pattern Byte Mask Registers 1 to 4 (RXFPBM, address 0x04C8 to 0x04CB)

The example below is intended to display configuration options when using Custom Pattern detection in the DP83TC811.

3.2.3.1 Custom Pattern, Pulse Mode Indication on CLKOUT

Byte Mask = 00-FF-FF-FF-FF-FF-FF-FF (Masking bytes 8 to 63) Custom Pattern = 01-23-45-67-89-AB-CD-EF (First eight bytes programmed, bytes 8 to 63 left to default 0x00 because they are don't-cares).

To enable Custom Pattern detection with pulse (8 clock cycles) indication on CLKOUT, use the register configurations listed in Table 15.

Table 15. Custom Pattern Pulse Mode Indication on CLKOUT

Step	Register	Value	Description
1	0x04A8	0x2301	Pattern bytes 0 and 1
2	0x04A9	0x6745	Pattern bytes 2 and 3
3	0x04AA	0xAB89	Pattern bytes 4 and 5
4	0x04AB	0xEFCD	Pattern bytes 6 and 7
5	0x04C8	0xFF00	Byte mask 0 to 15
6	0x04C9	0xFFFF	Byte mask 16 to 31
7	0x04CA	0xFFFF	Byte mask 32 to 47
8	0x04CB	0xFFFF	Byte mask 48 to 63
9	0x0463	0x0002	Configures CLKOIT for WoL indication
10	0x04A0	0x0082	WoL enabled, pulse indication, 8 clock cycles

4 Conclusion

There are two primary methods for operating with reduced power consumption in the DP83TC811: LPSM and WoL. Both methods have their own respective advantages, which must be considered when designing an optimized end equipment solution.

- PHY level power reduction is best achieved when using the LPSM because the device can self-power-down.
- System level power reduction is best achieved when using WoL because the PHY can wake-up the host controller when a qualifying frame is received.

For further details about the DP83TC811, please see the DP83TC811 datasheet (SNLS579, SNLS551).

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