Application Report
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Power-over-Coax Design Guidelines for DS90UB953-Q1

Cole Macias and Mandeep Singh

ABSTRACT

The DS90UB953-Q1 serializer represents the next generation in FPD-Link III serializers and is designed to support high-speed raw data sensors like 2MP imagers at 60 fps, as well as 4MP, 30-fps cameras, satellite RADAR, LIDAR, and Time-of-Flight (ToF) sensors. The chip delivers a 4.16-Gbps forward channel and an ultra-low latency, 50-Mbps bidirectional control channel, and also supports Power-over-Coax (PoC). The DS90UB953-Q1 also has advanced data protection and diagnostic features to support ADAS and autonomous driving. Together with a companion deserializer, the DS90UB954-Q1 delivers precise multi-camera sensor clock and sensor synchronization.

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Trademarks

1 Introduction

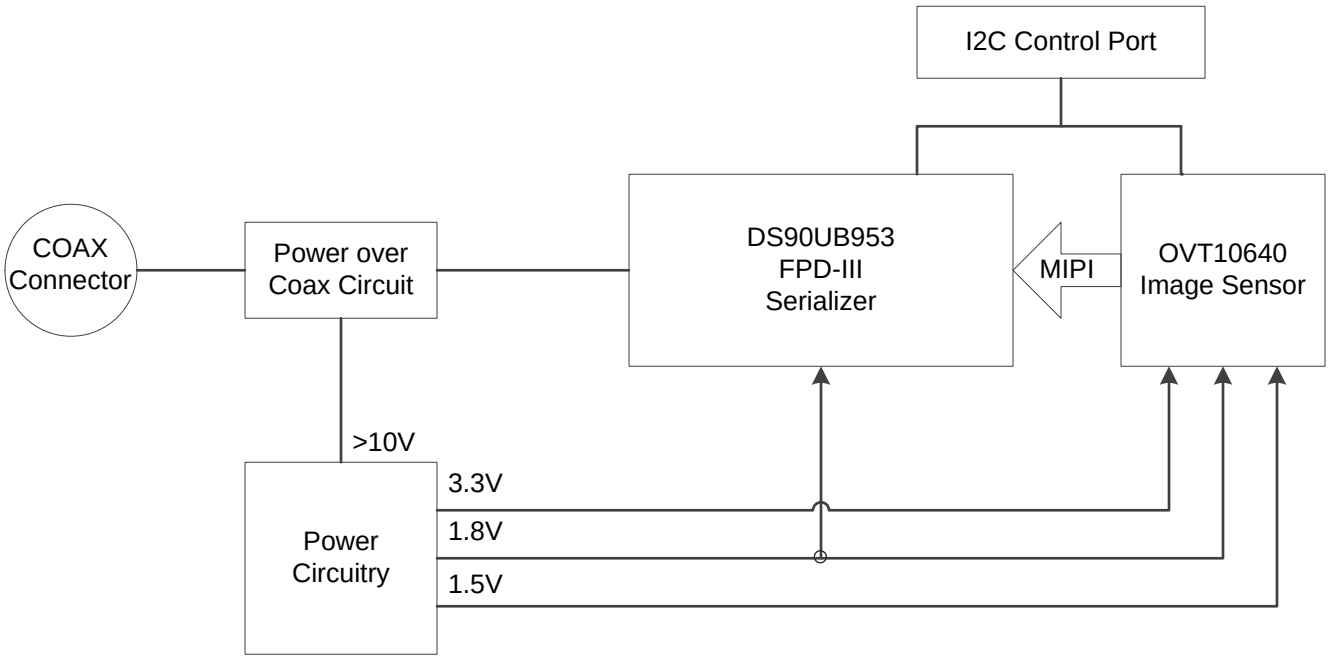

Figure 1. DS90UB953-Q1 and Camera Block Diagram With Power-over-Coax (PoC)

Real-time surround view has become a necessity in modern day automobiles with advanced driver-assistance systems (ADAS). General safety features, advanced driver-assist features, and autonomous vehicles all depend on multi-sensor systems acting in real time. Camera modules placed in strategic locations provide the best view around the outside of the vehicle. Typically, these placements do not have direct access to power. Therefore, the ability to remotely-power automotive sensors has become a sought-after feature. This application note outlines the design theory, with examples, when designing a remotely-powered device being implemented with a high-performance FPD-Link III, serializer/deserializer (SerDes) chipset.

A FPD-Link III system allows the video data, bidirectional control data, and power to be sent over a single coaxial cable. In a Power-over-Coax circuit, the direct current (DC) power for the sensor is separated from the transport high-speed data and is used to power the serializer and sensor in a SerDes system.

The DS90UB953-Q1 is a serializer to support automotive camera designs. The DS90UB953-Q1 is designed to support high-speed raw data sensors including 2MP imagers at 60 fps and as well as 4MP, 30-fps cameras, satellite RADAR, LIDAR, and Time-of-Flight (ToF) sensors. The chip delivers a 4-Gbps+ forward channel and an ultra-low latency, 50-Mbps, bidirectional control channel. In addition, the DS90UB953-Q1 features advanced data protection and diagnostic features to support ADAS and autonomous driving. Together with a companion deserializer, the DS90UB954-Q1 delivers precise multi-camera sensor clock and sensor synchronization.

Automotive sensors are often located in remote positions such as bumpers or trunk lids. A major component of the system cost is the wiring; therefore it is desirable to minimize the wiring to the camera by using a PoC circuit. This is because a shielded coaxial cable has less copper and lighter weight than transporting power and ground over separate wires in a shielded-twisted pair (STP) or a shielded-twisted quad (STQ) format.

2 Theory of Operation

2.1 Frequency Response

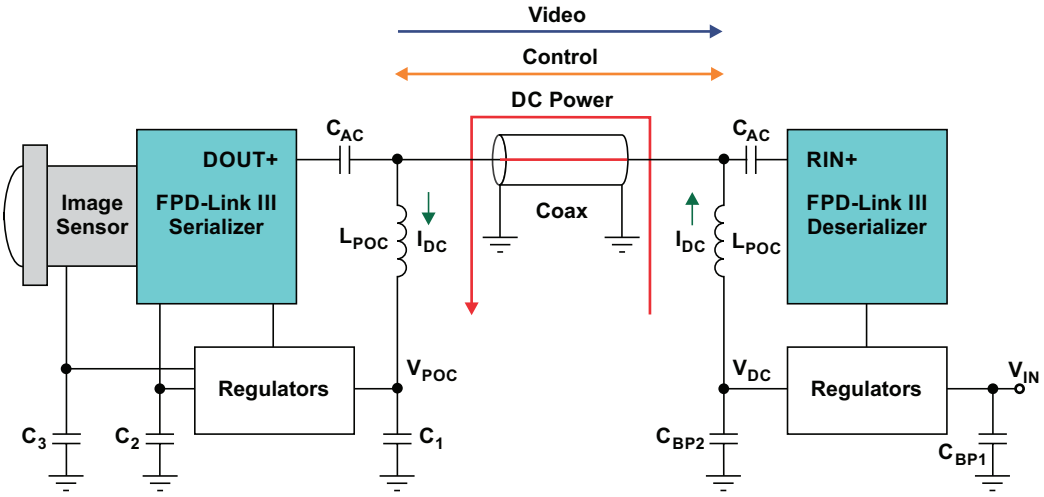

Figure 2. Block Diagram for Sharing Signal and DC Power on One Cable

Figure 2 shows a detailed implementation of the remote camera module. An inductor, L_{POC}, is used on each side of the cable to deliver DC power. At high frequencies, the inductor presents a high impedance that blocks the AC high-speed video and low-speed control signals. The coupling capacitors, C_{AC}, block the DC power voltage so that only the AC signals are allowed to communicate between the serializer and the deserializer.

The design of the isolation network that separates the power from the communications channels is therefore dependent on which mode the back channel is operating in. As a result, the mode will determine the frequency band during operation. In the case of the DS90UB953-Q1, the design on this circuit assumes that the forward channel will be in one of the modes where it is operating at 4 Gbps, and the back channel will be using the 25-MHz clock frequency. For 50-Mbps back channel rate, the $f_{BC}/2$ = 25 MHz. As a result, the designer must pay particular attention to a frequency band from 20 MHz to 2 GHz.

While this process will not be covered in this document, the DS90UB953-Q1 is compatible with deserializers with slower data rates, such as the DS90UB914A. However, the frequency band of interest will be different. The PoC network and the AC-coupling caps must be changed to accommodate for the lower data. PoC and AC cap recommendations can be found in the *DS90UB913A-CXEVM and DS90UB914A-CXEVM User's Guide* (SNLU135).

2.2 Return Loss Over Frequency Band

Table 1. Typical Specifications for Return Loss for the DS90UB953-Q1 PoC Network Running at 4 Gbps

OPERATION	TYPICAL RETURN LOSS PROFILE	EXAMPLE CONFIGURATION
4 Gbps	< –25 dB at 20 MHz < –12 dB at 2 GHz	FB + FB + FB + (10 µH || 4k)

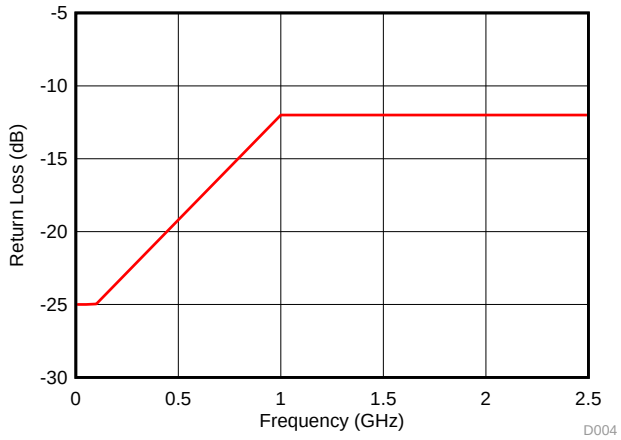

Figure 3. Return Loss Specification Graph

To determine what constitutes acceptable impedance for the DS90UB953-Q1, two parameters must be examined: the DC resistance of the circuit and cable and the return loss of the filter. As shown in Table 1, the typical input impedance seen by the sensor should yield return loss that is less than –25 dB at 20 MHz and less than –12 dB through 2 GHz. Return loss refers to the amount of reflections seen by the transmitter, so higher return loss from 20 MHz to 2 GHz will result in degraded performance using theDS90UB953-Q1.

Figure 3 shows the recommended specifications for the return loss scatter parameters (s-parameters) associated with measured return loss of a system. Specifically, the lines outline the typical return loss specifications for 4G operation. The typical return loss should be less than –25 dB at 20 MHz and less than –12 dB through 2 GHz, hence the typical return loss of the system should be below this line.

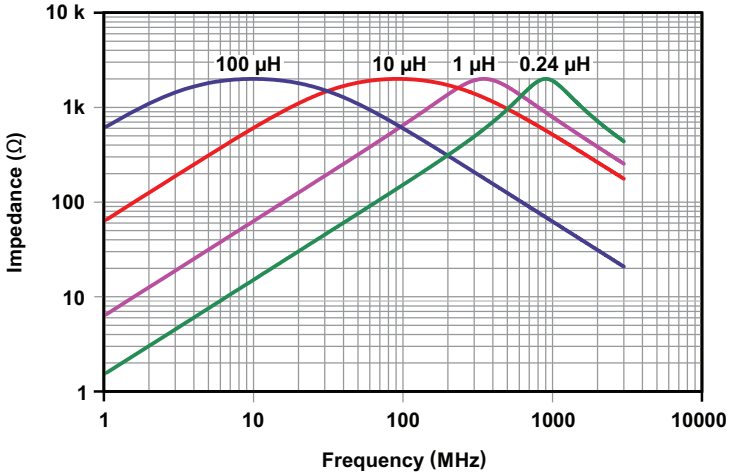

Figure 4. Impedance Plot of Individual Inductors

A 10-µH inductor is best for obtaining good return loss over the used frequency band. All inductors contain parasitic capacitance, however, which will not maintain good return loss and impedance through 2 GHz.

The effects of parasitic capacitance of an inductor can be understood by looking at the self-resonant frequency. At the frequency response of a real 10-µH inductor, like the one shown in Figure 4, the self-resonant frequency is about 90 MHz. This maintains high impedance, which relates to good return loss, at just 400 MHz. Beyond this frequency, the parasitic capacitance drives the impedance down. As a result, one of the most important factors is the self-resonant frequency and its effect on the impedance over frequency when choosing an inductor.

In addition to the return loss, the user must accommodate for the saturation current of the inductor. As the current increases, the magnetic field within the core of the inductor will begin to saturate and the inductor ceases to properly remain high impedance at higher frequency. Therefore, it is important to select components with saturation currents that are greater than the anticipated PoC current.

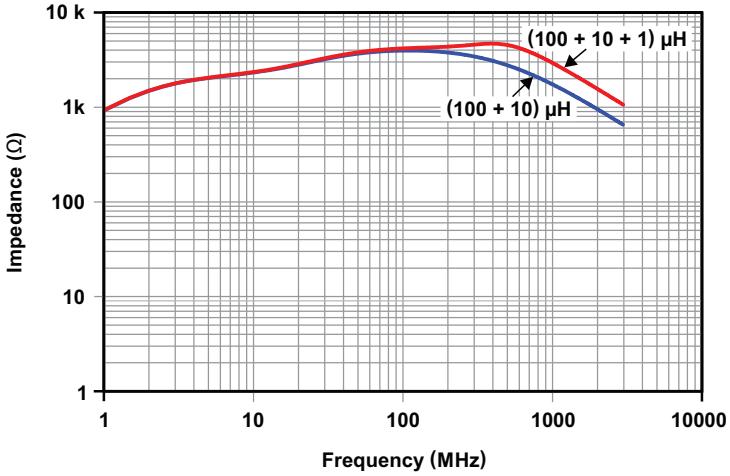

Figure 5. Impedance Plot of a Wide-Bandwidth, Cascaded Inductor Network

A wide-bandwidth inductor network can be constructed by cascading inductors of different sizes and bandwidths in series with each other. This will cover the low band, mid band, and high band of the frequency range required by BC and FC frequencies used in the 953's 4-Gbps operation shown in Figure 5. In the real application, ferrite beads and inductors with parallel resistors will cover the low, mid, and high bands. In 953 PoC systems operating at 4 Gpbs, a 10-µH inductor should take the role of the low-frequency band while ferrite beads should be used at the mid- and high-frequency bands.

Examples of inductor networks can be found in Section 3.1.

2.3 PoC Voltage

Because the required power set over coax is usually fixed, there are many benefits to decreasing the amount of current that the PoC circuit is carrying by increasing the PoC voltage.

For example, image sensors tend to have high dynamic power requirements, the Δ current draw multiplied by the DC resistance of the cable and PoC filters is translated into noise that can adversely affect both signal integrity and EMI. In addition, the inductors performance degrades as current increases and the magnetic flux in the core of the inductor gets higher. Inductors designed for higher currents tend to have heavier wire gauges and higher parasitic capacitances, leading to degraded AC performance. Furthermore, losses in the cable are lower as the current in the PoC circuit is lowered.

Once PoC voltage is increased, a high-efficiency switching regulator must be used to drop the voltage down to either the final voltage required or an intermediate voltage from which the final supply voltages can be derived.

When using PoC, a typical PoC voltage will range between 5 V and 36 V. The current must be under the rated current or saturation current spec for the ferrite beads or inductors used in the PoC network (for example, 150 mA), so TI suggests using a PoC voltage greater than 10 V.

2.4 Switcher and Sensor Generated Noise

When the sensor is operating, the sensor and the serializer will both draw current through the coax cable. The current paths are shown in Figure 6. If sharing a supply rail, TI recommends implementing a STAR connection PCB layout with separate power supply traces to the sensor and serializer to minimize the voltage supply noise coupling due to a shared resistive trace.

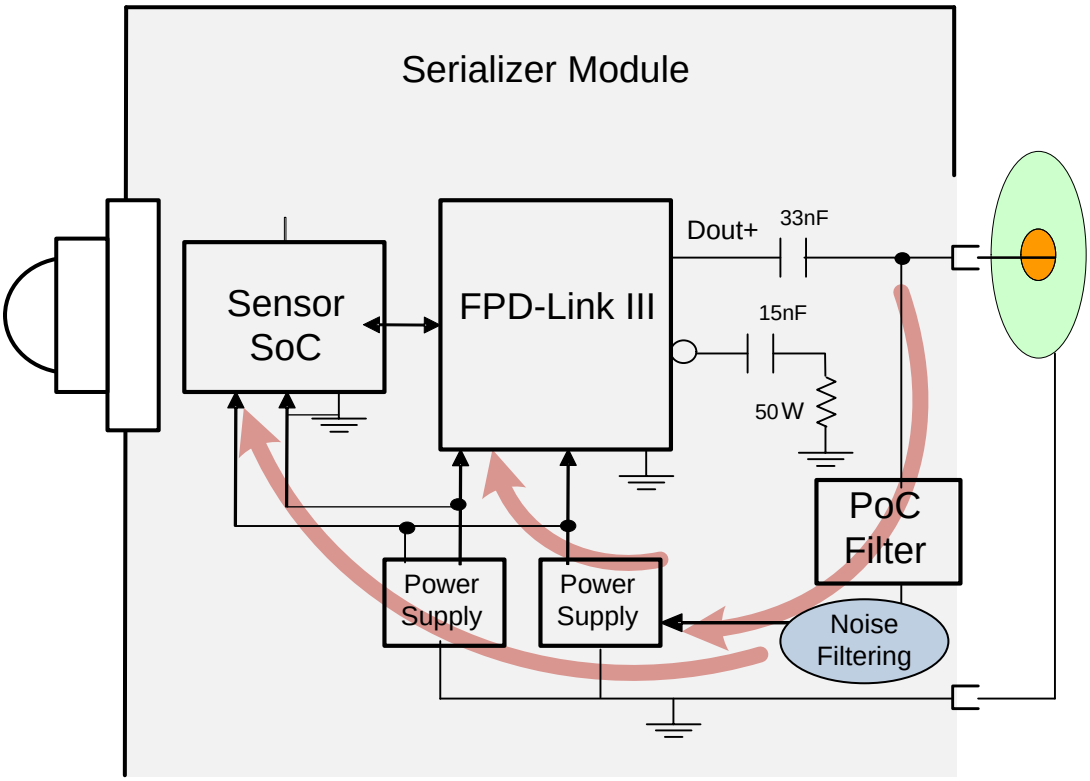

Figure 6. Sensor Current Flow

2.4.1 Switch Mode Power Supply (SMPS) Noise

The typical sensor implementation shown in Figure 6 illustrates that the system uses switching power supplies at the power feed to deliver current to the sensor module. The main power supply will generate a lower voltage subrail and minimize the power dissipation across the cable.

In designing this circuit, it is important to ensure that any switching noise present at the input to the switcher is properly filtered such that it does not feed significant ripple back to the PoC Filter input. Switching primary frequencies typically range from 500 kHz to 6 MHz, put can generate a wide spectrum of harmonics.

A large value input capacitor (≥ 10 µF) is recommended at C_{IN} with a short return path to the SMPS ground. TI also recommends keeping as much physical distance between the GND return of the Switched Mode Power Supply (SMPS) decoupling and the GND returns of the PoC filter. Additional filtering can also be incorporated at the PoC filter denoted in Figure 7 as C_{FILT}.

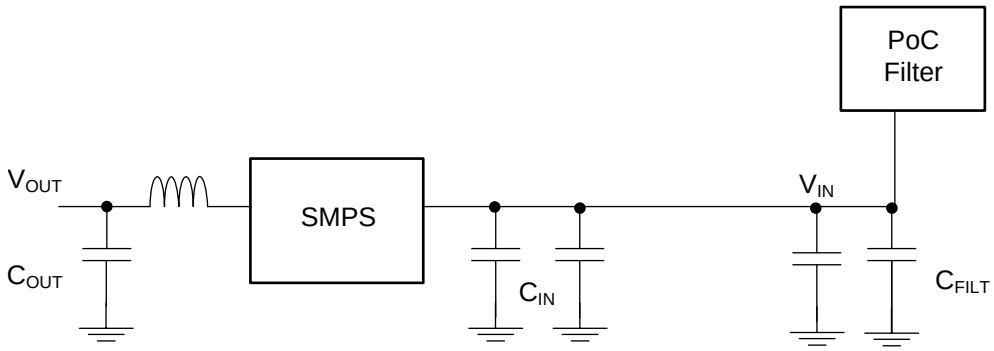

Figure 7. Switching Power Supply Filtering

2.4.2 Sensor Duty Cycle

A typical sensor System on Chip (SoC) will have periods of time, during a line transition or frame transition, when the current will be greatly reduced from the nominal power consumption. This duty cycle of higher and lower current draw from the SoC creates load transients at the power supply. This will inject noise back to the Power-over-Coax network.

The current levels can vary from as low as 20 mA in standby to over 200 mA in active mode. The frequency of the current pulses is largely determined by the line rate and frame rate set by the sensor, typically in the range of 25 to 33 kHz and 30 to 60 Hz, respectively. Any noise injected back to the input of the PoC network will appear at the Dout+ transceiver and superimpose with the received backchannel signal. The inductors in the Power-over-Coax filter are for filtering out higher frequency noise and do not provide significant rejection of frequencies below 100 kHz. The power consumption versus time is shown in Figure 8.

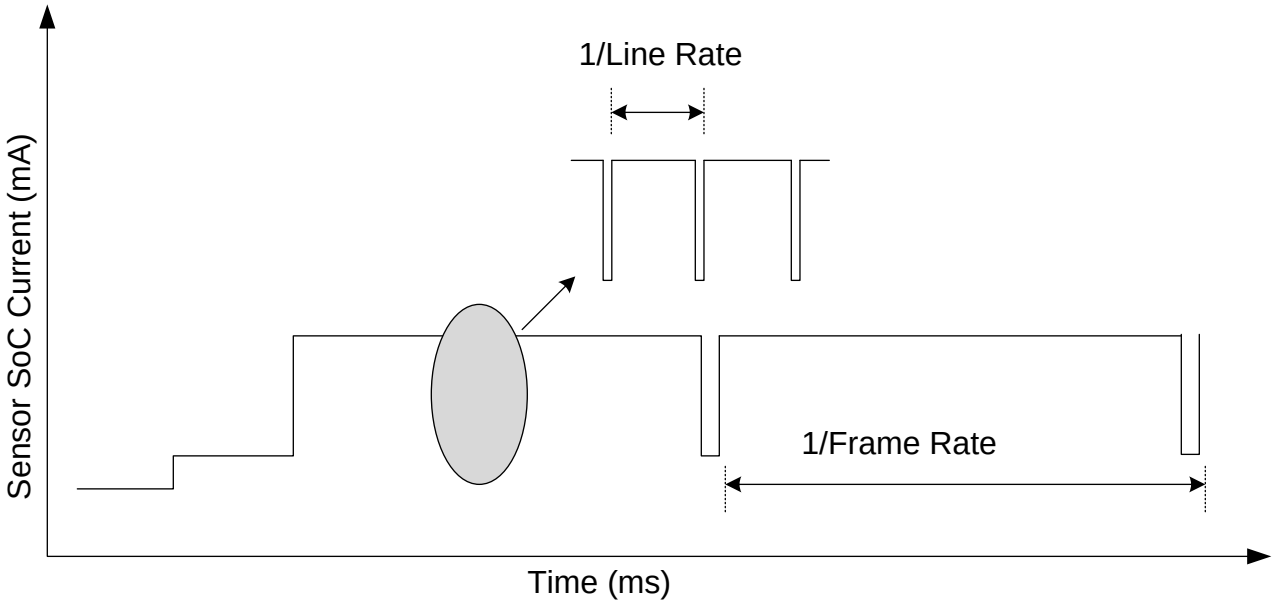

Figure 8. Sensor SoC Power Consumption vs. Time

2.5 Optimizing Decoupling of the FPD-Link III Link

To properly filter the supply noise coming over the coax cable, it is necessary to have sufficient decoupling. To address this potential impairment, TI recommends increasing the filtering capacitance value at the Power-over-Coax feed >20 µF. A typical implementation for Power-over-Coax filtering is in Figure 9. To increase filtering of any low frequency noise injected by sensor or the switcher, capacitors C2 should be 20 µF or greater, where in previous documentation the typical value is shown as 4.7 µF.

TI recommends maintaining the voltage ripple at the Dout+ input at < 25 mVp-p for optimal FPD-Link III operation. A significant noise ripple higher than 10 mVpp could start to reduce the maximum cable length across which the backchannel receiver will operate with robust BER margin. System level testing should be performed with sensor on and off to assess any impacts of power supply noise injection due to sensor operation or switching power supply under load transient conditions.

Additional decoupling at the sensor SoC or the power feed at the ECU may also be beneficial in reducing overall transient noise on the Dout+ line.

2.5.1 Considerations of Decoupling Capacitor Tolerance

In addition to selecting an automotive grade capacitor for the voltage and temperature range required, it is also important to consider several other performance factors than can impact the effective noise decoupling. Many capacitors will significantly degrade when the applied voltage is greater than the capacitor's voltage rating, sometimes as low as 20% to 40% of the nominal value. Therefore, TI recommends using a capacitor with twice the voltage rating of the intended applied voltage. Tolerance also can be ±20% for some part families. Temperature effects will also lessen the capacitor value. For example, a 4.7-µF capacitor with 10-V voltage rating that has ±10% tolerance, maintains 40% of its value at 10 V, and varies 15% at high temperature would only provide less than 1.5-µF decoupling capacitance worst case. This is shown in Equation 1 where η represents the error introduced by these effects.

$$\begin{aligned} C_{ACTUAL} &= C_{VALUE} \times \eta_{V\text{-rating}} \times (1-\eta_{Temp}) \times (1-\eta_{Tolerance}) \\ &= (4.7\ \mu) \times (0.4) \times (1-(0.15)) \times (1-(0.10)) \\ &= C_{ACTUAL} = 1.44\ \mu F \end{aligned} \quad (1)$$

3 Schematic and Layout

3.1 Schematic Examples

3.1.1 Example 1

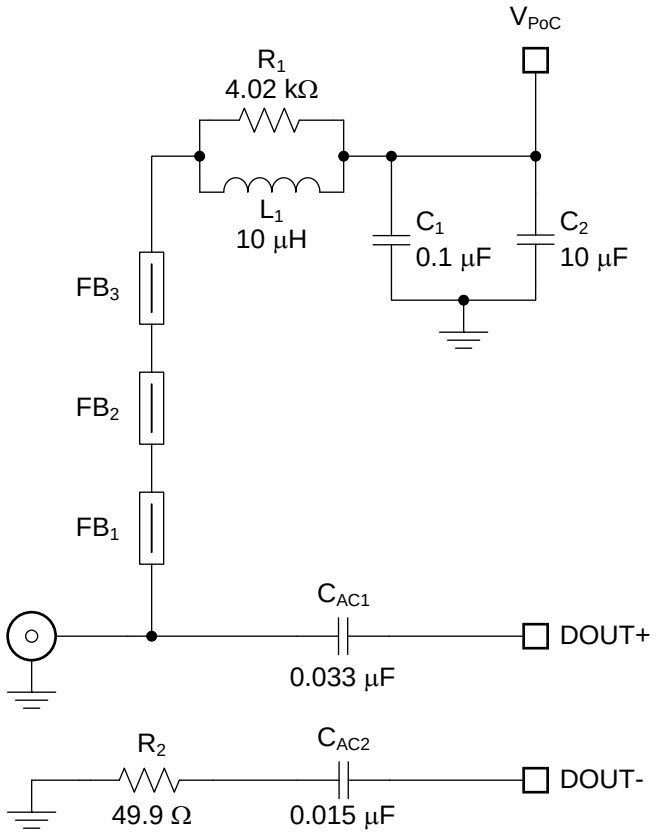

Figure 9. Typical PoC Network for a "4G" FPD-Link III

Referring to the 10-µH inductor in Figure 9, it has a self-resonant frequency of 45 MHz and maintains a high impedance up beyond 100 MHz. The ferrite bead has a high impedance at 100 MHz, and the impedance of the bead remains high well past 1 GHz. The two in series are able to provide a block to high-frequency signals across the entire frequency band of interest for the DS90UB953-Q1. The PoC current is limited by the ferrite bead which has a current limit of 250 mA—this can be accommodated by raising the PoC voltage and using an efficient switching regulator to bring the voltage down with no loss of power.

L_1 is the LQH3NPN100NGOL 10-µH inductor from Murata, and FB_1, FB_2, and FB_3 are the BLM18BD152BH1D Ferrite beads. The LQH3NPN100 has a series resonant frequency of 45 MHz, and is still providing good isolation up past 70 MHz. The BLM18BD152 has a good impedance at 100 MHz, and is still rising up until about 400 MHz when it begins to fall off, losing effectiveness above 2 GHz. By using two devices in series, 2-GHz performance can be improved. The Series DC resistance of the three components together is about 1.5 Ω. The current that this circuit can handle is limited by the ferrite beads at 250 mA.

3.1.2 Example 2

Using the same schematic as shown in Figure 9, L_1 is replaced with the ADL3225VT-100M from TDK, L_1 is replaced with the MPZ1005F47 and FB2 and FB3 is replaced the MPZ1005A331. The ADL3225VT has a self-resonant frequency of about 100 MHz, and as such, relieves some of the low-frequency burden from the ferrite beads. The MPZ1005 family of ferrite beads are 0402 components, and as such save some space over the BLM18 series components in Figure 9. However, 0402 components usually have lower the current carrying capacity—such as 400 mA. The MPZ1005F47 has excellent high-frequency performance and provides good isolation through 2.5 GHz, but leaves a gap between where the wire wound inductor falls off. The MPZ1005F47 picks up, the MPZ1005A331 fills this gap with good performance in the 100 to 500 MHz range.

3.2 Layout Tips

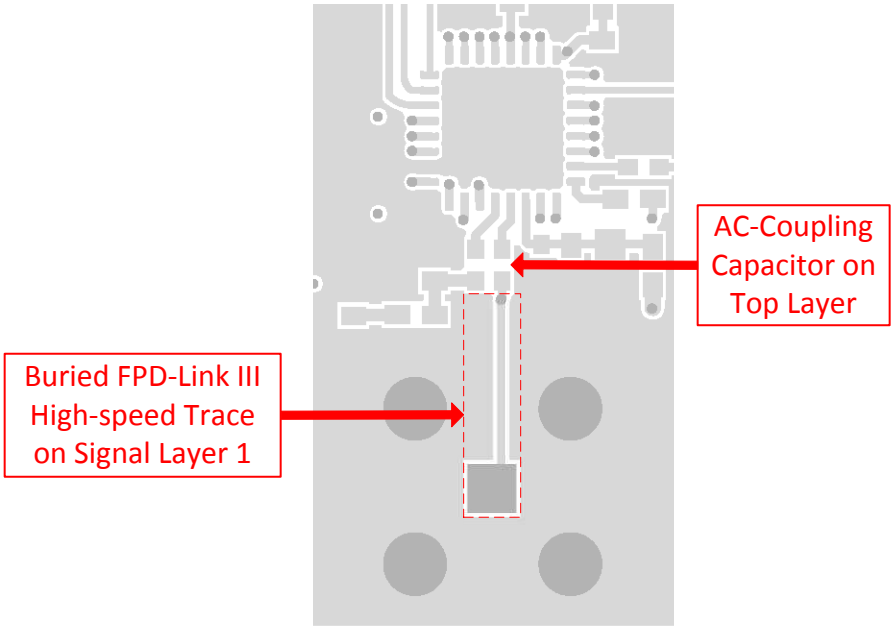

Figure 10. DS90UB953-Q1 Serializer DOUT+ Trace Layout

When using Power-over-Coax, the network will consist of ferrite beads between the FPD link and a larger inductor, and through the rest of the power network. TI recommends placing the highest frequency ferrite bead as close to the coax connector, bringing as much power into the sensor as possible. Anti-pads can be used in the PoC network to reduce parasitic capacitance that limits the bandwidth of the inductors.

Trace width should be chosen to provide 50-Ω, single-ended characteristic impedance (microstrip or stripline). Approximately 8 to 10 mils is an acceptable recommendation for the trace width. Differential traces should be at least three times greater than the trace width to avoid mutual coupling that increases Zo. There are noninverting signal terminates close to connector, so ensure that the inverting signal is extended so the traces are of equal length. In addition, avoid the stub created by through-hole connector by mounting the connector on the same side as the IC and running the trace from the bottom to the top by using a via.

4 Summary

The Power-over-Coax (PoC) capability requires the use of circuitry following certain specifications connected to both ends of the cable. These specifications include impedance versus frequency characteristics and return loss. The PoC circuit must have low impedance at DC but as to not interfere with the data path, the characteristic impedance must be large over the band of the forward channel and back channel, 20 MHz to 2 GHz, compared to the 50-Ω impedance of the coax line.

The critical consideration is the return loss profile after adding the Power-over-Coax (PoC) network. Limits on return loss make sure that the impedance of the PoC network is high enough that high speed path signal integrity is maintained. The PoC network offers low impedance at DC to allow for efficient power transfer to the DC/DC powering the serializer and the camera; in addition, offering high impedance at the frequencies the data is being transferred. Depending upon the current consumption of the camera and serializer board, there could be up to 250 mA of current going through the network. As a result, the PoC network components must be selected to ensure that they do not saturate at these current levels by checking the inductor current limits before finalizing components. A good starting point for the PoC network for providing high impedance at the high frequencies is to use the recommended network in the EVM schematic.

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