Application Report
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DP83822 Energy Efficient Ethernet IEEE 802.3az

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ABSTRACT

The DP83822 was designed to meet the needs of rugged and high performance applications while still offering a wide range of options for minimizing power consumption. This application note will discuss how the DP83822 Energy Efficient Ethernet feature works and how to implement Energy Efficient Ethernet.

Contents

1 Introduction

The DP83822 10/100Mbps Industrial Ethernet PHY offers a wide range of power saving modes that can be applied individually or in combination with each other depending on the desired operation. Supported low power modes include:

- Energy Efficient Ethernet – IEEE802.3az
- Wake-on-LAN
  - Magic Packet Detection
  - Magic Packet Detection with Secure-ON
  - Custom Packet Detection
- Low Power Sleep Modes
  - Passive Sleep
  - Active Sleep
- IEEE Power Down
- Deep Power Down

This application note will discuss EEE.

Table 1. Terminology

Acronym	Defintion
DUT	Device Under Test
MAC	Media Access Controller
LP	Link Partner
EEE	Energy Efficient Ethernet
WoL	Wake-on-LAN
Opcode	Operation Code
PHY	Physical Layer Transceiver
SMI	Serial Management Interface
IPG	Inter-Packet Gap
LPI	Low-Power Idle
NLP	Normal Link Pulse
TX	Transmit – Digital Pins
RX	Receive – Digital Pins
TD	Transmit – Analog Pins
RD	Receive – Analog Pins

2 Energy Efficient Ethernet

This section discusses the principles behind EEE and implementation of EEE.

2.1 EEE – Principles of Operation

Energy Efficient Ethernet (EEE) is a mechanism by which current consumption is lowered during periods of low packet traffic. The MAC and PHY must both support EEE functionality since EEE is an IEEE standard (IEEE802.3az) that governs both Layer 1 and Layer 2 operations.

Note: 10 Mbps EEE is achieved using only signal amplitude reduction and does not require any negotiation with a Link Partner (LP) or require MAC-PHY handshaking. 10BASE-T and 10BASE-Te only send link pulses during IPG, unlike 100 Mbps and 1000 Mbps operation where there is a constant stream of IDLES between frames.

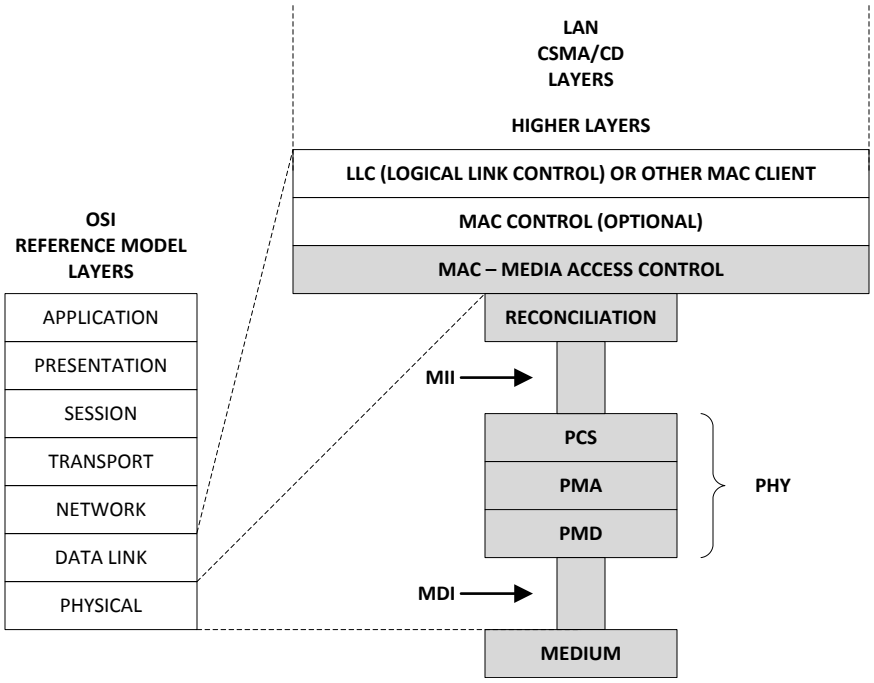

Figure 1. IEEE802.3az relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE802.3 CSMA/CD LAN model

100BASE-TX sends IDLES during the Inter-Packet Gap (IPG). These IDLES allow the PHY to maintain signal equalization and link status. The DUT and the LP also use IDLEs to recover the other device's transmit clock for their own internal recovered clock. The PHYs constantly send IDLEs even when no traffic is present, current consumption is high because the line drivers are always active. EEE helps minimize current consumption by allowing quiet periods during Low-Power Idle (LPI) operation.

LPI consists of a five main states: Active, Sleep, Quiet, Refresh and Wake. However the simplified diagram shown in Figure 2, with just Active, Low-Power and Wake is also acceptable.

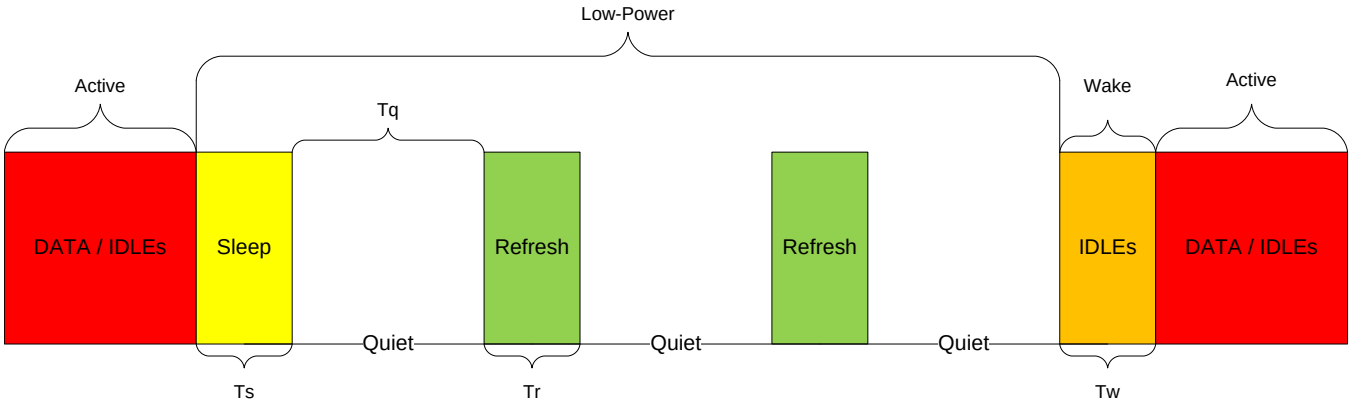

Figure 2. EEE LPI State Flow

Table 2. EEE LPI Timing

Line State	Symbol	Timing Parameter (Transmit)	Timing Parameter (Receive)	Line Signals
SLEEP	Ts	200 µs – 220 µs	240 µs - 260 µs	4B5B code-group /P/
QUIET	Tq	20 ms – 22 ms	24 ms – 26 ms	Differential DC zero volt
REFRESH	Tr	200 µs – 220 µs	240 µs - 260 µs	4B5B code-group /P/
WAKE	Tw	30 µs – 36 µs	30 µs - 36 µs	4B5B code-group /I/

A PHY transitions into the Low-Power state when the MAC asserts EEE LPI opcode on the TX PHY MAC pins. Periodic Refresh, a series of Sleep code-groups, is required to ensure link, maintain PLL lock (clock recovery) and signal equalization. When the MAC requests that the PHY exit LPI, IDLE code-groups will persist to inform the link partner that the device is transitioning into an active state.

Table 3. Transmit Opcodes

TX_EN	TX_ER	TXD[3:0]	Function
0	0	0000 through 1111	Normal Inter-Frame
0	1	0	Reserved
0	1	1	EEE LPI
0	1	0010 through 1111	Reserved
1	0	0000 through 1111	Data Transmission
1	1	0000 through 1111	Transmit Error

Table 4. Receive Opcodes

RX_DV	RX_ER	RXD[3:0]	Function
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000	Normal Inter-Frame
0	1	0001	EEE LPI
0	1	0010 through 1111	Reserved
0	1	1110	False Carrier Indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal Data Reception
1	1	0000 through 1111	Data Reception with Errors

Once the MAC initiates the LPI request by presenting the EEE LPI opcode on the TX pins, the PHY is responsible for providing the correct 4B5B code-group that is used to inform the LP that it is going to enter into a Quiet state. When the LP receives the Sleep request, the LP is responsible for informing its MAC through the receive pins that LPI is to be initiated by the DUT.

Table 5. 4B5B Code-Groups

PCS code-group [4:0] 4 3 2 1 0	Name	MII (TX[3:0]/RX[3:0]) 3 2 1 0	Interpretation
1 1 1 1 0	0	0 0 0 0	Data 0
0 1 0 0 1	1	0 0 0 1	Data 1
1 0 1 0 0	2	0 0 1 0	Data 2
1 0 1 0 1	3	0 0 1 1	Data 3
0 1 0 1 0	4	0 1 0 0	Data 4
0 1 0 1 1	5	0 1 0 1	Data 5
0 1 1 1 0	6	0 1 1 0	Data 6
0 1 1 1 1	7	0 1 1 1	Data 7
1 0 0 1 0	8	1 0 0 0	Data 8
1 0 0 1 1	9	1 0 0 1	Data 9
1 0 1 1 0	A	1 0 1 0	Data A
1 0 1 1 1	B	1 0 1 1	Data B
1 1 0 1 0	C	1 1 0 0	Data C
1 1 0 1 1	D	1 1 0 1	Data D
1 1 1 0 0	E	1 1 1 0	Data E
1 1 1 0 1	F	1 1 1 1	Data F
1 1 1 1 1	I	Undefined	IDLE
0 0 0 0 0	P	0 0 0 1	SLEEP; Low-Power Idle
1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter; Part 1 of 2
1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter; Part 2 of 2
0 1 1 0 1	T	Undefined	End-of-Stream Delimiter; Part 1 of 2
0 0 1 1 1	R	Undefined	End-of-Stream Delimiter; Part 2 of 2
0 0 1 0 0	H	Undefined	Transmit Error
0 0 0 0 1	V	Undefined	Invalid code
0 0 0 1 0	V	Undefined	Invalid code
0 0 0 1 1	V	Undefined	Invalid code
0 0 1 0 1	V	Undefined	Invalid code
0 0 1 1 0	V	Undefined	Invalid code
0 1 0 0 0	V	Undefined	Invalid code
0 1 1 0 0	V	Undefined	Invalid code
1 0 0 0 0	V	Undefined	Invalid code
1 1 0 0 1	V	Undefined	Invalid code

Figure 3 and Figure 4 show the progression of states for both transmit and receive paths when EEE LPI is enabled. Notice that at any point in the LPI state machine, a PHY can quickly exit out of the Low-Power mode and enter into an Active mode.

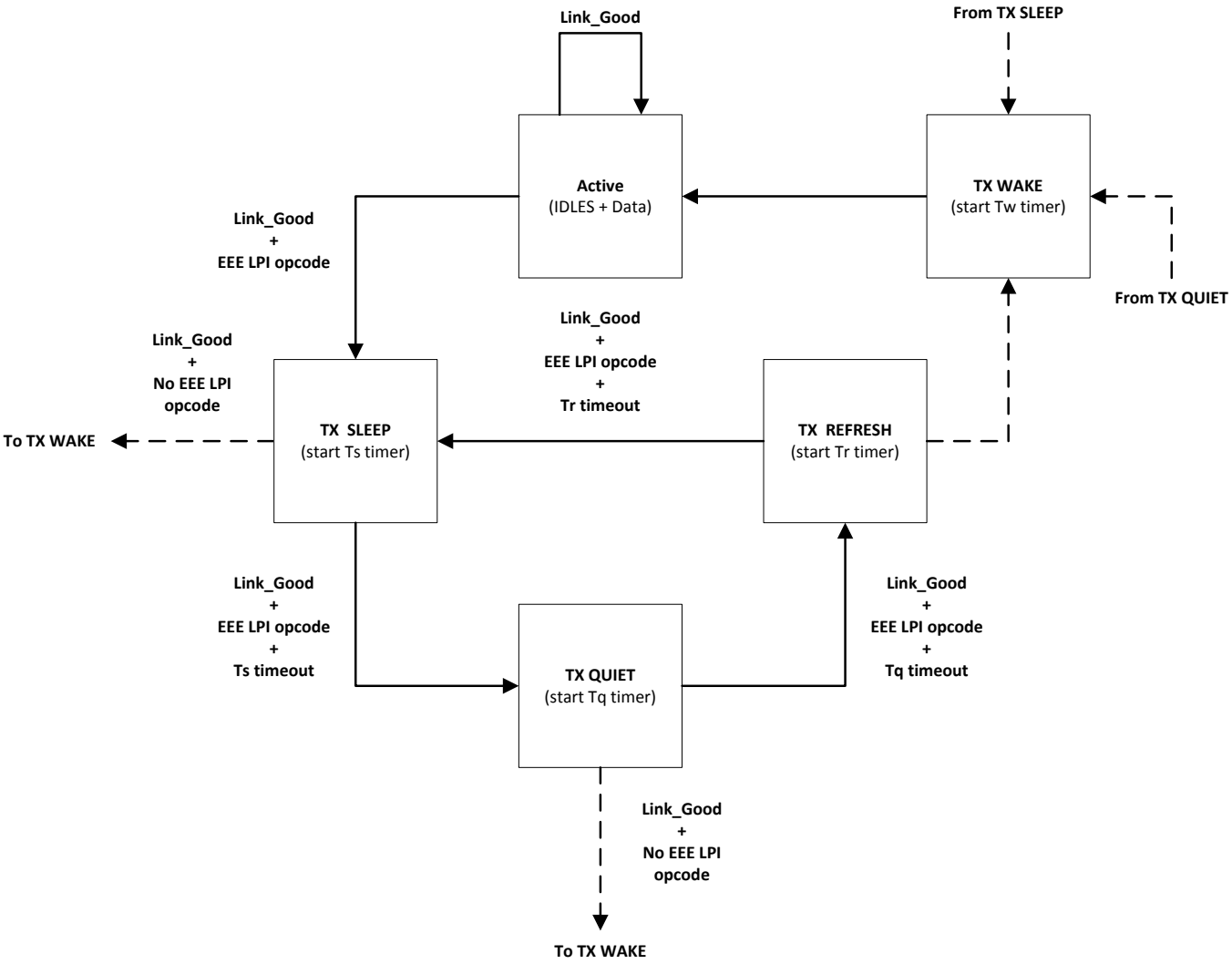

Figure 3. Transmit Path LPI State Diagram

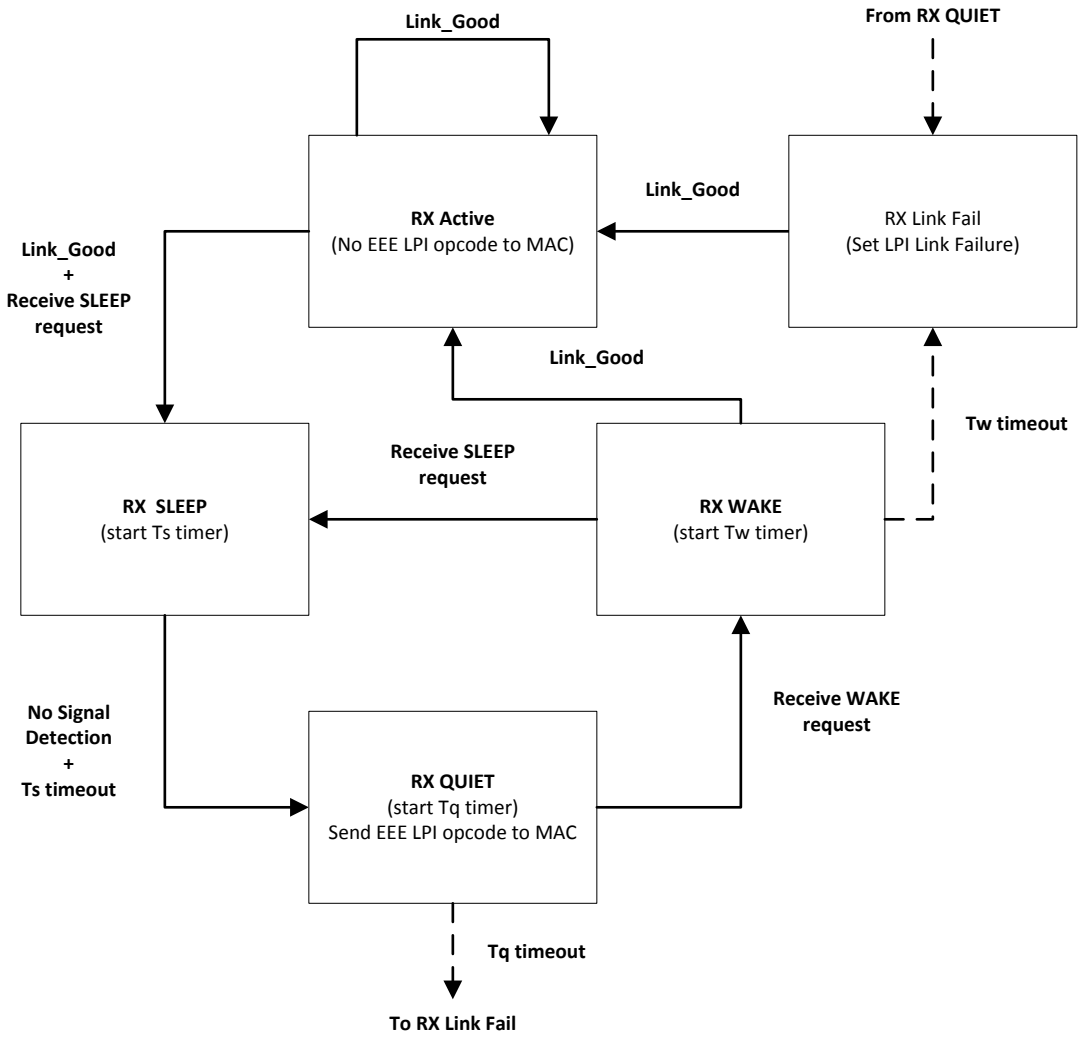

Figure 4. Receive Path LPI State Diagram

During Auto-Negotiation, PHYs capable of EEE operation at 100 Mbps speed advertise their abilities to inform their LPs. The exchange of abilities is part of NEXT PAGE advertisement. The control and status bits for EEE are found in MMD3 and MMD7 registers in the PHY's extended register set. Once both partners acknowledge EEE supported abilities, links can operate in any one of four combinations described in Figure 5, Figure 6, Figure 7 and Figure 8 for 100BASE-TX operation.

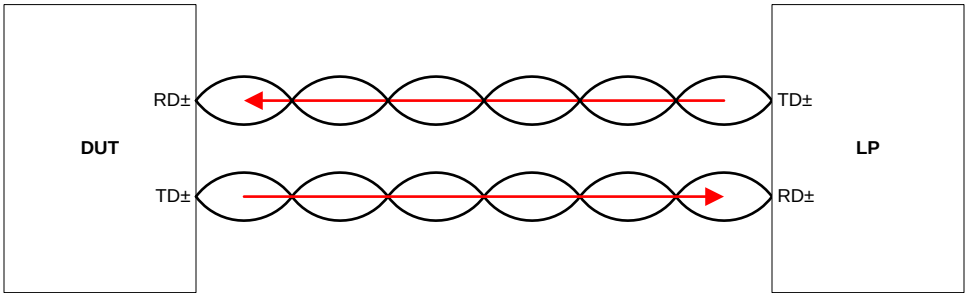

Figure 5. Both Active

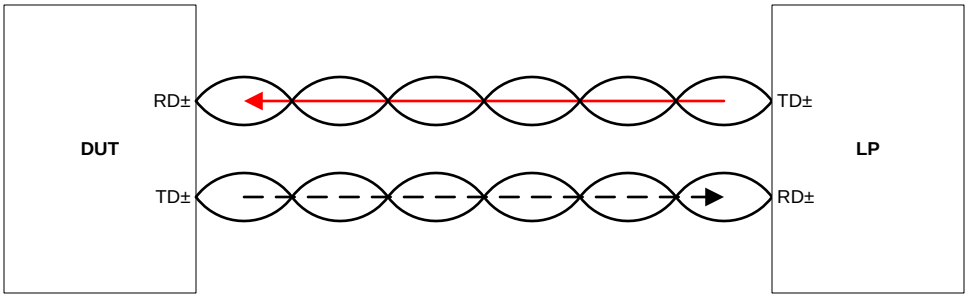

Figure 6. LP Active and DUT in LPI

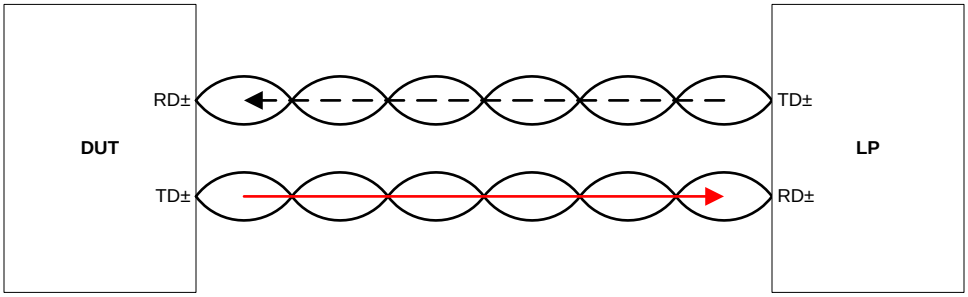

Figure 7. LP in LPI and DUT Active

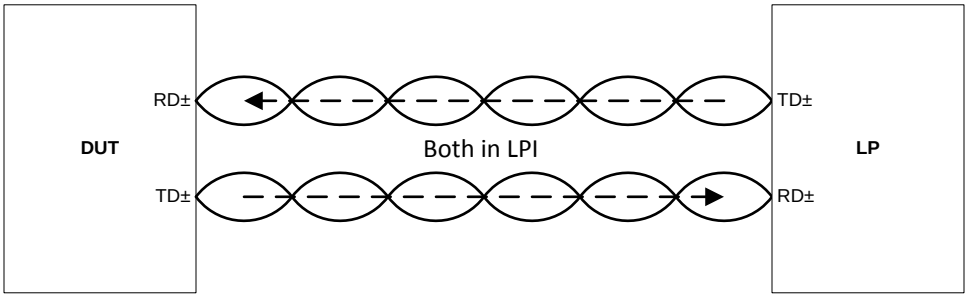

Figure 8. Both in LPI

Additionally, TX_CLK and RX_CLK can be stopped during LPI operation. Since TX and RX opcodes are static during LPI operation, there is no need to continually clock the digital signals. Power is lowered further by stopping these digital pins from toggling.

Note: MII only allows RX_CLK to be stopped since TX_CLK is an output from the PHY and is necessary to clock in the correct opcode. RGMII allows for both TX_CLK and RX_CLK to be stopped since RX_CLK is an output from the PHY and TX_CLK is an output from the MAC.

2.2 EEE - Implementation

EEE can be enabled through two different methods: hardware bootstrap and register configuration using the SMI.

2.2.1 Bootstrap Method

During RESET (either through power-cycle, RESET_N pin activation or using bit [15] in the Basic Mode Control Register; register 0x001F), the DP83822 will configure all digital pins to tri-state for over 100 ms. During this time period, external or internal resistors on specified bootstrap pins will pull the pin to a desired voltage state. An internal comparator samples the state of each bootstrap pin and will configure the PHY to its intended function.

RX_D1 (pin #31) is a dual purpose bootstrap pin, responsible for PHYAD_2 and EEE_EN bootstrap functions. Dual purpose bootstrap pins have four strap modes; Mode 1 through Mode 4. A default mode is assigned to each pin by use of weak internal pull resistors. RX_D1 is by default Mode 1 and has the following configuration:

Table 6. Bootstrap Mode 1

Bootstrap Name	Setting	Function
PHYAD_2	0	PHY Address bit [2] is ‘0’
EEE_EN	0	Energy Efficient Ethernet is Disabled

Only strap Mode 2 and Mode 3 will enable EEE advertisement functionality. The purpose for two modes to support EEE advertisement is because it allows for two different PHYAD_2 fields to support EEE as well. The following two configurations support EEE:

Table 7. Bootstrap Mode 2

Bootstrap Name	Setting	Function
PHYAD_2	0	PHY Address bit [2] is ‘0’
EEE_EN	1	Energy Efficient Ethernet is Enabled

Table 8. Bootstrap Mode 3

Bootstrap Name	Setting	Function
PHYAD_2	1	PHY Address bit [2] is ‘1’
EEE_EN	1	Energy Efficient Ethernet is Enabled

2.2.2 Register Configuration Method

Additionally, EEE advertisement can be enabled using register configuration. The DP83822 offers two methods for enabling EEE advertisement depending on user preference.

The typical method is through MMD3 and MMD7 extended register sets. These register maps are only accessible when the correct Device Address (DEVAD) Register Control is used. DEVAD is found in register 0x000D (REGCR) bits [4:0]. Vendor specific DEVAD cannot access MMD3 and MMD7 extended register sets. The DP83822 uses the vendor specific DEVAD [4:0] = '11111' for accesses to register 0x04D1 and lower. For MMD3 access, the DEVAD [4:0] = '00011'. For MMD7 access, the DEVAD [4:0] = '00111'.

To configure the DP83822 for 100BASE-TX EEE Advertisement, use the following register write steps:

Table 9. EEE 100BASE-TX Advertisement Configuration Steps

Step	Register	Value	Description
1	000D	0007	Access MMD7 through REGCR
2	000E	003C	Access Register 0x003C in MMD7
3	000D	4007	Write to Register 0x003C with no Post Increment
4	000D	0002	Advertise 100BASE-TX EEE
5	0000	3300	Restart Auto-Negotiation

The DP83822 has an added feature that allows for EEE advertisement using the vendor specific DEVAD. Register 0x04D1 is a DP83822 vendor specific register that has the ability to bypass MMD3 and MMD7 extended registers. This feature allows for a simpler driver control since it allows for a single DEVAD to be used.

To configure the DP83822 for 100BASE-TX EEE Advertisement with vendor specific register 0x04D1, use the following register write steps:

Table 10. EEE 100BASE-TX Advertisement Vendor Specific Configuration Steps

Step	Register	Value	Description
1	04D1	018F	Advertise 100BASE-TX EEE
5	0000	3300	Restart Auto-Negotiation

2.2.3 EEE – DP83822 Waveform

For reference, the DP83822 Eye diagram is shown in Figure 9. This was achieved by forcing the DP83822 into 100 Mbps with Auto-MDIX disabled. Upper and lower horizontal cursors are enabled to provide the IEEE802.3u min/max PMD amplitude limits.

Note: All images are using Tektronix FastAcq with positive edge trigger.

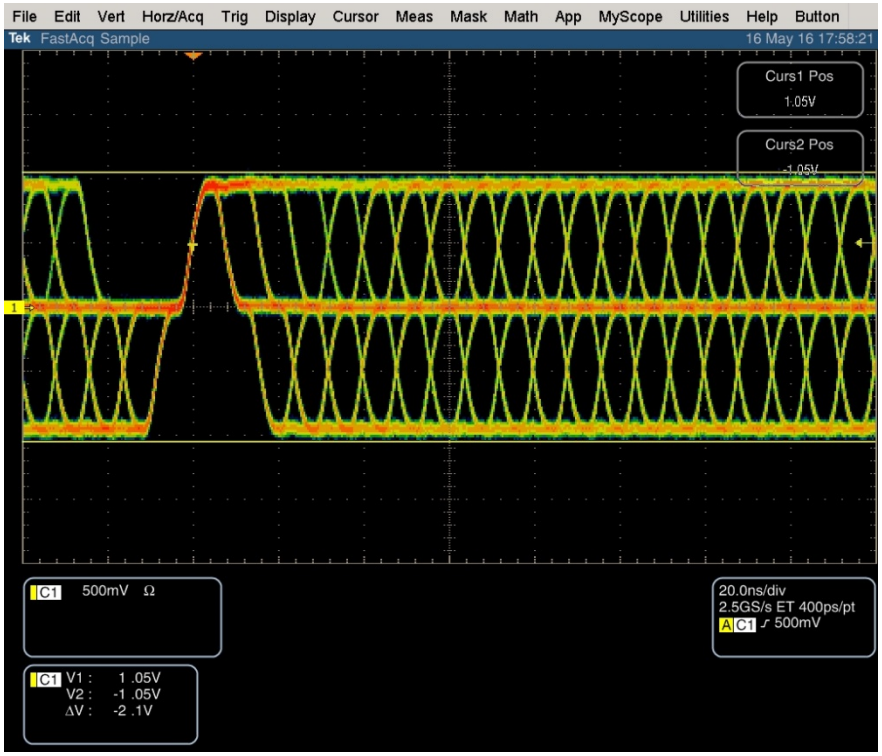

Figure 9. DP83822 Eye Diagram

A constant stream of IDLEs can be seen, which is expected for 100 Mbps operation as described in Section 2.1. There are three distinct levels to 100BASE-TX MLT-3 signaling; +1, 0 and -1. MLT-3 when viewed with variable persistence or infinite persistence will result in this stacked eye waveform.

An image of the DP83822 Refresh can be seen in Figure 10. Upper and lower horizontal cursors are enabled to provide the IEEE802.3 min/max PMD amplitude limits. The positive edge trigger provides the starting reference point for the Refresh burst and a vertical cursor is placed on this location (t1). A second vertical cursor is placed at the end of the Refresh burst (t2). Total Refresh burst time is 212 μs. This is well within the 200 μs – 220 μs Refresh burst time limits.

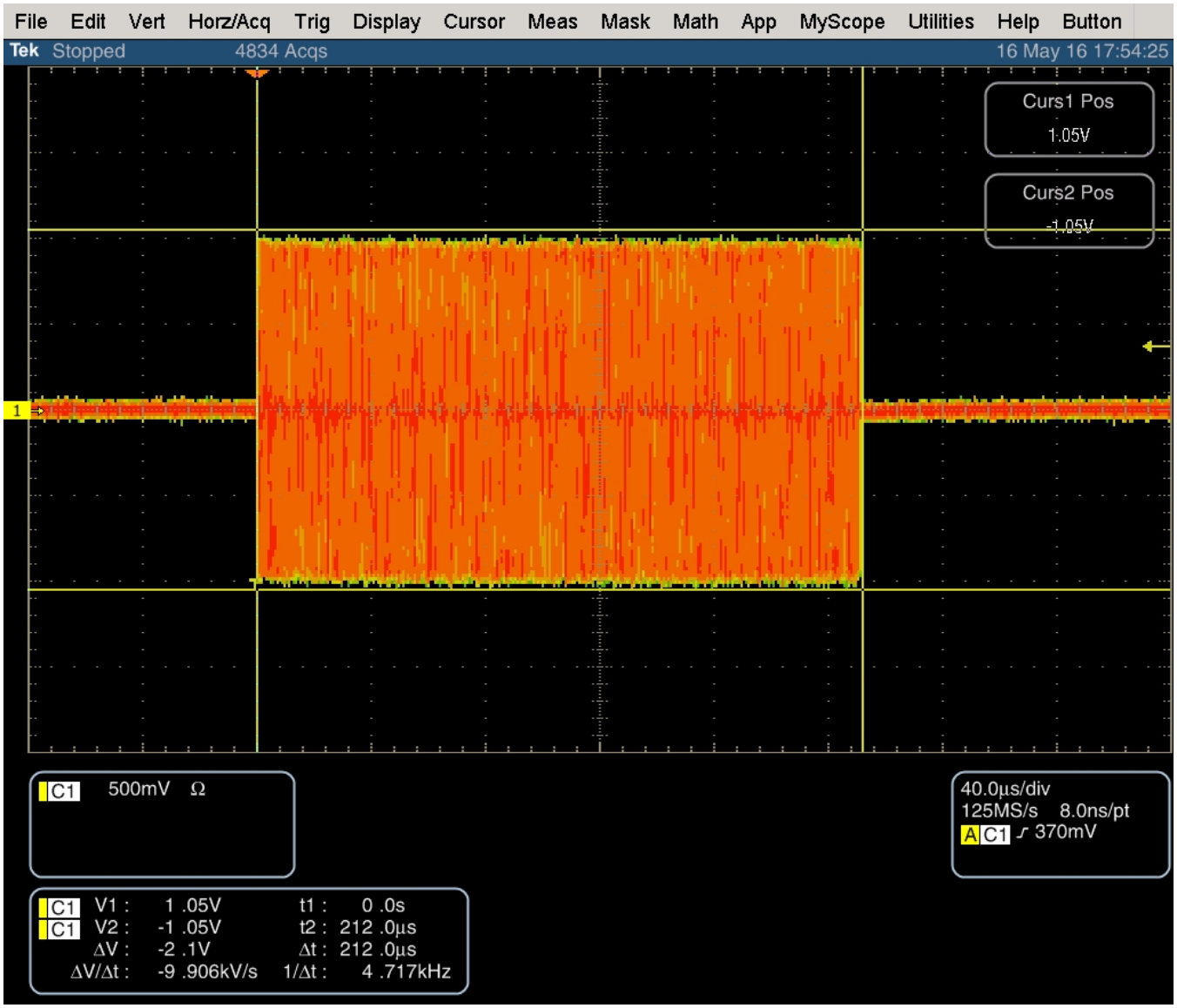

Figure 10. Refresh Burst

Zoomed out views of DP83822 Refresh bursts can be seen in Figure 11 and Figure 12. The first image shows two Refresh bursts with horizontal and vertical cursors to show the IEEE limits described above. A vertical cursor is placed on the rising edge of the first Refresh burst (t1). The second vertical cursor is placed on the rising edge of the second Refresh burst (t2). The Quiet period is 22 ms. The DP83822 is configured for the maximum allowable quiet time, which provided the most energy savings.

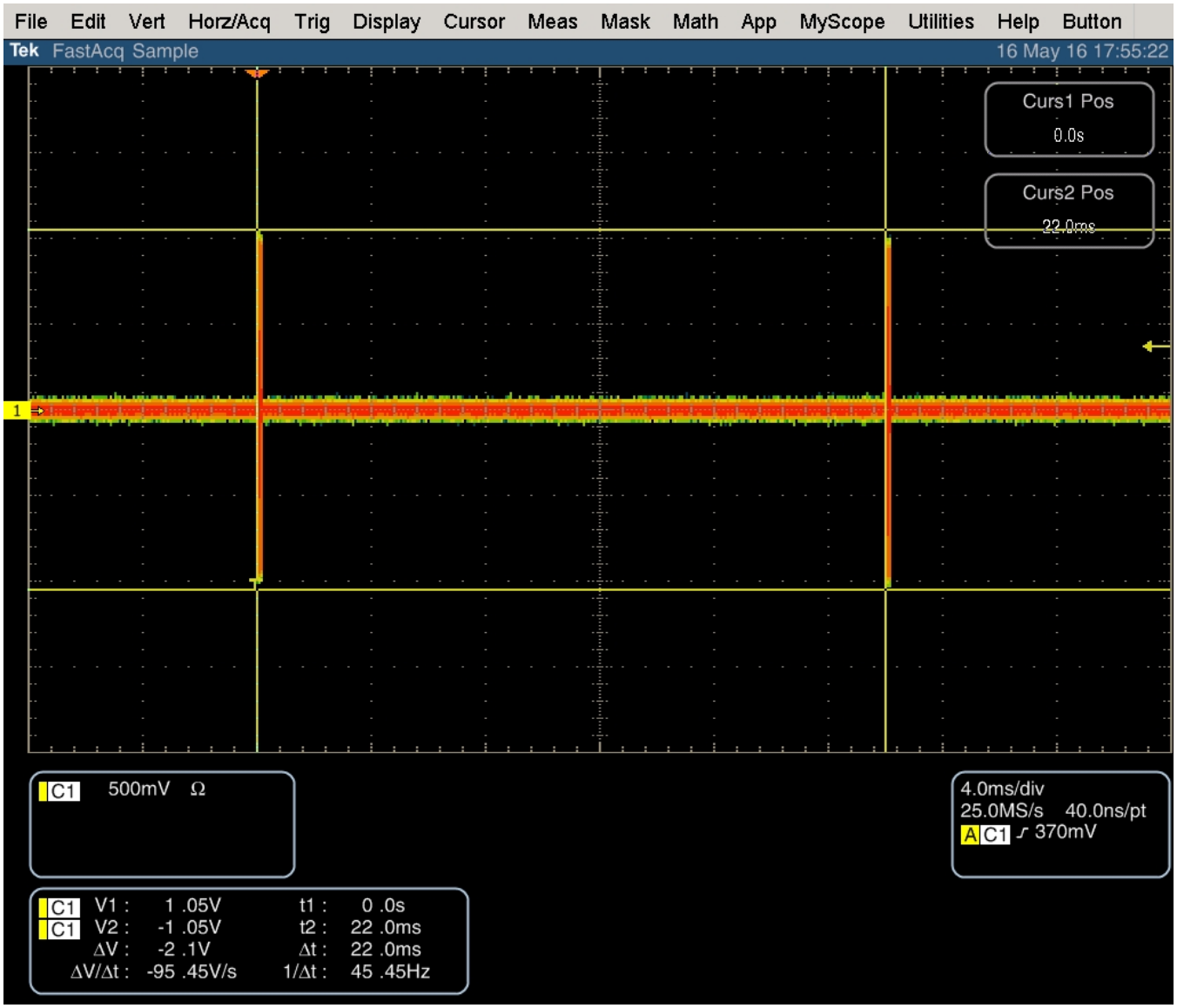

Figure 11. Two Refresh Bursts with Quiet Period

The second image shows four Refresh bursts with horizontal and vertical cursors to show the IEEE limits described above. A consistent Refresh burst is critical for maintaining quality link. DP83822 consistent timers can be seen in Figure 12. Again, a vertical cursor is placed on the rising edge of the first Refresh burst (t1). The second vertical cursor is placed on the rising edge of the second Refresh burst (t2). The Quiet period is 22 ms. All subsequent Quiet periods are 22 ms as well.

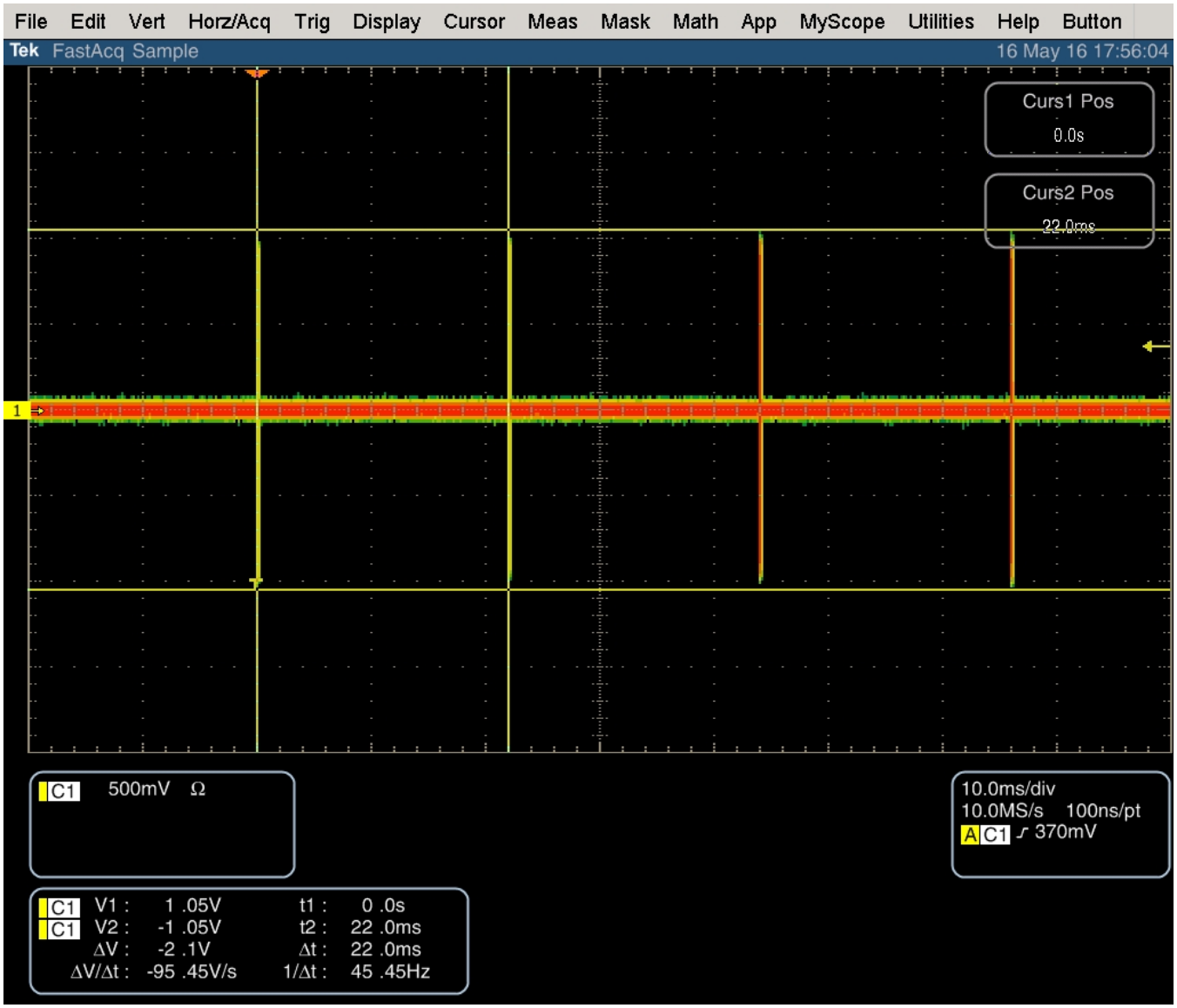

Figure 12. Four Refresh Bursts and Three Quiet Periods

3 Conclusion

This application note provided details on the principles behind EEE and the mechanisms to enable EEE in the DP83822.

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