Application Report
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KSZ9031RN to DP83867CR/CS/E/IR/IS System Rollover

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ABSTRACT

This application report outlines the necessary and potential steps for replacing the Micrel KSZ9031RN 10/100/1000 Mb/s Ethernet PHY with TI's DP83867CR/CS/E/IR/IS.

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1 Purpose

While both products have many similarities, DP83867 offers several features that improve performance and offer greater system customization. This system rollover document outlines how to replace the Micrel KSZ9031RN PHY with TI's DP83867CR/CS/E/IR/IS by comparing differences including required external components, pin functions, feature set, and register operation. The impact to a design is dependent on PHY configuration and features used.

2 Required Changes

This section describes the hardware/circuit modification required to transition from using the Micrel KSZ9031RN to TI's DP83867.

2.1 Package

The KSZ9031RN is only available in the 48 pin QFN package. DP83867 is available in a 48-pin QFN package as well as a 64-pin QFP (GMII only compatible with DP83867IR QFP and SGMII only compatible with DP83867CS/E/IS). There is no difference in the physical size and pin count of the QFN package between the DP83867 and KSZ9031RN, as shown in *Table 1*.

Table 1. Packaging Differences

	DP83867CS/CR/E/IS	DP83867IR	KSZ9031RN
Package	48-QFN	48-QFN/ 64-QFP	48-QFN
Footprint	7x7mm	7x7mm/ 12x12mm	7x7mm

2.2 Pinout

Both the KSZ9031RN and the DP83867CS/CR/E/IR/IS have 48 pins in QFN package while DP83867IR also supports 64-QFP Package. Please see Appendix A for the pin mapping between the KSZ9031RN and the DP83867, as well as pins not applicable for the DP83867.

2.3 Bias Resistor

Internal circuitry biasing between the devices is accomplished in a similar manner. The only difference is the value of the bias resistor and the bias connector pin.

DP83867 uses 11 kΩ (±1%) on pin 12 in QFN package or pin 15 in QFP package.

KSZ9031RN uses 12.1 kΩ (±1%) on pin 48.

Table 2. Bias Resistor Values

	DP83867	KSZ9031RN
Bias Resistor Value	11 kΩ	12.1 kΩ
Pin Number	12(QFN) / 15(QFP)	48

2.4 Strapping Configuration

DP83867 strap options allow configuring PHY address, Auto-Negotiation enable, RGMII clock skew, Mirror enable, SGMII enable, and speed select. DP83867 uses a 4-level strap option for configuration during hardware reset. Do not connect directly to VCC or GND since strap pins may have alternate functions after reset is deasserted.

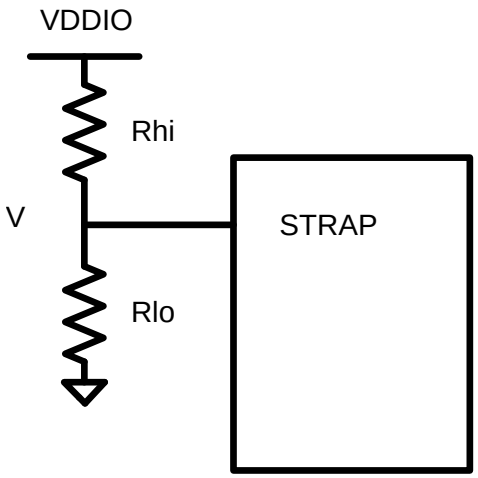

Figure 1. DP83867 Strapping Configuration

For specific strap options, please refer to the *Strap Configuration* section of the DP83867IR/CR data sheet or the DP83867E/IS/CS data sheet.

Micrel KSZ9031 uses strapping options with only pull-up or pull-down options (2 levels). Strap options for KSZ9031 allow configuring PHY address, PHY “mode” (as outlined in KSZ9031 data sheet), 125-MHz CLK output, and single vs. Tri-color dual LED mode.

See the KSZ9031RN data sheet for the specific strapping configurations.

2.5 MDIO Pull-Up Resistor

DP83867 requires a pull-up resistor on MDIO pin 17 (QFN) or pin 21 (QFP) for SMI/MIIM interface. The recommended value is 2.2 kΩ. KSZ9031RN has an internal pull-up resistor for MDIO.

2.6 LEDs

2.6.1 LED Modes

The DP83867 LED operation mode can be selected using the LEDCR1 register (address 0x0018).

KSZ9031RN LED Mode is determined by the strap of pin 41 to either Single-LED or Tri-Color dual-LED mode (pull-up and pull-down respectively). LED indication in each mode can be found in the KSZ9031RN data sheet.

2.6.2 LED Circuits

Because of the 4-option strapping of DP83867, the LED circuits must be reconfigured from the KSZ9031RN depending on PHY configuration.

For DP83867 the LED output pins are also used as straps, the external components required for strapping and LED usage must be considered in order to avoid contention. If the input is resistively pulled high then the corresponding output should be an active low driver otherwise the output should be an active high driver. LED circuits should be configured accordingly. It is recommended to operate the LED from higher supply as operating from 1.8V supply will result in dim LEDs. Example configuration is provided in the *LED Configuration* section of the DP83867IR/CR data sheet or the DP83867E/IS/CS data sheet DP83867E/IS/CS data sheet.

2.7 Power Configurations

The DP83867 can be operated in two or three supply mode with the option of a separate VDDIO supply (for digital and analog isolation).

When operating in three supply mode, it is highly recommended to first power the 1.8-V supply. There is no sequencing requirement for other supplies in three supply mode. There is no sequencing requirement for two supply mode. Refer to the *Power Supply Recommendations* section of the DP83867IR/CR data sheet or the DP83867E/IS/CS data sheet for configuration diagram.

KSZ9031RN has four power configurations with varying analog and digital supplies:

- Transceiver: 3.3 V or 2.5 V
- Digital I/O: Transceiver Voltage (3.3 V / 2.5 V) or 1.8 V
- Core: 1.2 V

The KSZ9031RN uses an external MOSFET for the on-chip LDO controller. DP83867 does not require this MOSFET.

3 Potential Changes

The following section describes the specific changes that may need to be changed in converting to a DP83867 design. The default values for the DP83867 vs. KSZ9031RN may be enough for transition between parts.

3.1 Power Up Timing

DP83867 has RESET_N set high (active low) with supply voltage power up, while KSZ9031RN has RESET_N set high with strap option latching. Because of the KSZ9031RN RESET_N required delay from power up, an external circuit is recommended. DP83867 does not require such a circuit. See the DP83867IR/CR data sheet or the DP83867E/IS/CS data sheet for in-depth power-up/power-down timing. Hardware and software resets can also be set using control register 0x0000 (IEEE 802.3 standard).

3.2 RGMII Internal Delay

Both DP83867 and KSZ9031 provide configurable internal clock skew for the GTX_CLK and RX_CLK to optimize timing across the interface. KSZ9031RN also allows individual pad skew for all RGMII signals, however not necessary for proper timing. DP83867 must be configured to “Shift” mode by setting RGMII Control Register (0x0032).

DP83867 also allows for both transmit and receive RGMII internal skew to be configured via strapping options for 8 configurations.

KSZ9031RN defaults to RX_CLK being delayed about 1.2 ns with respect to RX_DV and RXD[3:0]. GTX_CLK is not delayed with respect to the TX signals (MAC induced skew expected). DP83867 relies on strapping options for default RGMII delay options.

3.3 Integrated Termination Resistors

DP83867 offers programmable termination impedance for MII/GMII/RGMII interface and integrated MDI termination resistors. These features allow the removal of external series termination resistors. See register 0x0170 in the DP83867IR/CR data sheet or the DP83867E/IS/CS data sheet for termination impedance setting.

3.4 PHY Address

The DP83867 and KSZ9031RN have a default strap for PHY address 0x0000. However both can be strapped to another PHY address by adding pull-up or pull-down resistors to appropriate pin(s). Refer to the *Strap Configuration* section of the DP83867IR/CR data sheet or the DP83867E/IS/CS data sheet for details.

3.5 Physical Layer ID Register

The PHY Identifier Register #1 (PHYIDR1) and #2 (PHYIDR2) allow system software to determine applicability of device specific software based on the vendor model number. The vendor model number is represented by bits 9 to 4 in PHYIDR2. The vendor model number of DP83867 is 0x080028. For KSZ9031RN, the vendor model number is 0x0010A1.

Table 3. PHYID Comparison

Register Address	Register Name	Register Description	Device	
			DP83867	KSZ9031RN
0x03	PHYIDR2	PHY ID 2	0x080028	0x0010A1

3.6 MDIO Register Writes

The DP83867 and Micrel KSZ9031 have both standard and extended SMI/MIIM (MDIO) registers.

DP83867 can access the standard registers through the indirect method (using standard registers 0x000D and 0x000E as outline in IEEE 802.3). However, Micrel KSZ9031RN can only access the standard register set through the direct method (without using 0x000D and 0x000E registers).

Micrel KSZ9031RN also specifies the MMD address for all extended registers (e.g. “2h”) while DP83867 only uses MMD address 31 (0x001F) for all extended register writes and reads.

DP83867 and KSZ9031RN have different functions for their extended register sets. See Appendix B for Extended Register comparison. Registers not outlined in Appendix B can be found in the DP83867IR/CR data sheet or the DP83867E/IS/CS data sheet.

4 Informational Changes

This section describes features offered in DP83867, and how to transition to implementing them with DP83867. These functions may or may not be offered in KSZ9031RN device.

Table 4. DP83867 vs. KSZ9031RN Feature Set Comparison

Features	DP83867CR/CS/E/IS	DP83867IR	KSZ9031RN
RGMII	Yes	Yes	Yes
GMII	No	Yes	No
SGMII	Yes(1)	No	No
Interrupt	Yes	Yes	Yes
WoL	Yes	Yes	Yes
Time Domain Reflectometry (TDR)	Yes	Yes	Yes
JTAG	Yes	Yes	No
IEEE 1588 SFD	Yes	Yes	No
IEEE 802.3 Test Modes	Yes	Yes	Yes
Loopback Modes	Yes	Yes	Yes
BIST PRBS	Yes	Yes	No

(1) DP83867CR does not support SGMII.

4.1 Power Down / Interrupt

DP83867 offers a separate, multifunction pin to allow the system to power down the device, or to indicate an interrupt. In Power_Down mode, the PWR_DOWN/INT pin (pin 44) may be asserted low to put the device in a power down state. In Interrupt mode, this pin will be asserted low when an interrupt condition occurs, based on various criteria defined by the ISR (0x0013) and MICR (0x0012) registers. It is recommended to use an external pull-up resistor for proper operation of this function.

KSZ9031RN can generate an interrupt when specific PHY registers are changed. To configure the interrupt, use register 0x001B in the KSZ9031RN.

4.2 Wake on LAN (WoL)

Both DP83867 and KSZ9031 offer Wake on LAN function which is a way of bringing the device out of low-power state using a special Ethernet packet, called a Magic Packet. The DP83867 can be configured to generate an interrupt to wake up the MAC when a qualifying packet is received. It is recommended to use a 2.2-kΩ pull-up resistor if using the INT pin. KSZ9031RN requires a 1-kΩ pull-up resistor on the PME pin for this function.

For customized packet configuration and secure-on password configuration (DP83867 only), see the *Wake-on-Lan Packet Detection* section of the DP83867IR/CR data sheet or the DP83867E/IS/CS data sheet.

4.3 Time Domain Reflectometry (TDR)

DP83867 and KSZ9031 both support Time Domain Reflectometry (TDR) cable diagnostics when there is no active link partner. TDR control and status could be managed using specific MDIO register. Software resets before and after TDR tests are recommended. AutoMDIX should be disabled for KSZ9031RN, but not required for DP83867.

DP83867 supports automatically activated TDR with a link failure by register setting (results saved in TDR registers).

DP83867 also supports Active Link Cable Diagnostics (ALCD) for cable diagnostics with an active link partner.

4.4 Linux Driver

TI supplies a DP83867 Linux Driver available at http://www.ti.com/tool/dp83867sw-linux.

The Linux Driver is also available in the Linux mainline kernel.

4.5 SGMII

SGMII is supported in DP83867CS/E/IS. The Serial Gigabit Media Independent Interface (SGMII) provides a means of conveying network data and port speed between a 100/1000 PHY and a MAC with significantly less signal pins (4 or 6 pins) than required for GMII (24 pins) or RGMII (12 pins). The SGMII interface uses 1.25Gbps LVDS differential signaling which has the added benefit of reducing EMI emissions relative to GMII or RGMII. The following pins are used in SGMII mode:

- SGMII_SIP
- SGMII_SIN
- SGMII_SOP
- SGMII_SON
- SGMII_COP(6 pin mode)
- SGMII_CON(6 pin mode)

4.6 GMII

GMII is supported in DP83867IR 64-QFP package. The Gigabit Media Independent Interface (GMII) is the IEEE defined interface for use between an Ethernet PHY and an Ethernet MAC. GMII is available on the PAP devices only. The purpose of GMII is to make various physical media transparent to the MAC layer. The GMII Interface accepts either GMII or MII data, control and status signals and routes them either to the 1000BASE-T, 100BASE-TX, or 10BASE-Te modules, respectively. The following pins are used in GMII mode:

- TX_EN
- TX_ER
- GTX_CLK
- TX_D[7:0]
- RX_DV
- RX_ER
- RX_CLK
- RX_D[7:0]
- CRS
- COL

Pinout Mapping

Table 5. Pinout Mapping

	DP83867CS/CR/E/IS	DP83867IR	KSZ9031 Pin	Description
MAC Interface				
TX_D	25,26,27,28	31,32,33,34,35,36,37,38	19,20,21,22	Transmit Data
RX_D	33,34,35,36	44,45,46,47,48,49,50,51	32,31,28,27	Receive Data
RX_CLK	32	43	35	RGMII Receive Clock
GTX_CLK	29	40	24	RGMII Transmit Clock.
SGMII_SIP/N	27,28	—	—	Differential SGMII Data Input
SGMII_SOP/N	35,36	—	—	Differential SGMII Data Output
SGMII_COP/N	33,34	—	—	Differential SGMII Clock Output
TX_CTL	37	52	25	Transmit Control
RX_CTL	38	53	33	Receive Control
CS	—	56	—	Carrier Sense
COL	—	55	—	Collision Detect
RX_ER	—	54	—	Receive Error
RX_DV	—	53	—	Receive Data Valid
TX_EN	—	52	—	Transmit Enable
TX_ER	—	39	—	Transmit Error
GPIO				
GPIO_0:1	39,40	48,49,50,51,54,55,56	—	General Purpose I/O
Management Interface				
MDC	16	20	36	Management data Clock
MDIO	17	21	37	Management Data I/O
INT/PWDN	44	60	38	Interrupt / Power Down (Default Power Down)
Reset				
RESET_N	43	59	42	Reset
Clock Interface				
XI	15	19	46	Crystal/Oscillator Input
XO	14	18	45	Crystal Output
CLK_OUT	18	22	41	Clock Output
JTAG Interface Pins				
JTAG_TRSTN	—	24	—	JTAG Test Reset
JTAG_CLK	20	25	—	JTAG Test Clock
JTAG_TDO	21	26	—	JTAG Test Data Output
JTAG_TMS	22	27	—	JTAG Test Mode Select
JTAG_TDI	23	28	—	JTAG Test Data Input
LED Interface				
LED_0:2	47,46,45	61,62,63	17,15	External LED Connections. *KSZ9031RN: Only LED 1 & 2*

Table 5. Pinout Mapping (continued)

	DP83867CS/CR/E/IS	DP83867IR	KSZ9031 Pin	Description
Media Dependent Interface				
TD_P/M_A	1,2	2,3	2,3	Differential Transmit
				and Receive Signals
TD_P/M_B	4,5	5,6	5,6	Differential Transmit
				and Receive Signals
TD_P/M_C	7,8	10,11	7,8	Differential Transmit
				and Receive Signals
TD_P/M_D	10,11	13,14	10,11	Differential Transmit and Receive Signals
Other Pins				
RBIAS	12	15	48	Bias Resistor Connection. *KSZ9031RN: called ISET.*
Power and Ground Pins				
VDDIO	19,30,41	23,41,57	—	I/O Power
VDDA1P8	13,48	17,64	—	1.8-V Analog Supply (±5%).
VDDA2P5	3,9	4,12,	—	2.5-V Analog Supply (±5%).
VDD1P1	6,24,31,42	8,29,42,58	—	1.1-V Analog Supply (±5%).
GND	Die Attach Pad	Die Attach Pad	Die Attach Pad	Ground
AVDDH	—	—	1,12	3.3 / 2.5-V analog VDD
AVDDL	—	—	4,9	1.2-V analog VDD
AVDDL_PLL	—	—	44	1.2-V analog VDD for PLL
DVDDH	—	—	16,34,40	3.3, 2.5, 1.8-V digital VDDIO
DVDDL	—	—	14,18,23,26,30,39	1.2-V digital VDD
LDO_O	—	—	43	On-chip LDO controller to drive the 1.2-V DVDDL (can be left floating)
VSS	—	—	29	KSZ9031RN: Digital Ground

MDIO Register Comparison

Table 6. DP83867 vs. KSZ9031 MDIO Register Differences

Register; Bit	DP83867 Function	KSZ9031RN Function
0x0000; Bit 7	Collision Test	Reserved
0x0007; Bit 14	ACK (of link code word)	Reserved
0x0009; Bit 7	TDR auto run	Reserved
0x00010 – 0x001D (vendor specific)	see data sheet	see data sheet
Extended registers	see data sheet	see data sheet

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