Application Report
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4-Level Strap Device Configuration

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ABSTRACT

4-Level Strap Device Configuration serves as a guide to configure Texas Instruments Ethernet PHYs that feature 4-level strap pins.

4-level straps require more consideration than simple 2-level straps. This configuration note guides a design engineer through implementation of a 4-level strap, and evaluation of the strap in worst case conditions.

Some of the items covered are resistor tolerance considerations, resistor temperature coefficient consideration, and PHY and MAC leakage current.

Contents

1 Introduction[1]

Current generation Ethernet PHYs contain many more configurable features than earlier PHYs. The number of features configured at start-up, like multiple MAC interfaces, MAC interface timing, PHY address, EEE capability, and reference clock frequency, can outnumber the I/O pins available on a PHY. To configure more options than I/O pins, 4-level straps have been introduced to allow a single I/O pin to configure 2 features.

4-level straps require a resistive divider to implement, compared to 2-level straps that use a single resistor. 4-level straps must reliably create a voltage on the I/O pin that corresponds to a defined band. Careful consideration of resistor tolerance and temperature coefficient is key to ensuring proper voltage on the strap at the time of latch-in. This application note details how to use 4-level straps and how to analyze a 4-level strap for reliable operation.

2 Using 4-Level Straps

Texas Instruments' 4-level and 2-level straps are configured at power-up, or by hardware reset (RESET_N pin). The PHY will sample the voltage at each of its designated strap pins once the supply has ramped or post reset deassertion. This process is called *latch-in*. The ratio of R_{hi}, the resistor located between the VDDIO supply and the I/O pin, and of R_{lo}, the resistor placed between ground and the I/O pin, can be modified to configure the PHY for different modes of operation.

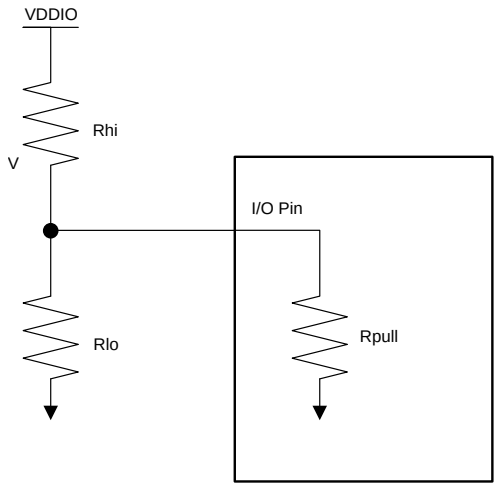

Figure 1. Generic 4-Level Strap Diagram (Internal Pull-Down)

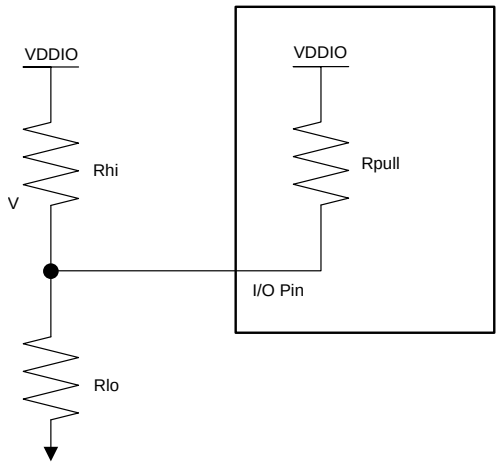

Figure 2. Generic 4-Level Strap Diagram (Internal Pull-Up)

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See the appropriate device data sheet for details on strap options for that device.

2.1 Determining Strap Mode From Datasheet

The following example details what is needed to determine the desired strap mode and the correct way to implement the 4-level strap.

The PHY's address will be set to 0x0002 for this example. Below is an example strap pin table containing PHY Address (PHY_ID) bits [3:0]. There are four PHY_ID pin straps that allow for PHY Address configurations between 0x0000 and 0x000F.

Table 1. Strap Function Table (Pull-Down)

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION		
RX_D0 / SGMII_COP	33	[00]	**MODE**	PHY_ADD1	PHY_ADD0
			1	0	0
			2	0	1
			3	1	0
			4	1	1
RX_D2 / SGMII_CON	35	[00]	**MODE**	PHY_ADD3	PHY_ADD2
			1	0	0
			2	0	1
			3	1	0
			4	1	1

To achieve a PHY ID of 0x2, PHY ID bit [1] should be set, and all other bits cleared. Referencing the above table, RX_D0 pin will be strapped to mode three, and RX_D2 pin must be strapped to mode 1. Note that the default setting of both of these pins is 0b00. The default setting is the value that will be strapped into the PHY if no strap resistors are present during latch-in. Because the default setting for RX_D2 is acceptable, RX_D2 will not be connected to any external resistors.

To strap pin RX_D0 to mode three, the strap resistor ratio table of the device is referenced. See the example table below.

Note: Strap pins have internal pull-up or pull-down resistors. This will change which table is referenced when dealing with devices that feature strap pins with both pull types. Ensure that the proper resistor ratio table is referenced based on resistor pull type.

Table 2. 4-Level Strap Resistor Ratios (Pull-Down)

MODE	TARGET VOLTAGE			IDEAL R_{hi} (kΩ)	IDEAL R_{lo} (kΩ)
	V_{min} (V)	V_{typ} (V)	V_{max} (V)		
1	0	0	0.098 × VDDIO	OPEN	OPEN
2	0.140 × VDDIO	0.165 × VDDIO	0.191 × VDDIO	10	2.49
3	0.225 × VDDIO	0.255 × VDDIO	0.284 × VDDIO	5.76	2.49
4	0.694 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

Table 3. 4-Level Strap Resistor Ratios (Pull-Up)(1)

MODE	TARGET VOLTAGE			IDEAL R_{hi} (kΩ)	IDEAL R_{lo} (kΩ)
	V_{min} (V)	V_{typ} (V)	V_{max} (V)		
1	0	0	0.182	OPEN	1.96
2	0.475	0.528	0.598	13	1.96
3	0.772	0.858	0.944	6.20	1.96
4	1.782	1.98	2.178	OPEN	OPEN

(1) VDDIO = 3.3 V

To place RX_D0 strap in mode three, when RX_D0 contains an internal pull-down resistor, Table 2 should be referenced for the strap voltage requirements.

In a typical application, the ideal resistor values for the desired mode can be used. In special cases, the strap's resistive divider should be analyzed to ensure it falls into the voltage range for the mode. Special cases include having an external pull resistor attached to the pin or use with MACs that have excessive leakage current (greater than 15 µA).

2.2 Considerations for 4-Level Strap Use

2.2.1 Resistor Tolerance

Resistor tolerance is the largest factor for meeting the voltage requirements of the strap pin modes. Resistors should be no more than 1% tolerance for reliable performance.

2.2.2 External Pull Resistors

A common challenge to strap resistive dividers is the presence of a pull-up or pull-down resistor inside of the attached MAC. When using a strap with a resistor internal to the connected MAC, the ideal resistor values cannot be used and a full analysis must be performed.

2.2.3 Leakage Current

Leakage current poses a source of error in the voltage presented to the strap pin. When the leakage current of a MAC's pins exceeds 15 µA, it may be necessary to perform a detailed analysis of the strap pins.

2.2.4 Temperature Variation

System ambient temperatures can be higher than the ideal room temperature of 25ºC when PHY straps are latched-in. During those cases the temperature coefficient of resistance (TCR) of a resistor can have a large impact on the strap's divider.

For example, a resistor with a 100 ppm/ºC TCR may vary as much as 0.8% at 105ºC from its resistance at 25ºC. This effect is compounded with the tolerance of the resistor to create an error of up to 1.8%. TCR is treated in the detailed analysis section. TCR is assumed to be negative when considering minimum tolerance, positive when treating maximum tolerance, and linear. This assumption provides a worst case scenario.

2.2.5 Capacitance External to the Strap Pin

4-level strap pins are latched-in quickly during device power up and reset. As such, a large capacitance should not be connected to the strap pin without a shunt resistor. If this is ignored, the capacitor may not charge or discharge completely before the voltage is sampled on the pin. This leads to strapping unintended values into the PHY.

2.2.6 SGMII Impedance Balancing

When placing a strap resistor divider on a pin that is used for an SGMII interface, like the DP83867E's SGMII_SOP pin, an identical resistor divider must be placed on the corresponding pin of the differential pair, in this case the SGMII_SON pin. This ensures the high-speed LVDS interface has balanced impedance on both lines, preserving the 100R differential characteristic impedance of the pair.

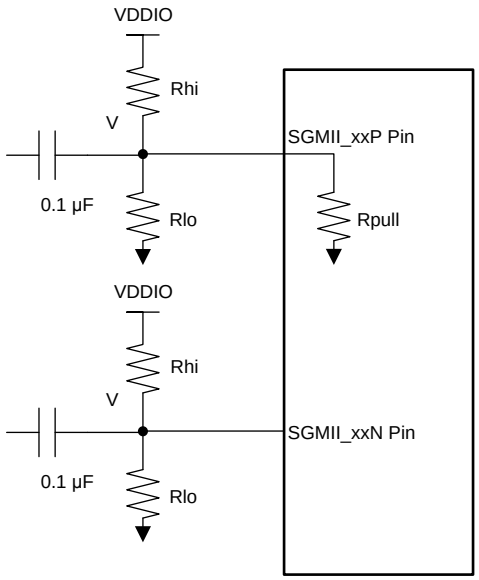

Figure 3. SGMII 4-Level Strap Diagram

3 Analysis of a 4-Level Strap Pin Voltage

Analysis of a strap pin's voltage divider will take into account the first four effects described in section 2.2: resistor tolerance, external pull resistors, leakage current, and TCR.

It must be ensured that the resistive divider provides a voltage greater than the V_{min} value published in the data sheet, this is referred to as V_{min} analysis in this application note. Conversely, the voltage created by the divider must not exceed the V_{max} voltage, this is referred to as V_{max} analysis. Both cases must be checked, and satisfied, for the divider to be considered a proper configuration for reliable operation.

The ideal case is ignored in the analysis because the ideal resistor values have already been calculated for all devices and provided in the data sheet.

3.1 Example with Internal Pull-Down Resistor

The below figure shows the equivalent circuit when considering a strap pin that has an internal pull-down resistor and a MAC connected with an internal pull-down resistor. In the case that the internal resistors are of a different pull type, the analysis should be adjusted accordingly.

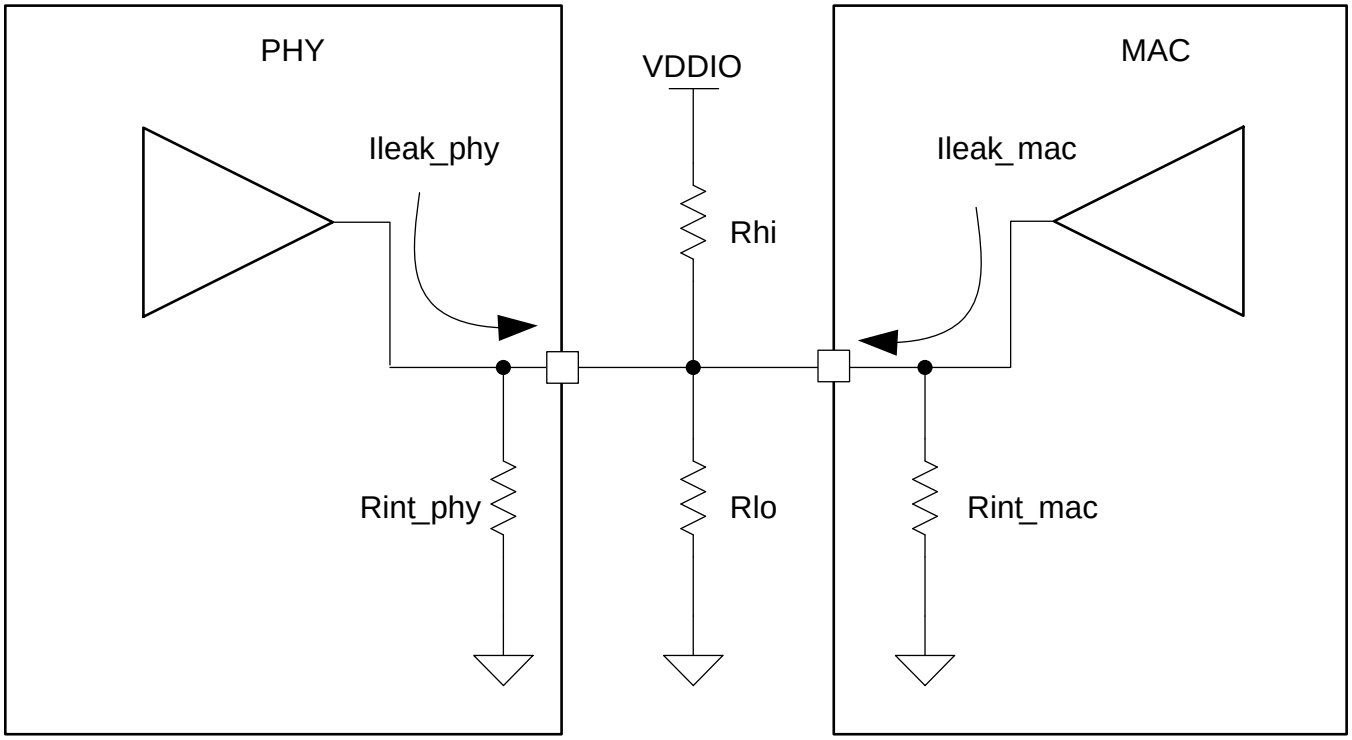

Figure 4. 4-Level Strap Voltage Analysis Model (Internal Pull-Down)

3.1.1 V_{max} Analysis

$$V_{max} \times VDDIO \geq \frac{R_{eq+}}{R_{eq+} + R_{hi-}} \times VDDIO + (I_{leak\_mac+} + I_{leak\_phy+}) \times R_{strap+} \quad (1)$$

where:

$$R_{strap+} = R_{eq+} \parallel R_{hi-}$$

$$R_{eq+} = R_{int\_phy+} \parallel R_{lo+} \parallel R_{int\_mac+} = \frac{R_{int\_phy+} \times R_{lo+} \times R_{int\_mac+}}{(R_{int\_phy+} \times R_{lo+}) + (R_{lo+} \times R_{int\_mac+}) + (R_{int\_mac+} \times R_{int\_phy+})}$$

$$R_{hi-} = R_{hi} \times (1 - R_{hi\_tol} - \frac{R_{hi\_TCR}}{10^6} \times [System\_max\_temp - Nominal\_R\_temp])$$

$$R_{lo+} = R_{lo} \times (1 + R_{lo\_tol} + \frac{R_{lo\_TCR}}{10^6} \times [System\_max\_temp - Nominal\_R\_temp])$$

$$R_{int\_phy+} = R_{int\_phy} \times (1 + R_{int\_phy\_tol})$$

$$R_{int\_mac+} = R_{int\_mac} \times (1 + R_{int\_mac\_tol})$$

3.1.2 V_{min} Analysis

$$V_{min} \times VDDIO \le \frac{R_{eq-}}{R_{eq-} + R_{hi+}} \times VDDIO + (I_{leak\_mac-} + I_{leak\_phy-}) \times R_{strap-} \quad (2)$$

where:

$$R_{strap-} = R_{eq-} \parallel R_{hi+}$$

$$R_{eq+} = R_{int\_phy+} \parallel R_{lo+} \parallel R_{int\_mac+} = \frac{R_{int\_phy+} \times R_{lo+} \times R_{int\_mac+}}{(R_{int\_phy+} \times R_{lo+}) + (R_{lo+} \times R_{int\_mac+}) + (R_{int\_mac+} \times R_{int\_phy+})}$$

$$R_{hi+} = R_{hi} \times \left(1 + R_{hi\_tol} + \frac{R_{hi\_TCR}}{10^6} \times [System\_max\_temp - Nominal\_R\_temp]\right)$$

$$R_{lo-} = R_{lo} \times \left(1 - R_{lo\_tol} - \frac{R_{lo\_TCR}}{10^6} \times [System\_max\_temp - Nominal\_R\_temp]\right)$$

$$R_{int\_phy-} = R_{int\_phy} \times (1 - R_{int\_phy\_tol})$$

$$R_{int\_mac-} = R_{int\_mac} \times (1 - R_{int\_mac\_tol})$$

3.1.3 Example Analysis

As an example, using the equations above and Table 2, calculate V_{max} and V_{min} of the resistive divider for an internal pull-down strap pin in mode three.

Given:

System_max_temp = 85 ºC
Nominal_R_temp = 25 ºC
TCR = 100 ppm/ºC
R_{hi} = 5.76 kΩ
R_{hi_tol} = ±1%
R_{lo} = 2.49 kΩ
R_{lo_tol} = ±1%
R_{int_phy} = 9 kΩ
$R_{int\_phy\_tol}$ = ±25%
R_{int_mac} = 1 MΩ (open)
$R_{int\_mac\_tol}$ = ±0%
I_{leak_mac} = ±10 µA
I_{leak_phy} = 0 µA / +5 µA
VDDIO = 3.3 V

For the hypothetical device from section 2, mode three has the following voltage requirements: VDDIO × V_{min} = 0.743 V and VDDIO × V_{max} = 0.937 V.

Solving for the right side of Equation 1, the result is 0.904 V. Solving for the right side of Equation 2, the result is
0.762 V.

In the example configuration, we satisfy the condition for V_{max} : 0.937 V ≥ 0.904 V. V_{min} is also satisfied: 0.743 V ≤ 0.762 V

The chosen values for R_{hi} and R_{lo} in the example meet both conditions for mode three and are a valid solution.

3.2 Example with Internal Pull-Up Resistor

The below figure shows the equivalent circuit when considering a strap pin that has an internal pull-up resistor and a MAC connected with an internal pull-down resistor.

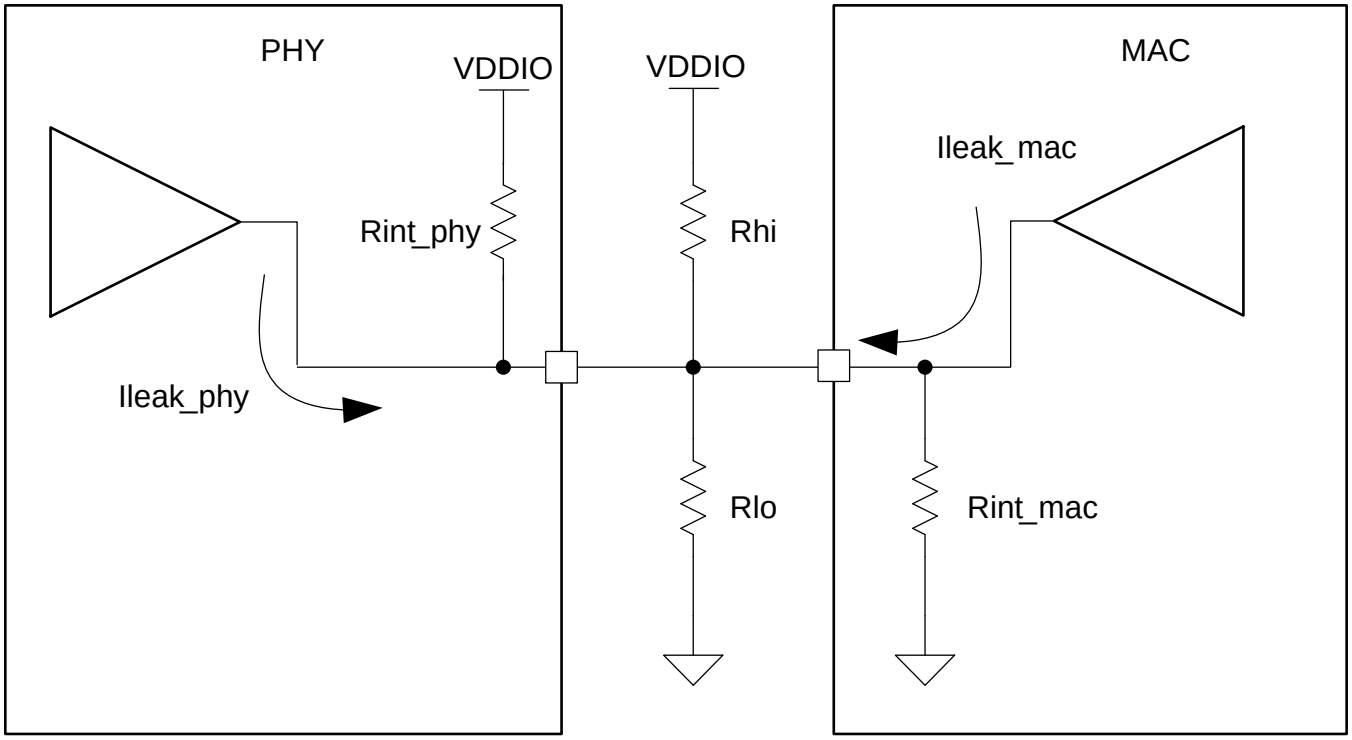

Figure 5. 4-Level Strap Voltage Analysis Model (Internal Pull-Up)

V_{max} Analysis

$$V_{max} \times VDDIO \geq \frac{R_{lo\_eq+}}{R_{lo\_eq+} + R_{hi\_eq-}} \times VDDIO + (I_{leak\_mac+} + I_{leak\_phy+}) \times R_{strap+} \quad (3)$$

where:

$$R_{strap+} = R_{lo\_eq+} \parallel R_{hi\_eq-}$$

$$R_{lo\_eq+} = R_{lo+} \parallel R_{int\_mac+} = \frac{R_{lo+} \times R_{int\_mac+}}{R_{lo+} + R_{int\_mac+}}$$

$$R_{hi\_eq-} = R_{hi-} \parallel R_{int\_phy-} = \frac{R_{hi-} \times R_{int\_phy-}}{R_{hi-} + R_{int\_phy-}}$$

$$R_{hi-} = R_{hi} \times (1 - R_{hi\_tol} - \frac{R_{hi\_TCR}}{10^6} \times [System\_max\_temp - Nominal\_R\_temp])$$

$$R_{lo+} = R_{lo} \times (1 + R_{lo\_tol} + \frac{R_{lo\_TCR}}{10^6} \times [System\_max\_temp - Nominal\_R\_temp])$$

$$R_{int\_phy-} = R_{int\_phy} \times (1 - R_{int\_phy\_tol})$$

$$R_{int\_mac+} = R_{int\_mac} \times (1 + R_{int\_mac\_tol})$$

3.2.1 V_{min} Analysis

$$V_{min} \times VDDIO \le \frac{R_{lo\_eq-}}{R_{lo\_eq-} + R_{hi\_eq+}} \times VDDIO + (I_{leak\_mac-} + I_{leak\_phy-}) \times R_{strap-} \quad (4)$$

where:

$$R_{strap-} = R_{lo\_eq-} \parallel R_{hi\_eq+}$$

$$R_{lo\_eq-} = R_{lo-} \parallel R_{int\_mac-} = \frac{R_{lo-} \times R_{int\_mac-}}{R_{lo-} + R_{int\_mac-}}$$

$$R_{hi\_eq+} = R_{hi+} \parallel R_{int\_phy+} = \frac{R_{hi+} \times R_{int\_phy+}}{R_{hi+} + R_{int\_phy+}}$$

$$R_{hi+} = R_{hi} \times (1 + R_{hi\_tol} + \frac{R_{hi\_TCR}}{10^6} \times [System\_max\_temp - Nominal\_R\_temp])$$

$$R_{lo-} = R_{lo} \times (1 - R_{lo\_tol} - \frac{R_{lo\_TCR}}{10^6} \times [System\_max\_temp - Nominal\_R\_temp])$$

$$R_{int\_phy+} = R_{int\_phy} \times (1 + R_{int\_phy\_tol})$$

$$R_{int\_mac-} = R_{int\_mac} \times (1 - R_{int\_mac\_tol})$$

3.2.2 Example Analysis

As an example, using the equations above and Table 3 , calculate V_{max} and V_{min} of a resistive divider for an internal pull-up strap pin in mode two.

Given:

System_max_temp = 85 ºC
Nominal_R_temp = 25 ºC
TCR = 100 ppm/ºC
R_{hi} = 13 kΩ
R_{hi_tol} = ±1%
R_{lo} = 1.96 kΩ
R_{lo_tol} = ±1%
R_{int_phy} = 50 kΩ
$R_{int\_phy\_tol}$ = ±25%
R_{int_mac} = 1 MΩ (open)
$R_{int\_mac\_tol}$ = ±0%
I_{leak_mac} = ±10 µA
I_{leak_phy} = 0 µA / +5 µA
VDDIO = 3.3 V

For the hypothetical device from section 2, mode two has the following voltage requirements: VDDIO × V_{min} = 0.475 V and VDDIO × V_{max} = 0.598 V.

Solving for the right side of Equation 3, the result is 0.595 V. Solving for the right side of Equation 4, the result is
0.480 V.

In the example configuration, we satisfy the condition for V_{max} : 0.598 V ≥ 0.595 V. V_{min} is also satisfied: 0.475 V ≤ 0.480 V

The chosen values for R_{hi} and R_{lo} in the example meet both conditions for mode two and are a valid solution.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2016) to A Revision	Page
• Fixed typos	1

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