Application Report
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RGMII Interface Timing Budgets

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ABSTRACT

RGMII Interface Timing Budgets is intended to serve as a guideline for developing a timing budget when using the RGMII v1.3 and v2.0 standard with a Gigabit PHY transceiver like the DP83867.

The methods in this document describe how to set up an RGMII specific timing budget and determine acceptable delays required for RGMII.

An example of creating a budget is shown, and also how to implement the required clock delay on the DP83867 using strap configuration options or MDIO access.

The application note then describes how to measure the delay of an RGMII transmitter.

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1 Introduction

The reduced gigabit media independent interface (RGMII) has become a widely used alternative to the gigabit media independent interface (GMII) by offering lower pin count which enables board space, and cost, savings. The RGMII standard achieves this by reducing parallel data bus width and through double data rate (DDR).

RGMII specifies that the clock and data will be generated simultaneously by the transmitting source which requires a skew be introduced between clock and data. The skew can be achieved by PCB trace routing or by an internal delay in the transmitting or receiving node. The skew imposed on the clock and data shall be chosen carefully to ensure meeting the requirements of the interface as described in the next section.

This application note describes how to put together a timing budget to determine an acceptable skew range.

2 RGMII Timing Specifications

All RGMII compliant devices shall conform to the requirements listed below:

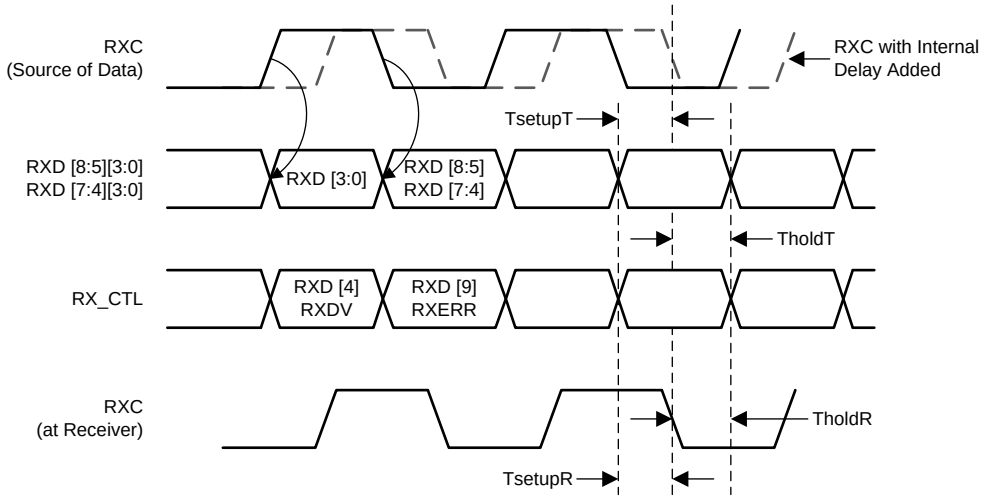

Figure 1. RGMII RX Timing Diagram

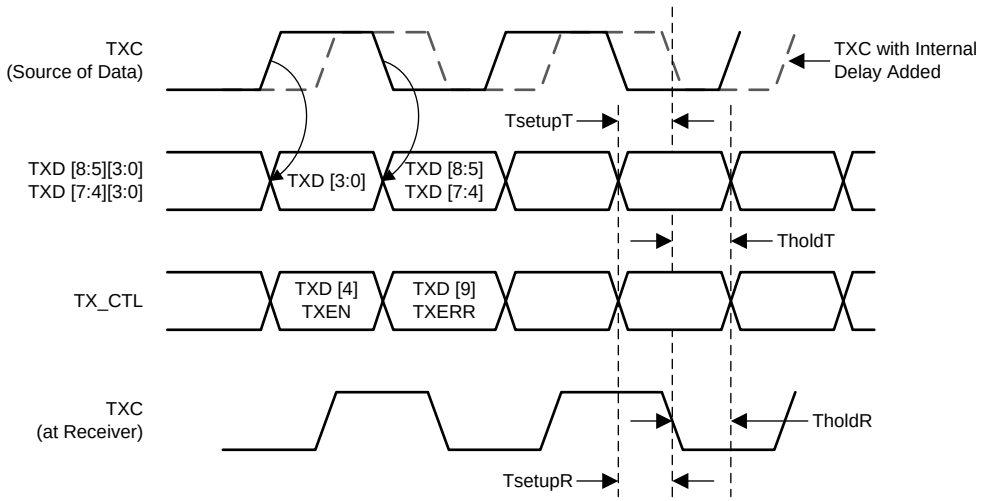

Figure 2. RGMII TX Timing Diagram

Table 1. RGMII v2.0 Timing Requirements

Symbol	Parameter	Min	Typ	Max	Units
TskewT	Data to Clock output Skew (at Transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at Receiver)	1	1.8	2.6	ns
TsetupT	Data to Clock output Setup	1.2	2		ns
TholdT	Data to Clock output Hold	1.2	2		ns
TsetupR	Data to Clock input Setup	1	2		ns
TholdR	Data to Clock input Hold	1	2		ns
Tcyc	Clock Cycle Duration (1)	7.2	8	8.8	ns
Duty_G	Duty Cycle for 1000BASE	45	50	55	%
Duty_T	Duty Cycle for 10/100BASE	40	50	60	%
Tr/Tf	Rise / Fall Time (20-80%)			0.75	ns

3 Timing Budget

This analysis will be focused on a worst case scenario using variables that are expected to impact the RGMII timing budget.

For the purpose of this document's analysis, 1000 Mb/s requirements will be used. 1000 Mb/s timing budget will satisfy the 10/100 Mb/s requirements.

The RGMII standard uses the same setup and hold requirements for RX and TX datapaths. The budget shown here will look at only one path, but a budget would be created for both paths for each application determine required RX and TX delays.

3.1 Definitions

The following definitions are used through the budget composition:

- Skew = Delay between clock and data transitions
- T_{skewT} = Skew between clock and data at the transmitter
- ID = Introduced delay between clock and data by PCB routing or internal buffer delay
- ID_{var} = Variation in introduced delay
- IO_{skew} = I/O buffer skew
- PCB_{skew} = Skew introduced by PCB effects
- Min_{SR} = Minimum setup time required by receiver
- Min_{HR} = Minimum hold time required by receiver

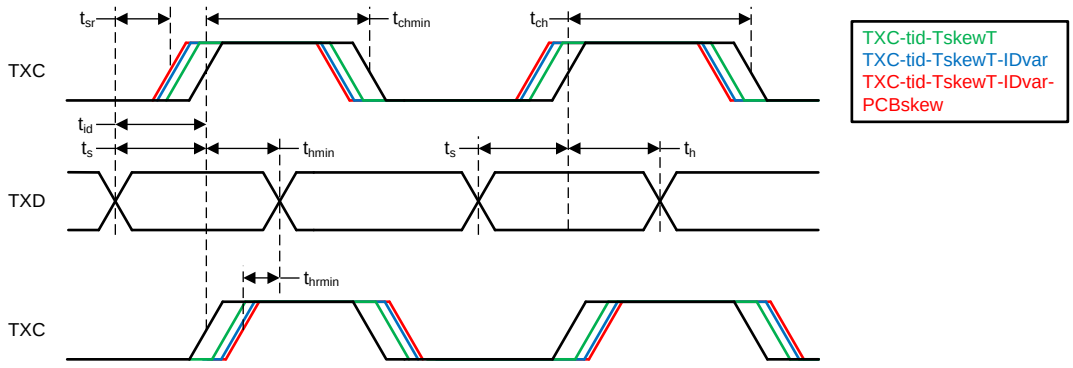

Figure 3. RGMII Timing Diagram Including Duty Cycle Effects

NOTE: Duty cycle affects data, as well as the clock, reducing hold time.

Table 2. RGMII Timing Diagram Symbols

SYMBOL	PARAMETER
t_{ch}	Cycle time during high period of clock. Ideally equal to 4 nanoseconds
t_{chmin}	Minimum cycle time during high period of clock (at 45% duty cycle)
t_{id}	Delay introduced by design
t_s	Nominal setup time
t_{sr}	Minimum setup time with non-idealities present
t_h	Nominal hold time
t_{hmin}	Hold time (at 45% duty cycle)
t_{hrmin}	Minimum hold time with non-idealities present

Figure 3 shows the timing relationship between the clock and data with the effect of all typical non-idealities included. The diagram uses the worst case values from the DP83867 family of PHYs to clearly illustrate their effects.

3.2 Equations

From Figure 3 we see that the nominal setup time is equal to the introduced delay. All other terms are subtracted to yield the worst-case setup time at the receiver.

$$t_{sr} = t_{id} - ID_{VAR} - T_{skewT} - IO_{skew} - PCB_{skew} \quad (1)$$

To calculate the setup margin, we subtract the minimum setup time required by the receiver from the worst-case setup time. If the Min_{SR} is less than the RGMII specified 1.2 ns, more margin can be gained by using the receiver's Min_{SR}.

$$Setup\,Margin = t_{sr} - Min_{SR} \quad (2)$$

The hold time is the remainder of the clock's high cycle once the introduced delay has been accounted for. Because the RGMII standard allows a 5% variation in duty cycle, worst-case scenario is that t_{ch} is 5% shorter than nominal, notated as t_{chmin} here.

$$t_{hr\,min} = t_{ch\,min} - t_{id} - ID_{VAR} - T_{skewT} - IO_{skew} - PCB_{skew} \quad (3)$$

To calculate the hold margin, we subtract the minimum hold time required by the receiver from the worst-case hold time. If the Min_{HR} is less than the RGMII specified 1 ns, more margin can be gained by using the receiver's Min_{HR}.

$$Hold\,Margin = t_{hr} - Min_{HR} \quad (4)$$

In the above equations, t_{id} and ID_{var} can be set to 0 if the delay is incorporated into PCB_{skew}.

3.3 Example Calculation

The following example calculation uses the DP83867 Gigabit Ethernet PHY which has RGMII internal delays programmable via register.

The example addresses the TX path where the minimum setup and hold times for the DP83867 can be substituted for the RGMII standard minimum setup and hold times.

Table 3. DP83867 RGMII Timing Specifications

Symbol	Parameter	Max	Units
ID_{var}	Variation in nominal internal delay	0.2	ns
IO_{skew}	I/O buffer skew	0.35	ns
Min_{SR}	Minimum setup time required by receiver	0.5	ns
Min_{HR}	Minimum hold time required by receiver	0.25	ns

NOTE: DP83867 allows adjustment of RGMII delay from 0 ns to 4 ns in 0.25 ns increments. Selected ID must fall in the range and be divisible by 0.25 to be valid.

ID selected = 2.0 ns

PCB skew tolerance = 0.1 ns

Using Equation 1 through Equation 4 we can calculate the margin of the setup and hold time with the selected ID and PCB skew.

$$\text{Setup Margin} = 2 - 0.2 - 0.5 - 0.35 - 0.1 - 0.5 = 0.35\,\text{ns} \quad (5)$$

$$\text{Hold Margin} = 3.6 - 2 - 0.2 - 0.5 - 0.35 - 0.1 - 0.25 = 0.2\,\text{ns} \quad (6)$$

From the results above we can see that the setup and hold margin are both greater than 0 as desired. This extra margin could be used to relax layout requirements on trace length matching and impedance control on cost sensitive PCBs.

4 Implementing RGMII Internal Delays With DP83867

The DP83867 offers two methods for enabling and setting internal delays for RGMII: MDIO register access and strap configuration.

4.1 Internal Delay With Strap Options

Strap configuration allows a designer to configure a device without use of the MDIO bus to access the device's register space. The DP83867 [applicable to DP83867xxRGZ devices only] has strap options available to set the RGMII RX and TX clock skew.

Strap modes are used by setting up a voltage on the strap pins at device start up or hardware reset. This is typically achieved by placing a resistive divider on the strap pins as described in the Strap Configuration section of the DP83867xxRGZ datasheet.

In order to strap an internal delay of 2.0 ns on the RX bus and 1.5 ns on the TX bus we need the following tables from the DP83867xxRGZ datasheet.

Table 4. DP83867xxRGZ RGMII Strap Pins

PIN NAME	48 QFN PIN #	DEFAULT	STRAP FUNCTION		
LED_2	44	[00]	**MODE**	RGMII Clock Skew TX[1]	RGMII Clock Skew TX[0]
			1	0	0
			2	0	1
			3	1	0
			4	1	1
LED_1	45	[00]	**MODE**	SPEED_SEL0	RGMII Clock Skew TX[2]
			1	0	0
			2	0	1
			3	1	0
			4	1	1
GPIO_0	39	[00]	**MODE**	RGMII Clock Skew RX[0]	
			1	0	
			2	Not Applicable	
			3	1	
			4	Not Applicable	
GPIO_1	40	[00]	**MODE**	RGMII Clock Skew RX[2]	RGMII Clock Skew RX[1]
			1	0	0
			2	0	1
			3	1	0
			4	1	1

Table 5. DP83867xxRGZ RX/TX Clock Skew Details

MODE	RGMII CLOCK SKEW RX/TX[2]	RGMII CLOCK SKEW RX/TX[1]	RGMII CLOCK SKEW RX/TX[0]	RGMII RX/TX CLOCK SKEW
1	0	0	0	2.0 ns
2	0	0	1	1.5 ns
3	0	1	0	1.0 ns
4	0	1	1	0.5 ns
5	1	0	0	4.0 ns
6	1	0	1	3.5 ns
7	1	1	0	3.0 ns
8	1	1	1	2.5 ns

1. For an RX delay of 2.0 ns, mode 1 from Table 5 is used. Table 5 shows RX[2:0] bits should be set accordingly: RX[2] = 0, RX[1] = 0, RX[0] = 0
2. Referring to Table 4 and the result in step 1, RX[2] = 0 & RX[1] = 0,which is only satisfied by strapping GPIO_1 pin in mode 1.
3. Referring to Table 4 and the result in step 1, RX[0] = 0, GPIO_0 should be strapped to mode 1.
4. For a TX delay of 1.5ns, mode 2 from Table 5 is used. Table 5 shows TX[2:0] bits should be set accordingly: TX[2] = 0, TX[1] = 0, TX[0] = 1.
5. Referring to Table 4 and step 4, TX[2] = 0, LED_1 should be strapped in either mode 1 or 3 depending on the designs requirements for the SPEED_SEL option.
6. Finally, for TX[1] = 0 & TX[0] = 1, is only satisfied by strapping the LED_2 pin in mode 2.
7. To select the proper resistor combination to place the strap pins in the correct modes, please refer to the strap configuration section in the DP83867xxRGZ datasheet.

4.2 Internal Delay Using MDIO Settings

If MDIO access is available, and software configuration is possible, RGMII internal delays can be set on the DP83867 family of devices.

To set an internal delay of 1.75 ns on the RX bus and 2.25 ns on the TX bus we need the following table from the DP83867 datasheet.

Table 6. DP83867 RGMII Delay Control Register (RGMIIDCTL), Address 0x0086

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
7:4	RGMII_TX_DELAY_CTRL	RW, 0111	RGMII Transmit Clock Delay: 1111: 4.00 ns 1110: 3.75 ns 1101: 3.50 ns 1100: 3.25 ns 1011: 3.00 ns 1010: 2.75 ns 1001: 2.50 ns 1000: 2.25 ns 0111: 2.00 ns 0110: 1.75 ns 0101: 1.50 ns 0100: 1.25 ns 0011: 1.00 ns 0010: 0.75 ns 0001: 0.50 ns 0000: 0.25 ns
3:0	RGMII_RX_DELAY_CTRL	RW, 0111	RGMII Receive Clock Delay: 1111: 4.00 ns 1110: 3.75 ns 1101: 3.50 ns 1100: 3.25 ns 1011: 3.00 ns 1010: 2.75 ns 1001: 2.50 ns 1000: 2.25 ns 0111: 2.00 ns 0110: 1.75 ns 0101: 1.50 ns 0100: 1.25 ns 0011: 1.00 ns 0010: 0.75 ns 0001: 0.50 ns 0000: 0.25 ns

1. For an RX delay of 1.75ns, Table 6 shows bits[3:0] should be set to 0b0110.
2. For an TX delay of 2.25ns, Table 6 shows bits[7:4] should be set to 0b1000.
3. Upon initialization of the DP83867 device, register 0x86 should be written with value 0x0086.
4. By default, RGMII RX/TX internal delays are enabled in the DP83867. To ensure the delays are enabled, bits[1:0] of RGMII Control Register(address 0x32) should be written as 0b11.

5 Measuring RGMII Delay

The following method to measure delay was performed with the DP83867ERGZ Customer EVM as the transmitter.

To measure the delay of the RX datastream from the DP83867 MDIO access will be needed as well as an oscilloscope with at least 250MHz bandwidth and 2 channels.

Connect channel 1 of the oscilloscope to the RX_CLK signal on the DP83867ERGZ Customer EVM.

Connect channel 2 of the oscilloscope to one of the RX_D[3:0] bits on the DP83867ERGZ Customer EVM.

Using the MDIO controller of your choice, perform the following register transactions to start pseudo-random data generation inside the DP83867 that will be output on the RX datapath.

```
write 0x0040 to register 0x0000 // Force 1000BASE speed
write 0x0c01 to register 0x0170 // Adjust IO pad impedance
write 0xd001 to register 0x0016 // Start PRBS generation and loopback to RGMII
write 0x0077 to register 0x0086 // Set RX & TX RGMII clock delay to 2.0 ns
write 0x00d3 to register 0x0032 // Enable RX & TX clock delay
```

Trigger the oscilloscope from the rising or falling edge of the RX_CLK signal on channel 1.

Use the oscilloscope measurement function or cursors to measure the distance between the clock edge and the data transition immediately before or after the clock transition to measure setup or hold time respectively.

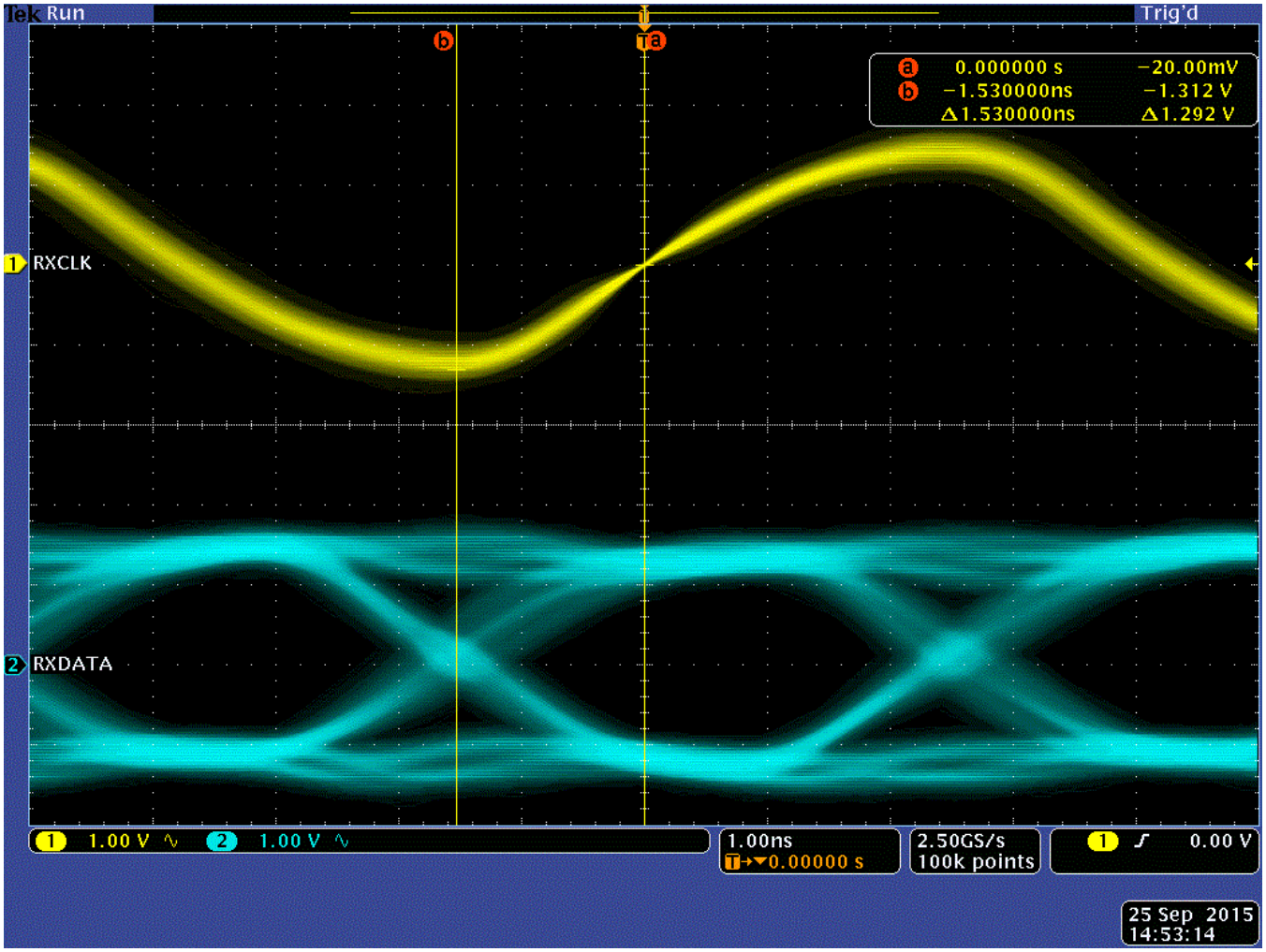

Figure 4. Example Measurement of RGMII Setup Time

In the above Figure 4, see that the measured setup time is 1.53ns. This fits within the worst case setup time expected of:

t_{id} - ID_{VAR} - T_{skewT} = 2.0 - 0.5 - 0.2 = 1.3 ns

6 References

1. *Reduced Gigabit Media Independent Interface (RGMII) Version 1.3*
2. *Reduced Gigabit Media Independent Interface (RGMII) Version 2.0*
3. *DP83867IRPAP/IRRGZ/CRRGZ Robust, High Immunity 10/100/1000 Ethernet Physical Layer Transceiver (SNLS484)*
4. *DP83867CSRGZ /ISRGZ/ERGZ Robust, High Immunity, Small Form Factor 10/100/1000 Ethernet Physical Layer Transceiver (SNLS504)*

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