Application Note

How to Configure DP8386x for Ethernet Compliance Testing

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ABSTRACT

This application note includes how to setup and configure the DP83867 and DP83869 (further refereed to as DP8386x) PHY for Ethernet Physical Layer Compliance (IEEE802.3). This application note primarily uses DP83867 as an example, but DP83869 can also use these scripts for compliance testing.

While the same 10/100 Mbps testing methodology is used in the exclusive 10/100 Mbps PHYs (DP83822, DP83825, DP83826), please refer to *DP8382x IEEE 802.3u Compliance and Debug*, application note for more detailed procedure specific to those devices.

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Trademarks

1 Standards and System Requirements

1.1 Standards

The following standards serve as references for the tests described in this document.

- Subclause 14.3.1 of IEEE standard 802.3-2002
- Subclause 40.6 IEEE standard 802.3-2002
- ANSI X3.263-1995

1.2 Test Equipment Suppliers

The different test equipment used to perform the various procedures described in this document can be procured from the following suppliers. Obtaining some of this equipment may require going through an agent.

- Tektronix
- Spirent
- Agilent (Keysight)
- Rohde and Schwarz
- Teledyne LeCroy

1.3 Test System Requirements

For testing an Ethernet PHY for compliance, the following hardware and software are required:

- Oscilloscope with Ethernet physical layer compliance software (for example, Tektronix TDSET3)
- Ethernet compliance test fixture
- Register access to PHY (for example, TI's USB-2-MDIO GUI when using MSP430)
- DC power supply
- Necessary cables and probes

1.4 Software Setup and Installation

Consult the test equipment OEM’s Ethernet compliance software manual for help with compliance software installation.

For alternative MDIO access through MSP430 Launchpad, see the USB-2-MDIO User’s Guide.

- USB-2-MDIO tool page

2 Ethernet Physical Layer Compliance Testing

2.1 Standard Test Setup and Procedures

For Ethernet physical layer compliance testing, the PHY is managed through the serial management interface (SMI – also know as MDIO interface) to configure the required test mode scripts. The testing results are determined and recorded by the oscilloscope's Ethernet compliance software (for example, Tektronix's TDSET3). It is best to consult with the user's manual of the instrument for proper operation of the software.

The variation between Ethernet physical layer compliance tests is primarily the test mode (see Appendix A) of the PHY and the connection to the test fixture .

The softwares can usually test for many speed options, but it is important to test for the desired end use-case application. When testing 1Gbps, all four channels will need to be tested, while in 10/100 Mbps, one or two channels (depending on MDI/MDIX) will need to be tested.

It is important to account for sample sizes and run-to-run variation when conducting testing.

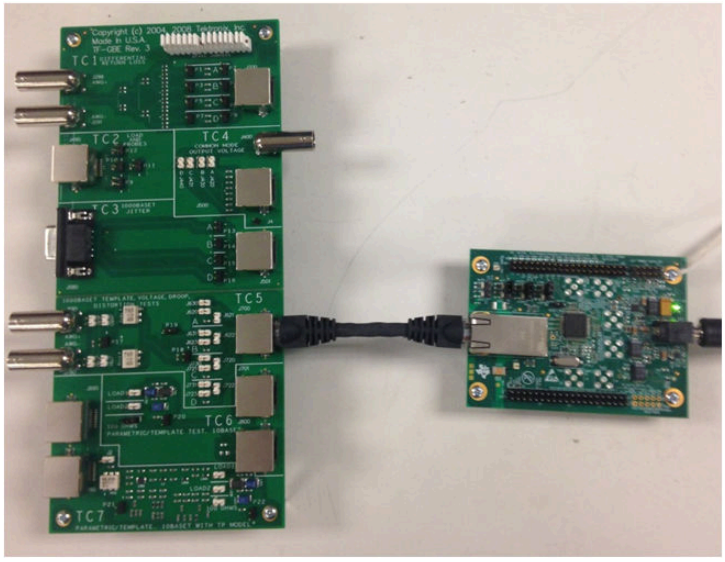

Figure 2-1. DP83867 Connected to Testing Fixture through CAT5e Cable

2.2 1000BASE-T

Refer to Appendix B for 1000BASE-T register writes.

2.2.1 Test Mode 1

Configure PHY to Test Mode 1 for the following tests by setting MDIO registers according to *1000 Base Test Mode 1* in Appendix B.

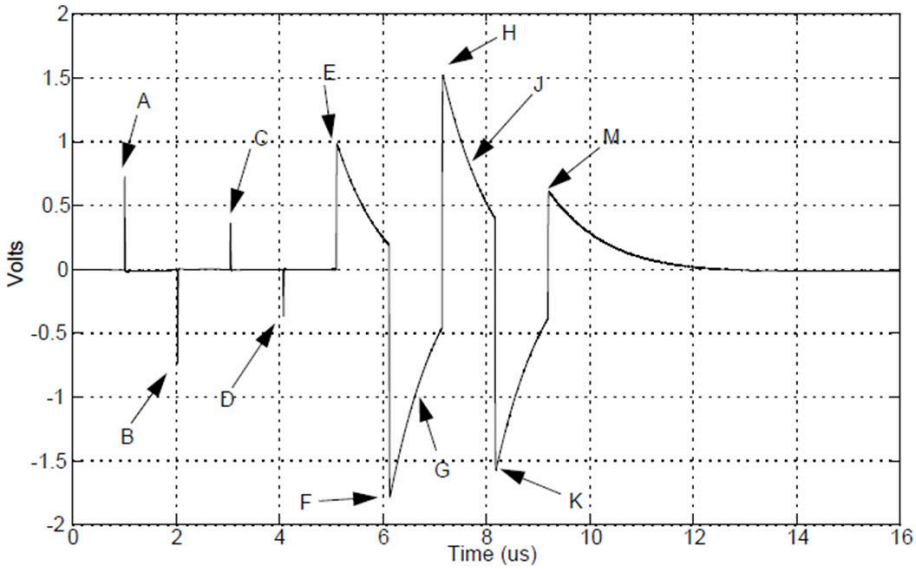

Figure 2-2. IEEE Test Mode 1 per Standard

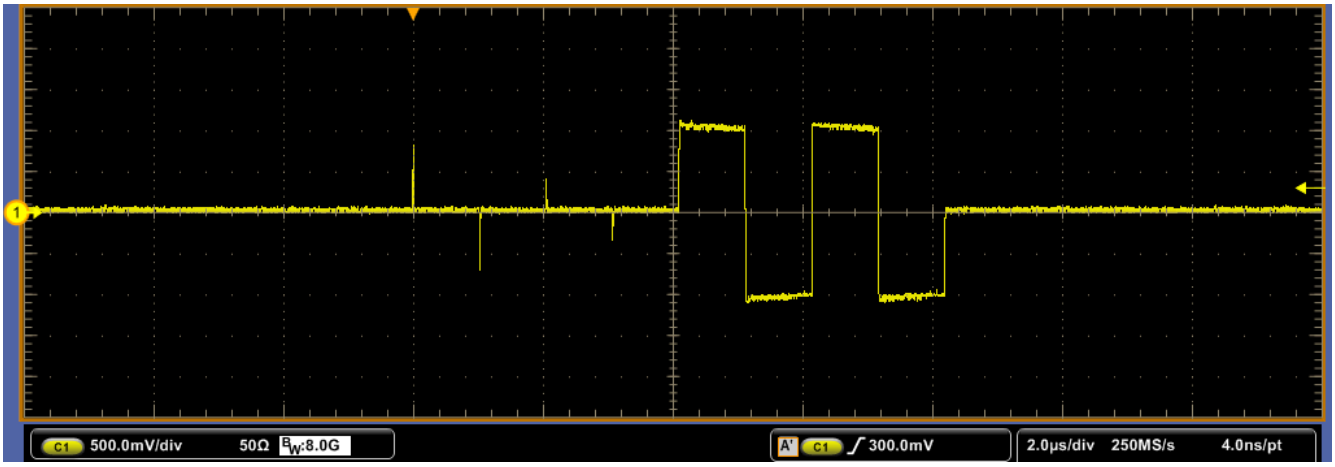

Figure 2-3. DP8386x Test Mode 1 Output Waveform

2.2.1.1 Template

Purpose: To make sure that the PHY transmit waveforms fit into the IEEE-defined templates.

Pass Condition: Voltage output waveforms fit into IEEE-defined templates with PHY in Test Mode 1 after normalization.

Specific Test Setup: Verify the correct test fixture connections. Note that some Ethernet compliance software can run Template and Peak Voltage Tests simultaneously.

2.2.1.2 Peak Voltage

Purpose: To ensure correct PHY transmitter output voltage levels.

Pass Condition: Voltage Levels are to be within:

$$0.67V < Peak\,Voltage\ A < 0.82V \quad (1)$$

$$0.67\ V < Peak\ Voltage\ B < 0.82\ V \quad (2)$$

$$\frac{Peak\ Voltage\ B - |Average\ of\ Peak\ Voltage\ A\ and\ B|}{|Average\ of\ Peak\ Voltage\ A\ and\ B|} \times 100\,\% < 1\,\% \quad (3)$$

$$2\,\% < 100\,\% \times \left(1 - \frac{0.5 \times |Average\ of\ Peak\ Voltage\ A\ and\ B|}{|Peak\ Voltage\ C|}\right) \quad (4)$$

$$2\,\% < 100\,\% \times \left(1 - \frac{0.5 \times |Average\ of\ Peak\ Voltage\ A\ and\ B|}{|Peak\ Voltage\ D|}\right) \quad (5)$$

Where *Average of Peak Voltage A and B* is defined as $\frac{Peak\ Voltage\ A + |Peak\ Voltage\ B|}{2}$.

Specific Test Setup: Verify the correct test fixture connections. Note that some Ethernet compliance software can run Template and Peak Voltage Tests simultaneously.

Note

Some older versions of Ethernet compliance software use an incorrect formula for determining symmetry within 1% between Peak Voltage A and B. This can result in 2x the actual percent value, failing the test case. Hence any failing result needs to be double checked using (3).

2.2.1.3 Droop

Purpose: To make sure that the transmitter output voltage does not decay faster than specified in IEEE 802.3.

Pass Condition: The magnitude of the voltage 500 ns after point F and H (called points G and J, respectively) needs to be greater than 73.1% of the magnitude of points F and H, respectively.

Specific Test Setup: Verify the correct test fixture connections.

2.2.2 Test Mode 2

Configure PHY to Test Mode 2 for the following tests by setting MDIO registers according to *1000 Base Test Mode 2* in Appendix B.

Note

DP8386x is unable to support providing the TX_TCLK signal to external pin. Therefore, slave jitter testing cannot be conducted as a link partner is required for this test. Please make sure the scope is set accordingly for these configurations when conducting jitter testing.

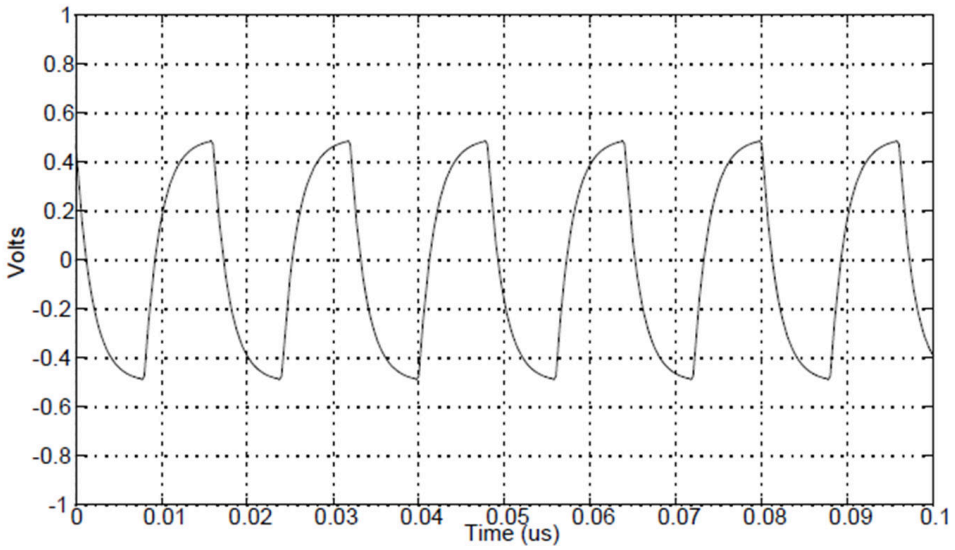

Figure 2-4. IEEE Test Mode 2 per Standard

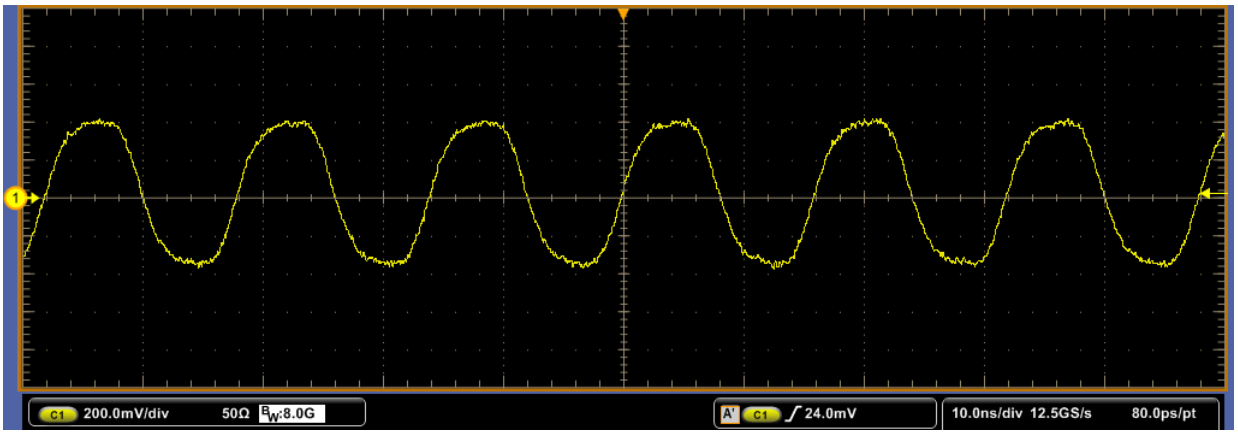

Figure 2-5. DP8386x Test Mode 2 Output Waveform

2.2.2.1 Jitter Master Unfiltered

Purpose: To make sure that the PHY TX_TCLK Jitter with respect to an unjittered reference is within the specified bounds.

Pass Condition: The peak-to-peak value of the jittered waveform with respect to the unjittered reference needs to be less than 1.4 ns.

Specific Test Setup: Verify the correct test fixture connections.

2.2.3 Test Mode 4

Configure PHY to output Test Mode 4 by setting MDIO registers according to *1000 Base Test Mode 4* in Appendix B.

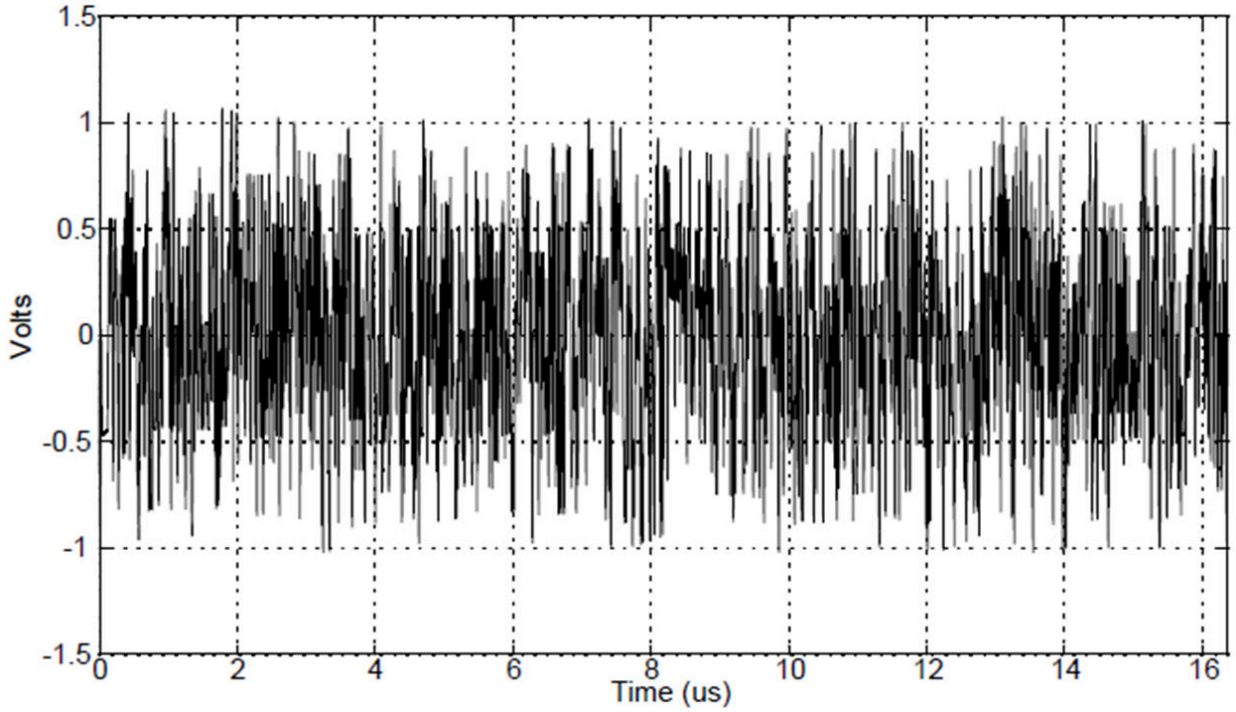

Figure 2-6. IEEE Test Mode 4 per Standard

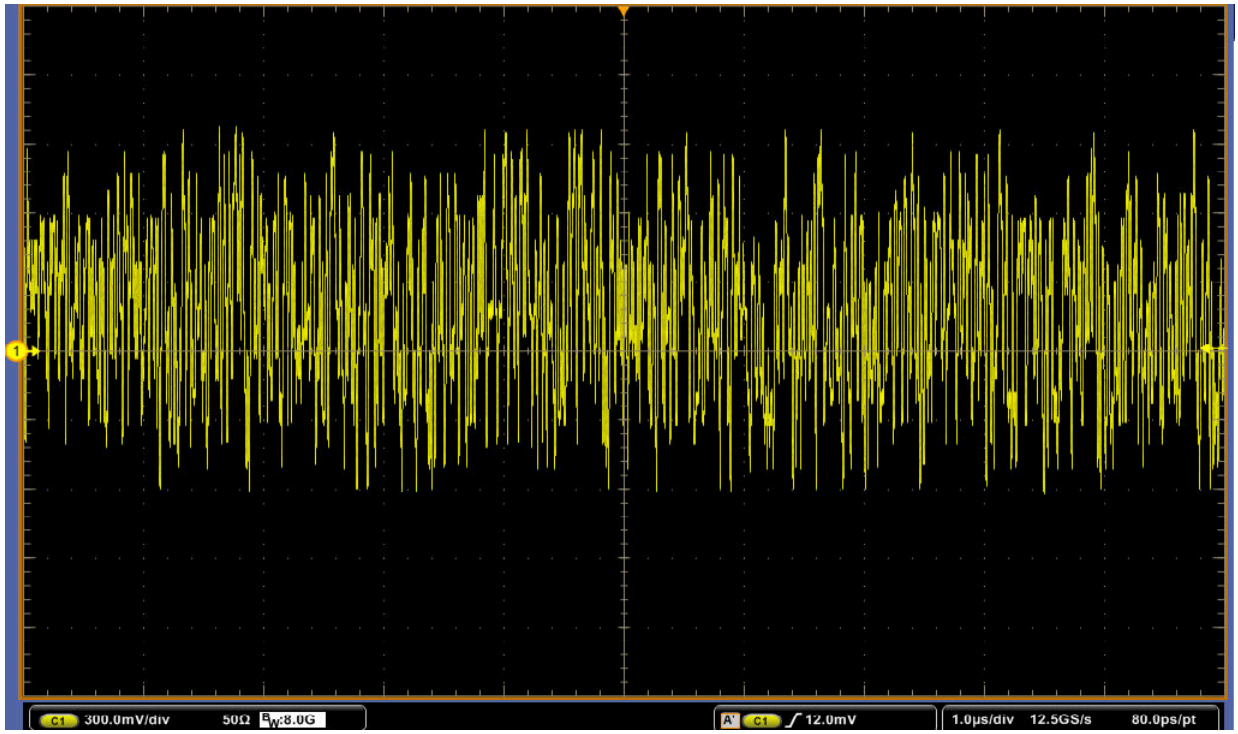

Figure 2-7. DP8386x Test Mode 4 Output Waveform

2.2.3.1 Distortion

Purpose: To make sure that the peak distortion is within the specified bounds.

Pass Condition: The peak distortion of the output differential signal should be less than 10 mV when sampled with TX_TCLK for at least 60% of the Unit Interval (UI) for 2047 consecutive samples at an arbitrary phase.

Specific Test Setup: Verify the correct test fixture connections.

A disturbing signal of 2.7 Vpp at 20.8 MHz is required to pass Distortion test (please see Ethernet Compliance Software's Manual for setup).

Also, verify that the Ethernet Compliance software is adhering to the "at least 60% of Unit Interval (UI) for 10 mV", not 100% (for example, TDSET uses 100% of UI, so failures are seen even with compliant parts).

2.2.3.2 Common-Mode Voltage

Purpose: To make sure that the Common-Mode Voltage is within the specified bounds.

Pass Condition: The magnitude of the Common-Mode Voltage needs to be within 50 mVpp.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 4 by setting MDIO registers according to 1000 Base Test Mode 4 in Appendix B.

Connect the DUT ground to test fixture ground for proper measurements (as outlined in IEEE 802.3 in Figure 2-8).

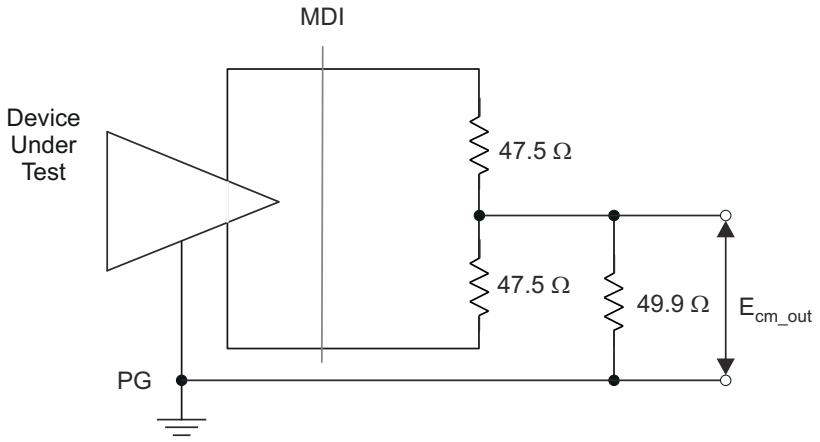

Figure 2-8. IEEE Defined CM Voltage Test Setup

2.2.3.3 Return Loss

Purpose: To make sure that the return loss is above the specified attenuation.

Pass Condition: The reflection of any incident signal to the PHY must be attenuated:

≥16 dB over the frequency range of 1.0 MHz to 40 MHz

≥10 – 20log 10 (f /80) dB over the frequency range 40 MHz to 100 MHz (f in MHz)

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 4 by setting MDIO registers according to 1000 Base Test Mode 4 in Appendix B. Note: A spectrum analyzer might be needed depending on Ethernet Compliance Software.

2.2.3.4 Common-Mode Noise Rejection

Purpose: Verify that the PHY's common-mode rejection ratio is within the specified bounds.

Pass Condition: See IEEE 802.3 40.6.1.3.

Specific Test Setup: Verify the correct test fixture connections. Configure the PHY according to 1000 Base Test Mode 4 in Appendix B.

2.3 100BASE-TX

Refer to Appendix B for 100BASE-TX register writes. Use MDI and MDIX configurations as needed. Test Mode 5 or forcing 100Mbps speed operation can be used. Note that some Ethernet compliance software can run Template, Differential Output Voltage, Signal Amplitude Symmetry, Rise and Fall Time, Overshoot, Jitter, and Duty Cycle Distortion tests simultaneously.

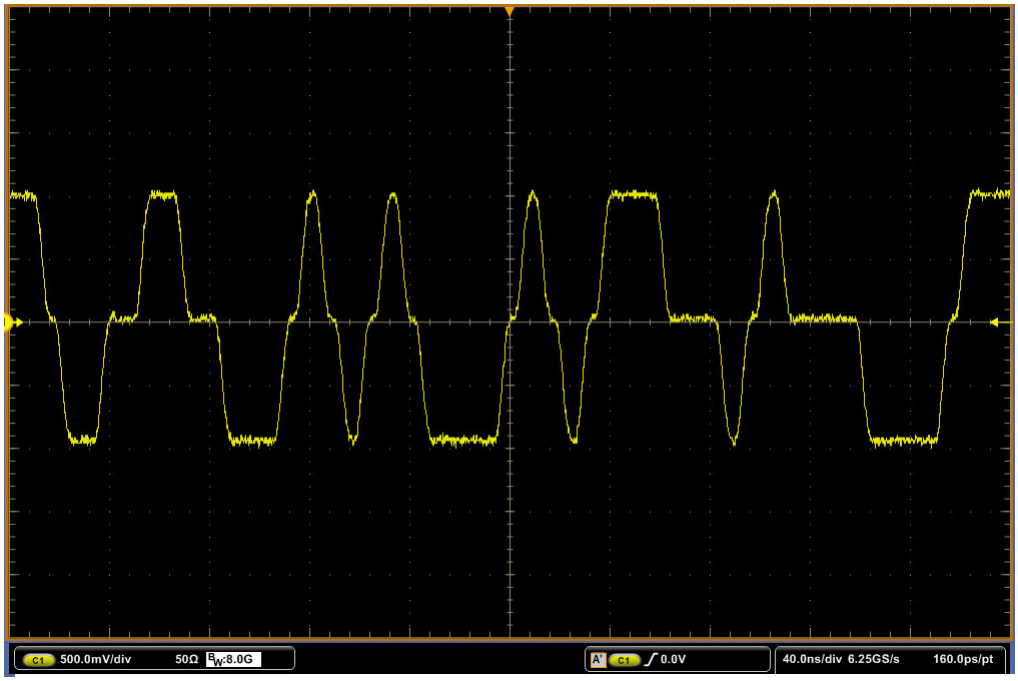

Figure 2-9. DP8386x Scrambled Idles Output Waveform 100M (Test Mode 5)

2.3.1 Template (Active Output Interface)

Purpose: To make sure that the output fits the transmit template.

Pass Condition: Fit into the specified ANSI Active Output Interface template.

2.3.2 Differential Output Voltage

Purpose: To make sure the differential output voltage is within the specified bounds.

Pass Condition: The differential output voltage needs to be within a positive or negative 950–1050 mV.

2.3.3 Signal Amplitude Symmetry

Purpose: To make sure the Signal Amplitude Symmetry is within the specified bounds.

Pass Condition: The ratio of the positive peak to negative peak amplitudes needs to be within 2% or $0.98 \leq |+V_{OUT}| / |-V_{OUT}| \leq 1.02$

2.3.4 Rise and Fall Time

Purpose: To make sure that the device rise and fall time are within the specified bounds.

Pass Condition: The rise and fall time (between 10% and 90% voltage levels for both positive and negative) needs to be between 3 ns and 5 ns. The maximum and minimum rise and fall times needs to be within 0.5 ns.

2.3.5 Waveform Overshoot

Purpose: To make sure that the waveform overshoot is below the specified bound.

Pass Condition: The overshoot (both positive and negative maximum voltage level on transition) must not exceed 5% over the steady state voltage level.

2.3.6 Jitter

Purpose: To make sure that the transmit output jitter is within the specified bounds.

Pass Condition: The transmit output jitter needs to be less than 1.4 ns.

2.3.7 Duty Cycle Distortion

Purpose: To make sure that the duty cycle distortion is below the specified bound.

Pass Condition: The duty cycle distortion (defined as above and below 50% of Vout) must not exceed ±0.25 ns.

2.3.8 Return Loss

Purpose: To make sure that the return loss is above the specified attenuation.

Pass Condition: The reflection of any incident signal to the PHY must be attenuated:

≥16 dB over the frequency range of 2 MHz to 30 MHz

≥10 – 20log 10 (f /30) dB over the frequency range 30 MHz to 60 MHz (f in MHz)

≥10 dB over the frequency range 60 MHz to 80 MHz

Specific Test Setup: Verify the correct test fixture connections. Configure PHY according to 100 Base Standard mode in Appendix B. Note a spectrum analyzer might be needed depending on Ethernet Compliance Software.

2.3.9 Common-Mode Voltage

Purpose: To make sure the common-mode voltage is within the specified bounds.

Pass Condition: The magnitude of the common-mode voltage needs to be less than 50mV peak.

Specific Test Setup: Verify the test fixture connections. Configure the PHY by setting MDIO registers according to 100 Base Standard mode in Appendix B

2.3.10 Common-Mode Noise Rejection

Purpose: Verify that the PHY's common-mode rejection ratio is within the specified bounds.

Pass Condition: See ANSI X3-263-1995 9.2.3

Specific Test Setup: Verify the correct test fixture connections. Configure the PHY by setting MDIO registers according to 100 Base Standard mode in Appendix B.

2.4 10BASE-Te

Refer to Appendix B for 10BASE-Te register writes. There are two scripts required for testing: one for link pulse and one for the remaining tests.

Note

DP8386x supports only 10BASE-Te mode of operation, not 10BASE-T. Please verify the scope supports the standard when performing compliance testing.

2.4.1 Link Pulse

Purpose: To make sure that the link pulse waveform is within the specified bounds.

Pass Condition: The link pulse must fit into the IEEE-defined template for loads 1 and 2 with and without the twisted pair model (TPM). Load 3 (100 Ω) is an informative test and is optional.

Specific Test Setup: Verify the test fixture connections. Set MDIO registers according to *10 Base Link Pulse* in Appendix B.

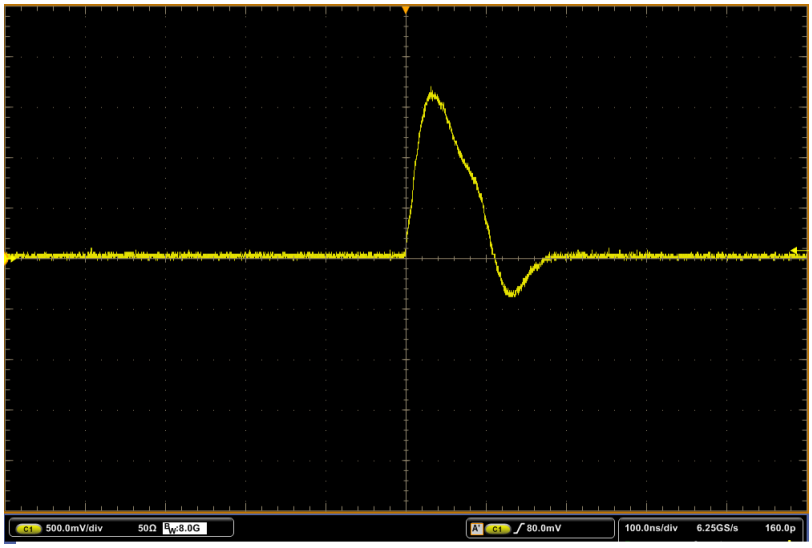

Figure 2-10. DP8386x Link Pulse Output Waveform 10M

2.4.2 10Base-Te Standard

Configure the PHY to output standard script in Appendix B. This configuration places the PHY in Digital Loopback and enables PRBS.

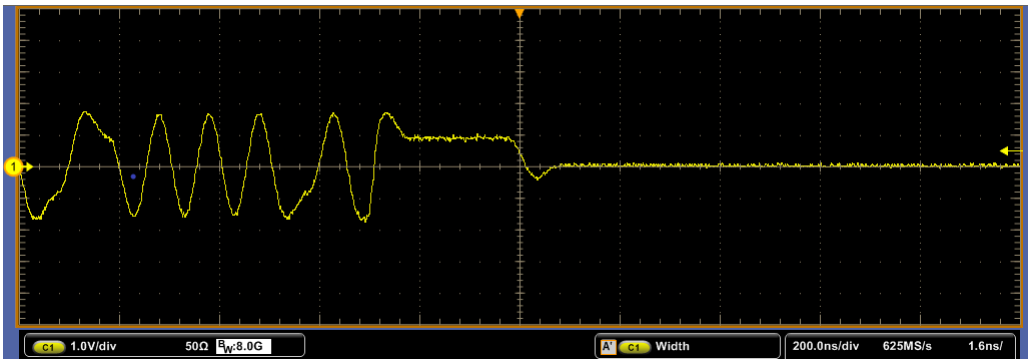

Figure 2-11. DP8386x 10Base-Te Standard

2.4.2.1 TP_IDL

Purpose: To make sure that the transmitter functions properly after transitioning to an idle state.

Pass Condition: The transmitter TP_IDL pulse must fit within the template for Loads 1 and 2 with and without the twisted pair model (TPM). Load 3 (100 Ω) is an informative test and is optional.

Specific Test Setup: Verify the test fixture connections.

2.4.2.2 MAU, Internal

Purpose: To make sure that the transmitter output equalization is within the specified bounds.

Pass Condition: The transmitter waveform needs to fit within the IEEE-defined template for all data sequences when terminated with a 100-Ω resistor.

Specific Test Setup: Verify the test fixture connections.

2.4.2.3 Jitter With TPM

Purpose: To make sure that the jitter is within the specified bounds.

Pass Condition: The transmitter output jitter needs be less than ±5.5 ns. Note: Failure with TPM does not necessarily mean noncompliance.

Specific Test Setup: Verify the test fixture connections.

2.4.2.4 Jitter Without TPM

Purpose: To make sure that the jitter is within the specified bounds.

Pass Condition: The transmitter output jitter needs to be less than ±8.0 ns.

Specific Test Setup: Verify the test fixture connections.

2.4.2.5 Differential Voltage

Purpose: To make sure that the differential voltage is within the specified bounds.

Pass Condition: The peak differential voltage needs to be between 2.2 V and 2.8 V when terminated with 100-Ω resistor for BASE-T. The peak differential voltage needs to be between 1.54 V and 1.96 V when terminated with 100-Ω resistor for 10BASE-Te.

Specific Test Setup: Verify the test fixture connections.

2.4.2.6 Common-Mode Voltage

Purpose: To make sure the common-mode voltage is within the specified bounds.

Pass Condition: The magnitude of the common-mode voltage needs to be less than 50-mV peak.

Specific Test Setup: Verify the test fixture connections. Configure the PHY to be in reverse loopback mode by setting MDIO registers according to 10 Base Standard in Appendix B

2.4.2.7 Return Loss

Purpose: To make sure that the return loss is above the specified attenuation.

Pass Condition: The reflection of any incident signal to the PHY must be attenuated:

≥ 15 dB over the frequency range of 5.0 MHz to 10 MHz

Specific Test Setup: Two waveform inputs might be necessary depending on testing setup. Verify the correct test fixture connections. Configure the PHY to be in reverse loopback mode by setting MDIO registers according to 10 Base Standard in Appendix B. Note a spectrum analyzer might be needed depending on Ethernet Compliance Software.

2.4.2.8 Harmonic Content

Purpose: To make sure the harmonic content of the PHY is within the specified bounds.

Pass Condition: The Data Out circuit must drive all ones or zeros. All subsequent harmonics must be 27-dB below the fundamental.

Specific Test Setup: Verify the test fixture connections. Configure the PHY by setting MDIO registers according to 10 Base Harmonic Content in Appendix B.

2.4.2.9 Common-Mode Rejection

Purpose: Verify that the PHY's common-mode rejection ratio is within the specified bounds.

Pass Condition: See IEEE 802.3 14.3.1.2.6

Specific Test Setup: Verify the correct test fixture connections. Set MDIO registers according to *10 Base Standard* in Appendix B.

3 Debug Test Methods

For more information on debugging compliance related issues, refer to SNLA246 for DP83867, and SNLA443 for DP83869.

4 References

1. *TDSET3 Manual*
2. ANSI X3.263-1995
3. Texas Instruments, *DP8382x IEEE 802.3u Compliance and Debug* , application note.
4. Texas Instruments, *DP83867E/IS/CS Robust, High Immunity, Small Form Factor 10/100/1000 Ethernet Phy*, data sheet.
5. Texas Instruments, *DP83867IR/CR High Immunity 10/100/1000 Ethernet Physical Layer Transceiver*, data sheet.
6. Texas Instruments, *DP83869HM High Immunity 10/100/1000 Ethernet Physical Layer Transceiver With Copper and Fiber Interface*, data sheet.

5 Revision History

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- Updated register configurations....16

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A Appendix A: Outline of Ethernet Compliance Tests for DP8386x

Table A-1 lists the Ethernet compliance tests for DP8386x.

Table A-1. Outline of Ethernet Compliance Tests for DP8386x

TEST	REGISTER CONFIGURATION (IN Appendix B)
1000BASE-T	
Template	1000 BASE Test Mode 1
Peak Voltage	
Droop	
Jitter Master Unfiltered	1000 Base Test Mode 2
Distortion	1000 Base Test Mode 4
Common Mode Voltage	
Common Mode Rejection	
Return Loss	
100BASE-TX	
Template	100 Base Standard
Differential Output Voltage	
Signal Amplitude Symmetry	
Rise and Fall Time	
Waveform Overshoot	
Jitter	
Duty Cycle Distortion	
Common Mode Voltage	
Common Mode Rejection	
Return Loss	
10BASE-Te	
Link Pulse	10 Base Link Pulse
TP_IDL	10 Base Standard
MAU, Internal	
Jitter with TPM	
Jitter without TPM	
Differential Voltage	
Common Mode Voltage	
Common Mode Rejection	
Return Loss	
Harmonic Content	

B Appendix B: Ethernet Compliance Testing MDIO Register Writes for DP8386x

1000 Base Test Mode 1

Reg 0x1F = 0x8000	//Reset PHY
Reg 0x0 = 0x0140	//1000 Base-T Mode, Autonegotiation disabled
Reg 0x10 = 0x5008	//Forced MDI Mode
Reg 0x9 = 0x3B00	//Test Mode 1
Reg 0x25 = 0x480	//Output test mode to all channels
Reg 0x1D5 = 0xF508	//Increases VoD swing. This register can be applied on the other test scripts as well as in end use-case applications.
Reg 0x1F = 0x4000	//Restart PHY

1000 Base Test Mode 2

Reg 0x1F = 0x8000	//Reset PHY
Reg 0x0 = 0x0140	//1000 Base-T Mode, Autonegotiation disabled
Reg 0x10 = 0x5008	//Forced MDI Mode
Reg 0x9 = 0x5B00	//Test Mode 2
Reg 0x25 = 0x480	//Output test mode to all channels
Reg 0x1F = 0x4000	//Restart PHY

1000 Base Test Mode 4

Reg 0x1F = 0x8000	//Reset PHY
Reg 0x0 = 0x0140	//1000 Base-T Mode, Autonegotiation disabled
Reg 0x10 = 0x5008	//Forced MDI Mode
Reg 0x9 = 0x9B00	//Test Mode 4
Reg 0x25 = 0x400	//Single channel selection. It is important to change to appropriate channel under test //400: Channel A //420: Channel B //440: Channel C //460: Channel D
Reg 0x1F = 0x4000	//Restart PHY

100 Base Standard

Reg 0x1F = 0x8000	//Reset PHY
Reg 0x0 = 0x2100	//Programs DUT to 100Base-TX Mode
Reg 0x10 = 0x5008	//Programs DUT to Forced MDI or MDIX mode (0x5028)
Reg 0x1F = 0x4000	//Restart PHY

10 Base Link Pulse

Reg 0x1F = 0x8000	//Reset PHY
Reg 0x0 = 0x100	//Programs DUT to 10Base-Te Mode
Reg 0x10 = 0x5008	//Programs DUT to Forced MDI Mode or MDIX mode (0x5028)
Reg 0x1F = 0x4000	//Restart PHY

10 Base Standard

Reg 0x1F = 0x8000	//Reset PHY
Reg 0x0 = 0x100	//Programs DUT to 10Base-Te Mode
Reg 0x10 = 0x5008	//Programs DUT to Forced MDI Mode or MDIX mode (0x5028)
Reg 0x16 = 0xD004	//Programs DUT to generate traffic
Reg 0x1F = 0x4000	//Restart PHY

10 Base Harmonic Content

Reg 0x1F = 0x8000	//Reset PHY
Reg 0x0 = 0x100	//Programs DUT to 10Base-Te Mode
Reg 0x10 = 0x5008	//Programs DUT to Forced MDI Mode or MDIX mode (0x5028)
Reg 0x25 = 0x0413	//Programs DUT to generate repetitive ones

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