Application Report
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DP83867IRPAP Power Consumption Data

Aniruddha Khadye

ABSTRACT

Power consumption on an Ethernet PHY is affected by different operating conditions. System design around Ethernet products requires accurate power consumption numbers for component selection, thermal management and power distribution planning. This application report details power consumption of DP83867 in different conditions.

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1 Introduction

Power consumption data mentioned in the datasheet is accurate for typical operating conditions. However, Ethernet transceiver power consumption is affected by the operating conditions. This application report details the key factors affecting the power consumption.

This application report is applicable to the following devices;

DP83867IRPAP

2 Factors Affecting Power Consumption

Power consumption is affected by several operating conditions like I/O pin loading, packet payload, channel utilization, cable length, operational mode and Temperature.

Power mentioned in Section 4.1 can be used as benchmark for comparison.

2.1 Operational Mode

Power consumption depends on the operational mode of the PHY. Depending on the data rate selected, the PHY has different signaling which affects the data coding, voltage and operating frequency. This in turn affects the power demand by the PHY.

See Appendix Section 6.1, Section 6.2 and Section 6.3 for observing the power variation due to change in operational mode.

2.2 I/O Pin Loading

Digital I/O pin loading affects the power consumption of the PHY. Digital I/O pins include clock output pins, general-purpose output pins, and MII digital output pins. For example, 6 digital outputs driving 5 pF loads at 25 MHz can result in a current demand of 15 mA in a typical application. Power demand can be reduced by making MII signal traces as short as possible, and by adding series termination to the MII output signals. Some PHYTER products include integrated digital output series resistance. For more details, see the device-specific datasheets

Higher voltage level on the Digital I/O pins also leads to higher power consumption. See Appendix Section 6.1 for observing the power variation due to change in VDDIO voltage.

2.3 Channel Utilization

Channel Utilization is defined by the length of inter-packet gap. Channel utilization can be increased by decreasing the interpacket gap. Increasing the channel utilization also increases the transitions on I/O pins which increases power consumption.

See Appendix Section 6.4 for observing power consumption variations due to change in channel utilization.

2.4 Payload

The size of data packets has a definite impact on power consumption. When the size of data packets is increased it leads to higher transitions on the I/O pins. This increases power consumption.

2.5 Temperature

Operating temperature also affects the power consumption of the PHY. Higher ambient temperature means higher power consumption.

Temperature has the least amount of influence on total power consumption because PHYTER products are designed to internally compensate temperature variations.

3 Power Saving Modes

See Appendix Section 6.5 for observing the power consumption of the PHY in Power Down modes.

3.1 IEEE Power Down

The PHY is powered down except for essential functions. Access to the PHY via MDIO-MDC pins is retained. This mode can be activated by asserting external PWDN pin or by setting bit 11 of BMCR (Register 0x00).

The PHY can be taken out of this mode by a power cycle, software reset or by writing 0 to bit 11 in BMCR register. However, the external PWDN pin should be de-asserted. If the PWDN pin is kept asserted then the PHY will remain in power down.

3.2 Deep Power Down Mode

Deep Power Down is same as IEEE power down but the XI pad will also be turned off. This mode can be activated by asserting the external PWDN pin or by setting bit 11 of BMCR (Register 0x00). Before activating this mode, it is required to set bit 7 for PHYCR(Register 0x10).

The PHY can be taken out of this mode by a power cycle, software reset or by writing 0 to bit 11 in BMCR register. Additionally, the external PWDN pin should be de-asserted. If the PWDN pin is kept asserted then the PHY will remain in power down.

3.3 Active Sleep

In this mode all the digital and analog blocks are powered down. The PHY is automatically powered up when a link partner is detected. This mode is useful for saving power when the link partner is down/inactive but the PHY cannot be powered down. In Active Sleep mode, the PHY will still routinely send NLP to the link partner. This mode can be active by writing 1 to bit 9 and 0 to bit 8 for PHYCR (Register 0x10).

3.4 Passive Sleep

Passive sleep is just like Active sleep except the PHY does not send NLP. This mode can be activated by writing 1 to bits 9 and 8 of PHYCR (Register 0x10).

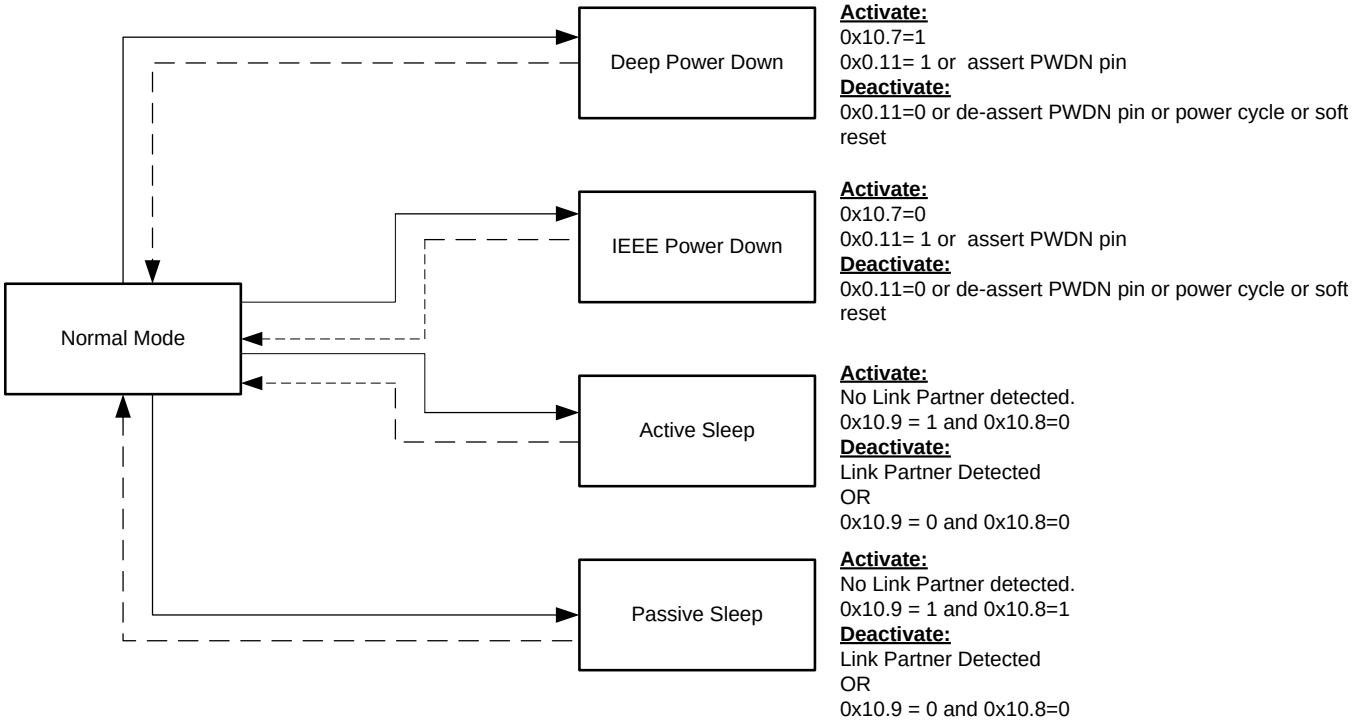

Figure 1. Power Saving Modes State Diagram

4 Power Consumption Baseline Data

The power consumption of the PHY can vary with all of the factors listed above. For the scope of this Application report, the PHY's power consumption with respect to Operating Mode, Supply type, VDDIO voltage and temperature is listed below. Also, the power numbers are measured after the optimization techniques listed above. The parameters for the tests are 1518 byte Packet size, 50% utilization, 100m cable length and random data pattern. The packet size, cable length and data pattern are selected to mimic the worst case conditions. The utilization is selected to be a worst case for most of the real world applications. As mentioned above, increasing the utilization will result in increase in power consumption.

The power numbers listed below were measured on a limited number of samples in a lab environment. Data is presented in a column format with current consumed by individual supplies listed with the total power number.

4.1 Base Line Power Consumption

The baseline power consumption number for each mode is measured by setting the following parameters. These numbers serve as a benchmark for observing changes in power consumption with change in parameters.

- Temperature: 25 °C
- Channel Utilization: 50%
- Cable Length: 100m
- VDDIO: 1.8V

Table 1. 1000M Triple Supply Baseline Power

Mode	Total Power (mW)	VDDIO			VDD2P5			VDD1P1			VDD1P8		
		V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)
1000	482	1.8	19	34	2.5	90	225	1.1	120	132	1.8	50	90
100	209	1.8	7	13	2.5	47	116	1.1	42	46	1.8	19	33
10	253	1.8	6	10	2.5	78	194	1.1	31	34	1.8	8	15

Table 2. 1000M Dual Supply Baseline Power

Mode	Total Power (mW)	VDDIO			VDD2P5			VDD1P1		
		V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)
1000	521	1.8	20	37	2.5	141	352	1.1	120	132
100	222	1.8	8	15	2.5	64	161	1.1	42	46
10	263	1.8	6	12	2.5	86	215	1.1	33	36

5 Summary

The data above shows the operating conditions have a significant impact on the power consumption of the PHY. Voltage levels of the I/O pins and supply mode are the major factors affecting the power consumption.

6 Appendix

All power consumption numbers are for 50% utilization, unless specified otherwise.

6.1 1000M Power

Table 3. 1000M Triple Supply

Temp (°C)	Total Power (mW)	VDDIO			VDD2P5			VDD1P1			VDD1P8		
		V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)
-40	469	1.8	13	23	2.5	91	227	1.1	116	128	1.8	50	90
-40	513	2.5	26	65	2.5	92	230	1.1	116	128	1.8	50	90
-40	564	3.3	35	116	2.5	92	230	1.1	116	128	1.8	50	90
25	482	1.8	19	34	2.5	90	225	1.1	120	132	1.8	50	90
25	515	2.5	26	66	2.5	90	226	1.1	120	132	1.8	50	91
25	565	3.3	35	117	2.5	90	225	1.1	120	132	1.8	50	91
85	498	1.8	21	37	2.5	89	222	1.1	134	148	1.8	51	91
85	532	2.5	29	71	2.5	89	222	1.1	134	148	1.8	51	91
85	583	3.3	37	123	2.5	89	221	1.1	134	148	1.8	51	91

Table 4. 1000M Dual Supply

Temp (°C)	Total Power (mW)	VDDIO			VDD2P5			VDD1P1			VDD1P8		
		V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)
-40	520	1.8	20	36	2.5	142	356	1.1	116	128	0	0	0
-40	550	2.5	26	66	2.5	142	356	1.1	116	128	0	0	0
-40	599	3.3	35	115	2.5	142	356	1.1	116	128	0	0	0
25	521	1.8	20	37	2.5	141	352	1.1	120	132	0	0	0
25	552	2.5	27	68	2.5	141	352	1.1	120	132	0	0	0
25	602	3.3	36	118	2.5	141	352	1.1	120	132	0	0	0
85	534	1.8	21	37	2.5	140	349	1.1	134	148	0	0	0
85	568	2.5	28	71	2.5	140	349	1.1	134	148	0	0	0
85	619	3.3	37	122	2.5	140	349	1.1	134	148	0	0	0

6.2 100M Power

Table 5. 100M Triple Supply

Temp (°C)	Total Power (mW)	VDDIO			VDD2P5			VDD1P1			VDD1P8		
		V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)
-40	209	1.8	5	9	2.5	49	122	1.1	39	43	1.8	19	35
-40	220	2.5	9	23	2.5	48	119	1.1	39	43	1.8	19	34
-40	240	3.3	14	45	2.5	48	119	1.1	39	43	1.8	19	33
25	209	1.8	7	13	2.5	47	116	1.1	42	46	1.8	19	33
25	225	2.5	11	27	2.5	47	116	1.1	42	46	1.8	19	35
25	246	3.3	15	50	2.5	47	117	1.1	42	46	1.8	19	34
85	224	1.8	8	15	2.5	46	114	1.1	56	62	1.8	19	34
85	236	2.5	11	27	2.5	46	114	1.1	56	62	1.8	19	34
85	257	3.3	15	49	2.5	45	114	1.1	56	62	1.8	19	34

Table 6. 100M Dual Supply

Temp (°C)	Total Power (mW)	VDDIO			VDD2P5			VDD1P1			VDD1P8		
		V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)
-40	222	1.8	7	13	2.5	66	166	1.1	39	43	0	0	0
-40	233	2.5	10	25	2.5	66	165	1.1	39	43	0	0	0
-40	253	3.3	14	45	2.5	66	166	1.1	39	43	0	0	0
25	222	1.8	8	15	2.5	64	161	1.1	42	46	0	0	0
25	238	2.5	11	29	2.5	65	163	1.1	42	46	0	0	0
25	259	3.3	15	50	2.5	65	163	1.1	42	46	0	0	0
85	238	1.8	8	15	2.5	65	161	1.1	56	62	0	0	0
85	251	2.5	11	28	2.5	65	161	1.1	56	62	0	0	0
85	271	3.3	15	48	2.5	64	161	1.1	56	62	0	0	0

6.3 10M power

Table 7. 10M Triple Supply

Temp (°C)	Total Power (mW)	VDDIO			VDD2P5			VDD1P1			VDD1P8		
		V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)
-40	261	1.8	6	11	2.5	81	203	1.1	30	33	1.8	8	15
-40	269	2.5	8	19	2.5	81	203	1.1	30	33	1.8	8	15
-40	288	3.3	11	37	2.5	81	203	1.1	30	33	1.8	9	16
25	253	1.8	6	10	2.5	78	194	1.1	31	34	1.8	8	15
25	263	2.5	8	21	2.5	77	194	1.1	31	34	1.8	8	15
25	281	3.3	11	38	2.5	78	194	1.1	31	34	1.8	8	15
85	267	1.8	6	12	2.5	75	188	1.1	48	52	1.8	8	15
85	279	2.5	9	23	2.5	75	188	1.1	48	52	1.8	8	15
85	295	3.3	12	40	2.5	75	188	1.1	48	52	1.8	8	15

Table 8. 10M Dual Supply

Temp (°C)	Total Power (mW)	VDDIO			VDD2P5			VDD1P1			VDD1P8		
		V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)
-40	267	1.8	6	11	2.5	89	223	1.1	30	33	0	0	0
-40	278	2.5	8	20	2.5	90	225	1.1	30	33	0	0	0
-40	293	3.3	11	37	2.5	89	223	1.1	30	33	0	0	0
25	263	1.8	6	12	2.5	86	215	1.1	33	36	0	0	0
25	273	2.5	9	22	2.5	86	215	1.1	33	36	0	0	0
25	289	3.3	12	38	2.5	86	215	1.1	33	36	0	0	0
85	273	1.8	7	12	2.5	84	210	1.1	47	52	0	0	0
85	285	2.5	9	23	2.5	84	209	1.1	47	52	0	0	0
85	302	3.3	12	40	2.5	84	209	1.1	48	52	0	0	0

6.4 Channel Utilization 1000M

Table 9. 1000M Triple Supply Power for Channel Utilization

Temp (°C)	Utilization (%)	Total Power (mW)	VDDIO			VDD2P5			VDD1P1			VDD1P8		
			V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)
25	0	465	1.8	12	22	2.5	90	225	1.1	114	125	1.8	50	90
25	50	482	1.8	19	34	2.5	90	225	1.1	120	132	1.8	50	90
25	100	507	1.8	29	51	2.5	90	225	1.1	127	140	1.8	50	90
25	0	488	2.5	18	45	2.5	90	225	1.1	114	125	1.8	50	90
25	50	515	2.5	26	66	2.5	90	226	1.1	120	132	1.8	50	91
25	100	552	2.5	37	93	2.5	90	225	1.1	129	141	1.8	50	90
25	0	520	3.3	23	77	2.5	90	225	1.1	114	126	1.8	50	90
25	50	565	3.3	35	117	2.5	90	225	1.1	120	132	1.8	50	91
25	100	621	3.3	50	165	2.5	90	225	1.1	128	140	1.8	50	90

Table 10. 1000M Dual Supply Power for Channel Utilization

Temp (°C)	Utilization (%)	Total Power (mW)	VDDIO			EXT2.5			VDD			EXT1.8		
			V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)	V (V)	I (mA)	Power (mW)
25	0	504	1.8	13	24	2.5	141	354	1.1	115	126	1.8	0	0
25	50	521	1.8	20	37	2.5	141	352	1.1	120	132	0	0	0
25	100	543	1.8	29	52	2.5	141	352	1.1	127	140	1.8	0	0
25	0	524	2.5	18	45	2.5	141	353	1.1	114	126	1.8	0	0
25	50	552	2.5	27	67	2.5	141	353	1.1	121	133	1.8	0	0
25	100	588	2.5	38	96	2.5	141	352	1.1	128	141	1.8	0	0
25	0	555	3.3	23	76	2.5	141	353	1.1	114	126	1.8	0	0
25	50	602	3.3	36	118	2.5	141	352	1.1	120	132	0	0	0
25	100	656	3.3	50	164	2.5	141	352	1.1	127	140	1.8	0	0

6.5 Power Down Consumption

Table 11. Deep Power Down

Triple/ Dual Supply	Total Power (mW)	VDDIO			VDD1P1			VDD2P5			VDD1P8		
		V (V)	I (mA)	Power(mW)	V (V)	I (mA)	Power(mW)	V (V)	I (mA)	Power(mW)	V (V)	I (mA)	Power(mW)
triple	30	1.8	5	8	1.1	13	14	2.5	2	6	1.8	1	1
triple	34	2.5	5	13	1.1	13	14	2.5	3	6	1.8	1	1
triple	49	3.3	8	27	1.1	13	14	2.5	3	6	1.8	1	1
dual	29	1.8	5	9	1.1	13	14	2.5	2	6	0	0	0
dual	34	2.5	5	13	1.1	13	14	2.5	2	6	0	0	0
dual	48	3.3	8	27	1.1	13	14	2.5	2	6	0	0	0

Table 12. IEEE Power Down

Triple/ Dual Supply	Total Power (mW)	VDDIO			VDD1P1			VDD2P5			VDD1P8		
		V (V)	I (mA)	Power(mW)	V (V)	I (mA)	Power(mW)	V (V)	I (mA)	Power(mW)	V (V)	I (mA)	Power(mW)
triple	31	1.8	5	8	1.1	13	14	2.5	3	8	1.8	1	1
triple	36	2.5	5	13	1.1	13	14	2.5	3	8	1.8	1	1
triple	50	3.3	8	27	1.1	13	14	2.5	3	8	1.8	1	1
dual	31	1.8	5	9	1.1	13	14	2.5	3	8	0	0	0
dual	35	2.5	5	13	1.1	13	14	2.5	3	7	0	0	0
dual	49	3.3	8	27	1.1	13	14	2.5	3	8	0	0	0

Table 13. Active Sleep

Triple/ Dual Supply	Total Power (mW)	VDDIO			VDD1P1			VDD2P5			VDD1P8		
		V (V)	I (mA)	Power(mW)	V (V)	I (mA)	Power(mW)	V (V)	I (mA)	Power(mW)	V (V)	I (mA)	Power(mW)
triple	108	1.8	6	11	1.1	20	23	2.5	24	59	1.8	9	15
triple	114	2.5	7	17	1.1	21	23	2.5	24	59	1.8	8	15
triple	131	3.3	10	34	1.1	21	23	2.5	24	59	1.8	8	15
dual	114	1.8	6	11	1.1	21	23	2.5	32	80	0	0	0
dual	121	2.5	7	17	1.1	21	23	2.5	32	80	0	0	0
dual	138	3.3	10	34	1.1	21	23	2.5	32	81	0	0	0

Table 14. Passive Sleep

Triple/Dual Supply	Total Power (mW)	VDDIO			VDD1P1			VDD2P5			VDD1P8		
		V (V)	I (mA)	Power(mW)	V (V)	I (mA)	Power(mW)	V (V)	I (mA)	Power(mW)	V (V)	I (mA)	Power(mW)
triple	108	1.8	6	11	1.1	21	23	2.5	24	59	1.8	8	15
triple	114	2.5	7	17	1.1	21	23	2.5	24	59	1.8	8	15
triple	131	3.3	10	34	1.1	21	23	2.5	24	59	1.8	8	15
dual	114	1.8	6	11	1.1	21	23	2.5	32	80	0	0	0
dual	121	2.5	7	18	1.1	21	23	2.5	32	81	0	0	0
dual	137	3.3	10	34	1.1	21	23	2.5	32	81	0	0	0

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