*Application Note*

# *Sending Power Over Coax in FPD-Link Designs*


**ABSTRACT**

Automotive applications continue to advance with new features such as 360-degree eye views and interior vehicle monitoring to check for driver awareness. To support these features multiple cameras must be installed around and within the vehicle, with each camera requiring additional hardware and cabling components. FPD-Link III devices can simplify automotive system designs by transmitting both video data and power over a single standard coaxial cable between the camera and serializer. This decreases weight, removes the need for separate power supplies, and minimizes cabling costs. This application note discusses the constraints involved in the power design portion of these applications as well as providing multiple Power-over-Coax (PoC) network solutions.


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## Trademarks

# 1 Introduction

Advanced driver assistance systems (ADAS) have become increasingly more complex including applications such as driver monitoring, driver assistance features, and in some cases autonomous driving. These systems often use multiple types of sensors and cameras spread across various locations of the vehicle. As the number of sensors and cameras continue to increase, the total length and number of cables required to transfer the high-speed data and power signals will increase as well. This results in extensive cabling, which is costly and can complicate system implementation.

FPD-Link SerDes chipsets eliminate the need to have a separate cable to deliver power from the deserializer board to the serializer and sensor, which allows ADAS systems to support an increased number of sensors without an extensive amount of cabling. This is achieved by using Power over Coax (PoC) filters to separate DC power from the high speed FPD-Link signal, allowing power to be transferred over the same coax cable as the FPD-Link data.

# 2 Theory of Operation for Power Over Coax

The purpose of a PoC network is to separate the high-speed data signal from the DC power signal. The high-speed signal consists of a high-speed forward channel carrying video and control data to the deserializer and a lower speed back channel carrying control data to the serializer. Figure 2-1 shows a high-level overview of how FPD-Link and DC power share a single coax cable. The DC power signal must be completely isolated from the DOUT pins of the serializer and the RIN pins of the deserializer. This is accomplished by placing AC coupling capacitors in line with the FPD-Link signal path, which blocks the DC signal and passes the forward and back channel data signals. A simple capacitor can work for this since it has very low impedance over the forward and back channel frequency and is an open circuit at DC.

The PoC network is a type of low pass filter circuit that is designed to pass the transmitted DC signal with minimal interference on the high-speed AC signal. For this low pass filter circuit to not interfere with the high-speed signal, the circuit needs to have an impedance much larger than the characteristic impedance of the channel. It is recommended that an impedance of 1 kΩ be met over the entire FPD-Link operational frequency band.

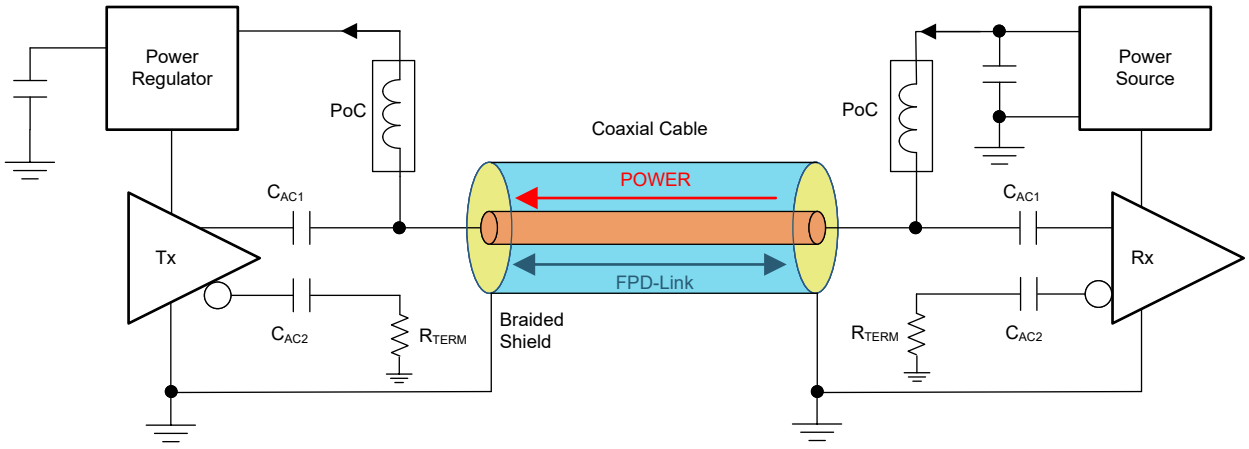


**Figure 2-1. Concept for Power Over Coax**

## 2.1 Inductor Characteristics

An ideal inductor is capable of blocking all AC frequencies and passing all DC power. However, inductors have characteristics that make them behave less like an inductor in extreme circumstances. Real-world inductors behave more closely to the circuit shown in Figure 2-2 with parasitic capacitance and resistance components. At low frequencies, the capacitor acts like an open circuit with high impedance, and the inductor acts like a short circuit with low impedance. At very high frequencies, the capacitor acts like a short circuit, at which point the impedance is equal to $R_L$.

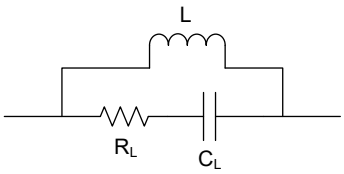


**Figure 2-2. Model for a Real-World Inductor**

The impedance peaks at the self-resonant frequency (SRF) where the inductor and capacitor resonate. At frequencies past the SRF, the parasitic capacitance takes over and lowers the impedance. The SRF can be calculated using Equation 1, where L is the inductance, C is the parasitic capacitance, and F is the resonant frequency. These values are typically listed in the component's data sheet.

$$F = \frac{1}{\sqrt{LC}} \tag{1}$$

The impedance of a 100 µH inductor is shown in Figure 2-3 where the black line shows the impedance of an ideal inductor before the SRF and the red line shows the impedance of the parasitic capacitance after the SRF.

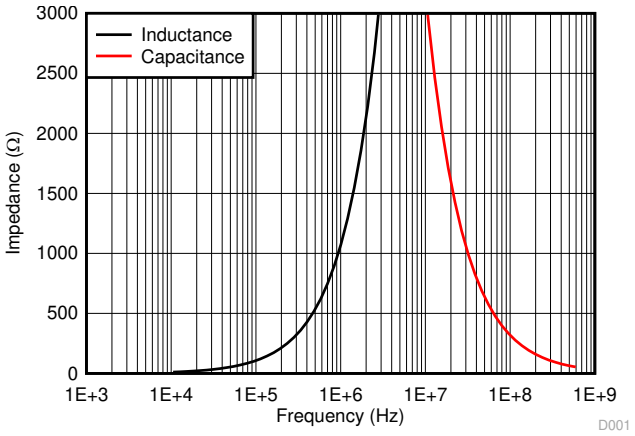


**Figure 2-3. Real-world Inductor Impedance - 100 µH Inductor**

Figure 2-3 shows that for a 100 µH inductor, the impedance rises above 1 kΩ at about 1 MHz and drops below 1 kΩ above frequencies of about 30 MHz. Although not strictly required, an impedance above 1 kΩ is recommended as high impedance correlates to lower signal loss. For this reason, a more complex low pass filter is required to raise the impedance over the entire FPD-Link bidirectional signaling frequency range.

To increase the impedance of the circuit over the entire operational frequency range, additional inductive components of different values can be added in series. Figure 2-4 shows the impedance of a 100 µH and 4.7 µH inductor individually and in series. Compared to the 100 µH inductor the 4.7 µH inductor has a higher SRF but still does not achieve a high impedance across a large frequency range. However, when used in series, the impedance remains above 1 kΩ from about 1 MHz to well over 500 MHz.

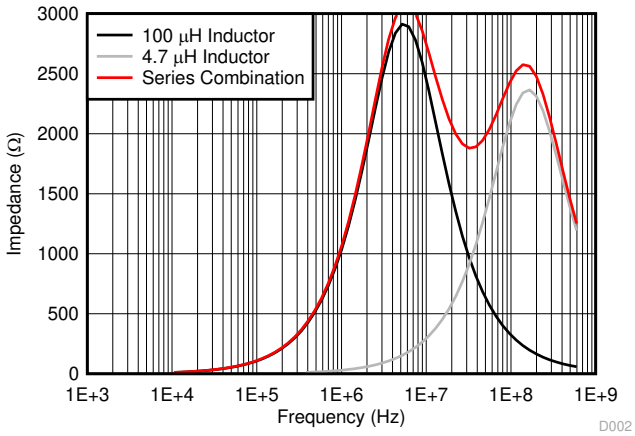


**Figure 2-4. Impedance of Series Inductors**

By cascading inductors in series, a wide-bandwidth inductor can be created to cover the entire range of frequencies across the back channel and the forward channel. This is demonstrated further in Figure 2-5 and Figure 2-6. Figure 2-5 shows impedance graphed for individual inductors of various values. The individual inductors do not provide an impedance of 1 kΩ over a wide frequency range. However, Figure 2-6 shows that when combined, the inductors provide consistent impedance of 1 kΩ over a large frequency range.

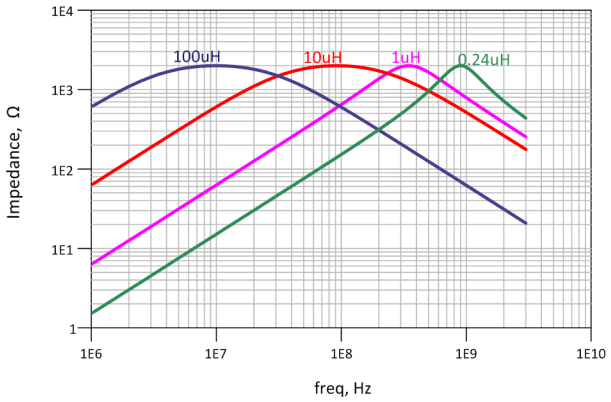


**Figure 2-5. Impedance of Individual Inductors**

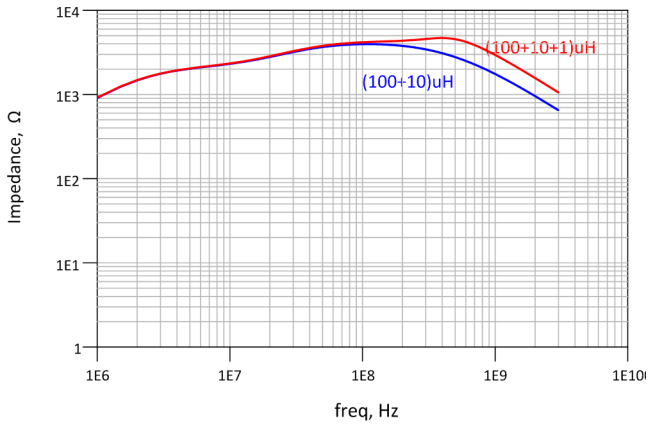


**Figure 2-6. Impedance of Combined Inductors**

An additional consideration when working with real-world inductors is the saturation current. Inductors store electrical energy in the form of a magnetic field. The strength of the magnetic field is correlated to the current flowing through the inductor. The saturation current is the maximum current that can be supported before the inductor ceases to behave like an ideal inductor. When implementing a PoC network, it is crucial to verify that the operating conditions do not exceed the max rated electrical characteristics of any component.

## 2.2 Capacitor Characteristics

Figure 2-7 shows a representative model of a real-world capacitor component. A capacitor has an accompanying parasitic resistance and inductance, and at very high frequencies the inductance takes over and the capacitor no longer behaves like a capacitor. If the impedance of the capacitor is plotted across a frequency range, the result looks similar to Figure 2-3 but flipped horizontally with the lowest impedance occurring at the resonant frequency.

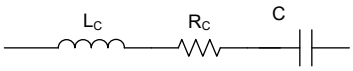


**Figure 2-7. Real-World Capacitor**

Capacitors are used in the PoC network for decoupling the input of DC regulators on the serializer side of the link. The input capacitance of the DC regulator is based on both the FPD-Link serializer and DC regulator recommendations found in the device data sheets. The chosen capacitors must have appropriate voltage and temperature ratings for the system. Similarly to how the inductors are cascaded in series to create a wide-bandwidth inductor, capacitors can be cascaded in parallel to create a wide-bandwidth capacitor, or a capacitor that can pass a larger frequency range and better decouple the DC regulators. Often times when choosing a decoupling capacitor, the capacitor can be treated as an ideal capacitor because noise from the DC regulators is at a much lower frequency than the signal frequency trying to be blocked. Equation 2 shows the impedance of a capacitor as a function of frequency, where Z is the impedance in Ohms, f is the frequency in Hertz, and C is the capacitance in Farads.

$$Z = \frac{1}{\sqrt{2\pi f C}} \tag{2}$$

## 2.3 Ferrite Bead Characteristics

As the frequency of FPD-Link communications rise, the need for more complex PoC networks follows. Ferrite beads can help greatly when dealing with extremely high frequencies. Ferrite beads are special kinds of inductors that have very low inductance but are rated for frequencies in the MHz to GHz range. Where standard coil inductors typically begin behaving like a capacitor, a ferrite bead can continue to provide high impedance. Figure 2-8 shows a real-world ferrite bead that has an inductive component, capacitive component, and resistive components. The Ferrite bead is primarily inductive, therefore $L_{FB}$ is the most dominant portion of this model. The parasitic capacitance $C_{Par}$ does not become significant until very high frequencies.

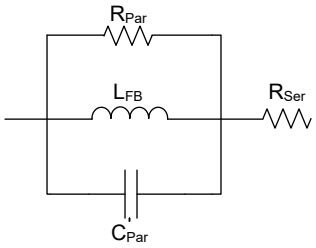


**Figure 2-8. Real-World Ferrite Bead**

Adding ferrite beads to the PoC network can result in broader frequency coverage. However, a ferrite bead can have a higher resistive component at DC than a standard coil inductor. While the resistance is typically rather small (<1Ω), higher DC resistance can result in significant IR drop in applications where current is drawn.

# 3 Design Considerations

There are two main functional factors to consider when selecting a PoC network: device operational frequency range and power consumption of the serializer or imager board.

## 3.1 Frequency Range

To design an appropriate PoC network, consider the frequency range that the network must be able to filter. The operational frequency range of FPD-Link communication depends on the particular device pairing and mode configuration.

For example, a system using the DS90UB953-Q1 and DS90UB954-Q1 running in synchronous mode with a reference clock of 26 MHz will operate with a forward channel rate of 4.16 Gbps (up to 2.1 GHz) and a back channel of 50 Mbps (down to 25 MHz). So the chosen PoC network needs to support a frequency range of 25 MHz to 2.1 GHz. However, the same devices running in non-synchronous external clock mode with a reference clock of 26 MHz will operate with a forward channel rate of 2.08 Gbps (up to 1.04 GHz) and a back channel of 10 Mbps (down to 5 MHz). For this configuration, the chosen PoC network needs to support a frequency range of 5 MHz to 1.04 GHz. Understanding the operational frequency is particularly important for designs that may potentially support multiple configurations.

Table 3-1 shows some common SerDes configurations and their forward and back channel communication frequencies. The last column shows the frequency range that the PoC network must be able to filter. For additional details on device compatibility and mode configurations, please refer to the respective device data sheets.

**Table 3-1. PoC Frequency Ranges**

| Serializer | Deserializer | Mode | Clock | BC Frequency | FC Frequency | PoC Filter Frequency Range |
|---|---|---|---|---|---|---|
| DS90UB913A-Q1 | DS90UB914-Q1 | 12 Bit LF | 50 MHz | 2.5 MHz | 700 MHz | 1.25 MHz - 700 MHz |
| DS90UB933-Q1 | DS90UB934-Q1 | 12 Bit | 100 MHz | 2.5 MHz | 935 MHz | 1.25 MHz - 935 MHz |
| DS90UB933-Q1 | DS90UB954-Q1 | 10 Bit | 100 MHz | 2.5 MHz | 700 MHZ | 1.25 MHz - 700 MHZ |
| DS90UB953-Q1 | DS90UB934-Q1 | DVP | 25 MHz | 2.5 MHz | 350 MHZ | 1.25 MHz - 350 MHZ |
| | DS90UB954-Q1 | Synchronous | 26 MHz | 50 MHz | 2.1 GHZ | 25 MHz - 2.1 GHZ |
| | DS90UB954-Q1 | Non-Synchronous | 52 MHz | 10 MHz | 2.1 GHz | 5 MHz - 2.1 GHz |

## 3.2 Power Considerations

Each PoC network has a maximum current rating based on the saturation characteristics of the components. As discussed in Section 2.1, inductors saturate, dissipate heat, and pass very high frequencies when the maximum current rating is not respected. The individual operating specifications of every PoC component must be followed to provide proper filtering.

The PoC network must have a current rating that allows for an appropriate amount of power to be supplied to the serializer and sensor. The maximum power drawn by the serializer board can be calculated from the worst-case scenario power consumption of the serializer side of the link. An example of a potential maximum power consumption scenario is a period where the sensor is actively gathering data and all other remote devices are operating. Please note that the worst-case scenario and maximum power consumption is system dependent and can vary across designs. The IR drop due to the parasitic impedance of the individual components and cables must also be considered. TI recommends several different PoC networks capable of different levels of power delivery. The chosen PoC network must be capable of supplying enough current and power from the given PoC voltage for the serializer and sensor.

## 3.3 Inductor Size Considerations

Although not required for functionality, some systems have size constraints that must be considered when designing a PoC network. The values of the inductors used are based on the impedance and filtering needs of the system, but the physical size of the inductors is dependent on the ability of the device core to sustain the magnetic field. Physically smaller inductors have lower saturation currents and limit the current rating of the PoC network. One way to safely use an inductor with a lower saturation current is to reduce the current requirement

of the circuit by increasing the voltage being carried by the coax cable. For example, if the camera or sensor requires 1.5 W and a PoC voltage of 5 V is used, a current of 300 mA must be supported. However, if a PoC voltage of 12 V is used, a current of only 125 mA must be supported. The lower current requirement allows for an inductor with a lower saturation current and potentially smaller footprint to be used.

### 3.4 Layout Considerations

The layout of the PoC network is equally important as the network design. Due to the PoC network components making direct contact with the high-speed signal trace, good layout techniques and component placement are crucial to maintain signal integrity and remain within the insertion loss and return loss requirements. Both the high-speed channel and PoC network require tightly controlled 50-Ohms (+/-10%) impedance to minimize reflections. In addition to impedance, the PCB traces need to be thick enough to support the maximum expected current load.

Place the first inductive component of the PoC network orthogonally to be barely touching the high-speed RIN+ trace. An anti-pad must be added under the first component to keep the impedance as close to 50-Ohms as possible. The anti-pad is created by adding a cut-out to the ground plane directly underneath the component's landing pad. Since a continuous ground reference is required for the high-speed and PoC traces, the cut-out must not include any area under the connecting trace. Place the remaining PoC components close together to minimize the total footprint of the PoC network and limit 90-degree routing. For best EMI performance, do not route any high-frequency signals, including the PoC network, near the edge of the PCB board. Figure 3-1 shows an example PoC PCB layout with many of the previously described recommendations highlighted.

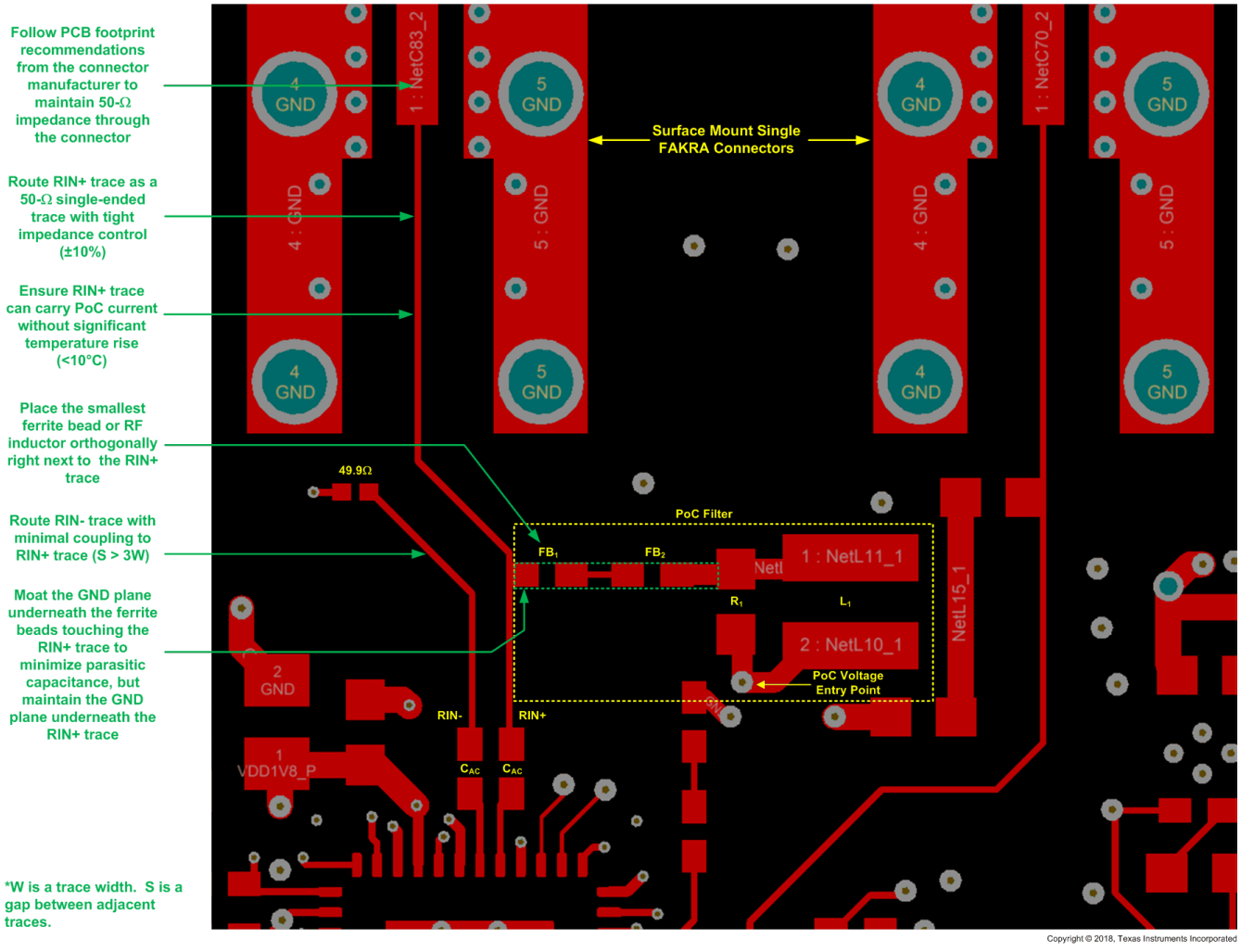


**Figure 3-1. Example PoC Layout and Routing**

Keeping the entire PoC network on the same layer as the high-speed RIN+ trace is recommended since vias can result in impedance discontinuities. However, if space constraints arise, all components other than the first inductive component can be routed to a layer other than the layer with the high-speed trace. To maintain the 50-Ohm impedance, add ground reference vias near all signal vias. When sending signals between layers, care needs to be taken to avoid creating stubs. A stub is any transmission line that is only connected at one end. Stubs are commonly created by vias, routing, or through-hole connectors, which create reflections and degrade the signal quality.

For additional recommendations, refer to device data sheets.

# 4 FPD-Link PoC Requirements

When incorporating a PoC network into a system, the user must make sure that any PoC network chosen meets TI's channel specifications and PoC noise requirements to provide robust operation across all component tolerances and operating conditions.

## 4.1 Channel Requirements

For error-free communication between FPD-Link devices, the return loss and insertion loss on the high-speed channel must be within the limits defined by TI under worst-case current load and temperature conditions. The high-speed channel includes the serializer PCB, cable, and deserializer PCB. A PoC network is only one part of the PCB budget and overall total channel requirement. The traces on each PCB, connectors, as well as any components touching the high-speed trace can all impact loss on the channel. For this reason the layout and quality of the selected components and cables are paramount.

TI defines the channel requirements in terms of budgets for the total channel, PCB, and cable, where total channel is a combination of the PCB and cable budgets. Although meeting both the PCB and cable budgets individually is recommended, the main requirement is meeting the total channel budget. This allows for some flexibility as a PoC network that slightly violates the PCB budget, can still meet the total channel budget if a shorter or more high-quality cable is used to compensate for the additional loss. Similarly, if a lossy cable violates the cable budget, the total channel loss requirement can still be met if the PCB design results in additional margin within the PCB budget. As long as the combined PCB and cable loss is within the total channel budget, the channel specifications are considered met. However, meeting each budget with as much margin as possible is recommended. When evaluating the insertion and return loss via simulation or measurements, the system must be stressed under the maximum temperature conditions and current load.

The return loss requirement protects against signal degradation. Return loss refers to the amount of reflections in the link seen by the transmitter. A network typically fails the return loss requirement when there is an impedance mismatch in the channel. A network can also fail when inductors and ferrite beads have been chosen incorrectly. Return loss can be calculated using Equation 3.

$$Return\ Loss(dB) = 10\log_{10}\left(\frac{P_{out}}{P_{in}}\right) \quad (3)$$

Following the FPD-Link and PoC layout guidelines from the data sheet is important to make sure the return loss requirement is met. If a board has already been designed and does not meet return loss requirements, a TDR test can be useful to help locate the area of the board where impedance mismatches occur. The return loss requirement for a FPD-Link III coax application is given in Table 4-1. For robust operation of the system, the return loss must be less than the listed values over the operating frequency range of the system. Contact TI for more information on the required Channel Specifications defined for each individual FPD-Link device and mode of operation.

**Table 4-1. Return Loss Requirement**

| Frequency | PCB Budget (dB) | Total Budget (dB) | Cable Budget (dB) |
|---|---|---|---|
| 1 – 100MHz | -20 | -16 | -20 |
| 0.1 – 1GHz | -12 + 8×log(f[ GHz]) | -9 + 7×log(f[ GHz]) | -12 + 8×log(f[ GHz]) |
| 1 – 2.1GHz | -12 | -9 | -12 |

Insertion loss refers to the amount of power the signal loses as the signal travels through the channel. Causes of insertion loss requirements not being met are typically due to signal attenuation in the channel and can be calculated using Equation 4.

$$Insertion\ Loss(dB) = -10\log_{10}\left(\frac{P_{out}}{P_{in}}\right) \quad (4)$$

If meeting insertion loss requirements is an issue, verify that all board layout and PoC guidelines provided by TI are being followed and high quality components are used in the signal transmission and PoC. The insertion loss requirement for a FPD-Link III coax application is given in Table 4-2. For robust operation of the system, the insertion loss must be greater than the values listed over the operating frequency range of the system. Contact TI for more information on the required Channel Specifications defined for each individual FPD-Link device and mode of operation.

**Table 4-2. Insertion Loss Requirement**

| Frequency | PCB Budget (dB) | Total Budget (dB) | Cable Budget (dB) |
|---|---|---|---|
| 1MHz | -0.35 | -1.4 | -0.7 |
| 5MHz | -0.35 | -2.3 | -1.6 |
| 10MHz | -0.35 | -2.5 | -1.8 |
| 50MHz | -0.35 | -3.5 | -2.5 |
| 100MHz | -0.35 | -4.5 | -3.9 |
| 500MHz | -0.35 | -9.5 | -8.7 |
| 1.0GHz | -0.6 | -14.0 | -12.8 |
| 2.1GHz | -1.2 | -21.6 | -19.2 |

## 4.2 PoC Noise Requirements

PoC networks must be designed with the integrity of the high-speed signal in mind. The network cannot interfere with data transmission, and the DC signal must have as little noise as possible. Noise seen on the PoC voltage supply and the deserializer $R_{IN+}$ pin are particularly important and must remain below the recommended conditions. Figure 4-1 shows the measurement nodes of the $V_{PoC}$ and $R_{IN+}$ noise relative to the system.

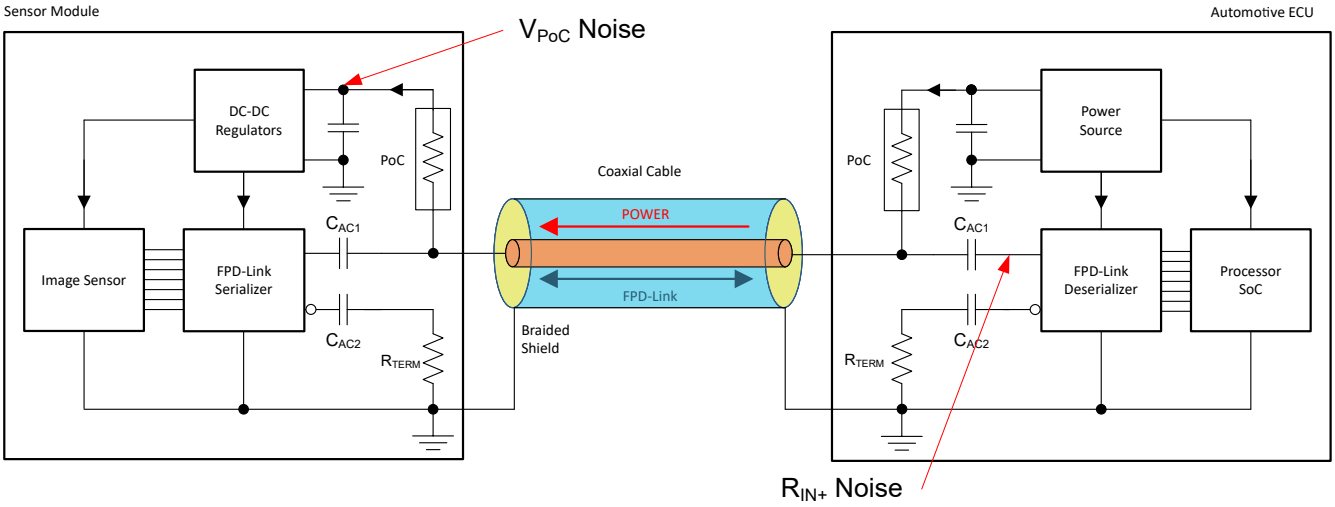


**Figure 4-1. PoC Noise Measurement Nodes**

### 4.2.1 $V_{PoC}$ Noise and Pulse

$V_{PoC}$ noise is the measurement of noise introduced into the system from serializer and sensor operation. Figure 4-2 shows a typical waveform measured from the input of the DC regulators. The supply noise is introduced from the switching of DC buck regulators, and the pulse is due to the switching of the sensor. During periods

of blanking, the current draw from the sensor is significantly lower than during active periods, which causes the voltage to spike.

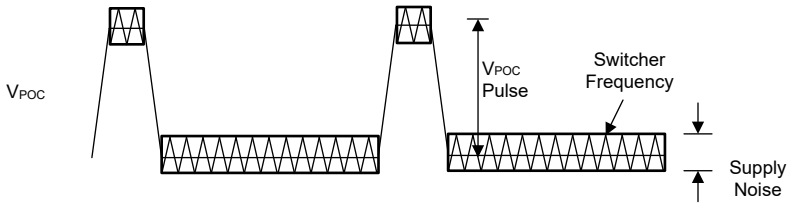


**Figure 4-2. $V_{PoC}$ Noise**

The $V_{PoC}$ must meet the following requirements for proper FPD-Link operation.

- $V_{PoC}$ supply noise must be less than 100mV peak-to-peak
- $V_{PoC}$ pulse must be less than 500mV peak-to-peak (from image sensor blanking and valid periods)
- $V_{PoC}$ pulse slew rate must be greater than 200µs/V

The $V_{PoC}$ of a PoC network can be measured with the following procedure.

1. Connect the serializer to the deserializer through coax
2. Measure the noise floor of the oscilloscope by shorting the probe to ground
3. Power the entire system (sensor, serializer, deserializer, and so on.)
   a. Verify the image sensor is configured to capture video data
4. Set the oscilloscope bandwidth to 0 – 50MHz
5. Probe $V_{PoC}$ at the input of DC regulators on the serializer board
6. Subtract the noise floor measurement from the $V_{PoC}$ noise measurement

### 4.2.2 $R_{IN+}$ Noise

$R_{IN+}$ noise is the noise measured on the deserializer board at the input of the $R_{IN+}$ pin. The $R_{IN+}$ noise must be less than 10 mV peak-to-peak between 0 and 50 MHz to prevent degradation of the FPD-Link signal.

To accurately measure $R_{IN+}$ noise in the system, the image sensor and all other load carrying devices on the serializer side must be actively drawing current. The forward channel and back channel transmissions generated by the connected serializer and deserializer must also be disabled to prevent interference in the noise measurements. To disable the forward channel and back channel transmissions, the PDB pin on the serializer and deserializer devices must be pulled to GND. The image sensor is expected to contribute to the $R_{IN+}$ noise when actively capturing video data. Therefore if the image sensor is not enabled at the time of measurement, the results do not accurately represent the $R_{IN+}$ noise of the system. An example of the RIN+ noise measurement procedure is listed in the following:

1. Rework the serializer and deserializer boards such that the PDB pin on the serializer and deserializer are both pulled to GND for the duration of the measurement
2. Solder wire connections from the I2C bus (SCL, SDA, GND) on the serializer board to an external I2C Controller
3. Connect the serializer and deserializer boards using a coax cable
4. If not determined previously during $V_{PoC}$ measurement, measure the noise floor of the oscilloscope by shorting the probe to ground
5. Power the entire system (sensor, serializer, deserializer, and so on)
6. Configure the image sensor locally through the external I2C controller and confirm that video is being generated
7. Set the oscilloscope bandwidth to 0 – 50MHz
8. Probe $R_{IN+}$ noise at a point close to the deserializer pin using a short probe tip for measuring ground
9. Account for noise floor by subtracting the noise floor measurement from the $R_{IN+}$ noise measurement

### 4.2.3 Causes of PoC Noise

There are various system level factors that impact the noise seen on a PoC network. Some potential sources of PoC noise are listed below.

- Switching regulators – Switching regulators switch the output on and off at a high frequency to step a high voltage DC signal down to a lower voltage. This switching is back fed through the regulator to the input $V_{PoC}$. The switching frequency is typically in the range of kHz and can travel through the PoC network, degrading the signal-to-noise ratio.
- Image sensors – Sensors can introduce noise into the system at the frame rate of the sensor due to the varying power demands. This demand peaks during the gathering of valid frame data and drops during the blanking period. This low frequency noise can more easily travel through the PoC network which is designed to block frequencies in the MHz to GHz range.
- Poor board layout – Not following the guidelines in the data sheet for board layout can lead to signal degradation and extra noise in the system.
- Environmental noise – Environmental noise is from the surroundings and can behave like white noise. This can impose noise at all frequencies across the spectrum.

### 4.2.4 Noise Measurement Best Practices

Proper probing technique is critical to minimize any potential interference or measurement noise when conducting PoC noise measurements. When probing the deserializer board to measure the $R_{IN+}$ noise of the system, probing the RIN+ pin directly on the IC is recommended. Additionally, ground the probe by accessing the ground plane near the pin directly on the PCB board. Grounding close to the pin helps minimize the ground loop and reduces measurement noise. The probe used to collect noise measurements can also impact the results. Select a probe such that the path to ground is as short as possible. For example, ground the probe using a short ground spring rather than an alligator clip or other types of large clips. This minimizes the ground loop and reduces measurement noise. When measuring noise, it is important that the system under test is an accurate representation of the final operational system. The intended cable type and length must be used with the deserializer, serializer, and imager all configured to operate in the intended operational mode.

### 4.2.5 Reducing Effects of PoC Noise

Switching regulators are large contributors to PoC noise. To reduce their effect, TI recommends using low-dropout regulators (LDOs) wherever possible because an LDO does not generate any noise from switching. In the case where an LDO cannot be used and a switching regulator is required, switching noise introduced into the system must be taken into account. To reduce the switching noise, TI recommends using a high PoC voltage. As the PoC voltage rises, current consumption by the switching regulator is reduced, therefore reducing the noise introduced from switching.

Another way to reduce the effect of noise is to use a switching regulator with a higher switching frequency. A higher switching frequency increases the effectiveness of the decoupling capacitors because their impedance is lowered as frequency increases. Figure 5-1 shows decoupling capacitors C1 and C2; with higher switching frequency these capacitors become more effective. Finally, increasing the decoupling capacitance at $V_{PoC}$ can help to better filter any high frequency noise introduced by the regulator. Equation 2 shows the impedance of a capacitor as a function of frequency where Z is the impedance in Ohms, f is the frequency in Hertz, and C is the capacitance in Farads. The capacitance and frequency are in the denominator, which means increasing either value decreases the impedance and therefore shorts high frequencies to ground. When choosing decoupling capacitors, select high quality capacitors rated for the voltage and temperature range required. Some capacitors can significantly degrade when operated near their rated voltage. Sometimes the capacity can drop as low as 20 – 40% of the nominal rating. For this reason, TI recommends selecting capacitors with a voltage rating 2x or 3x the voltage being used to avoid any unexpected drop in capacitance.

# 5 TI Recommended PoC Networks

This section provides multiple TI recommended PoC networks. TI recommends selecting a network based on the desired frequency range, current rating, and temperature. Please note, each of these networks have been tested by TI to meet the channel specification requirements of the PCB budget using a minimal coupon test board. However, due to system dependent factors such as additional traces, touching components, the chosen connector, and general layout techniques, any chosen PoC network must be re-validated to verify that the insertion loss and return loss requirements are still met by the system.

**Table 5-1. Recommended Networks Operating Ratings**

| Vendor | Network | Frequency Range | Current Rating | Temperature Rating |
|---|---|---|---|---|
| N/A | From FPD-Link III data sheet | 25MHz – 2.1GHz | 250mA | 105°C |
| Murata | Network 1 | 5MHz – 5GHz | 800mA | 105°C |
| | Network 2 | 5MHz – 5GHz | 825mA | 105°C |
| | Network 3 | 1MHz – 1GHz | 300mA | 105°C |
| TDK | Network 1 | 5MHz – 4.2GHz | 300mA | 105°C |
| | | | 300mA | 115°C |
| | Network 2 | 5MHz – 4.2GHz | 600mA | 105°C |
| | | | 300mA | 115°C |
| | Network 3 | 5MHz – 4.2GHz | 300mA | 105°C |
| | | | 200mA | 115°C |
| | Network 4 | 5MHz – 4.2GHz | 1000mA | 115°C |
| | Network 5 | 5MHz – 4.2GHz | 600mA | 115°C |
| | Network 6 | 5MHz – 4.2GHz | 600mA | 115°C |
| | Network 7 | 1MHz – 1GHz | 300mA | 105°C |
| | Network 8 | 1MHz – 1GHz | 400mA | 105°C |
| Coilcraft | Network 1 | 1MHz – 5GHz | 300mA | 125°C |
| | Network 2 | 1MHz – 5GHz | 300mA | 125°C |
| | Network 3 | 1MHz – 5GHz | 800mA | 125°C |
| | Network 4 | 1MHz – 5GHz | 1200mA | 125°C |

## 5.1 PoC Network From FPD-Link III Data Sheet

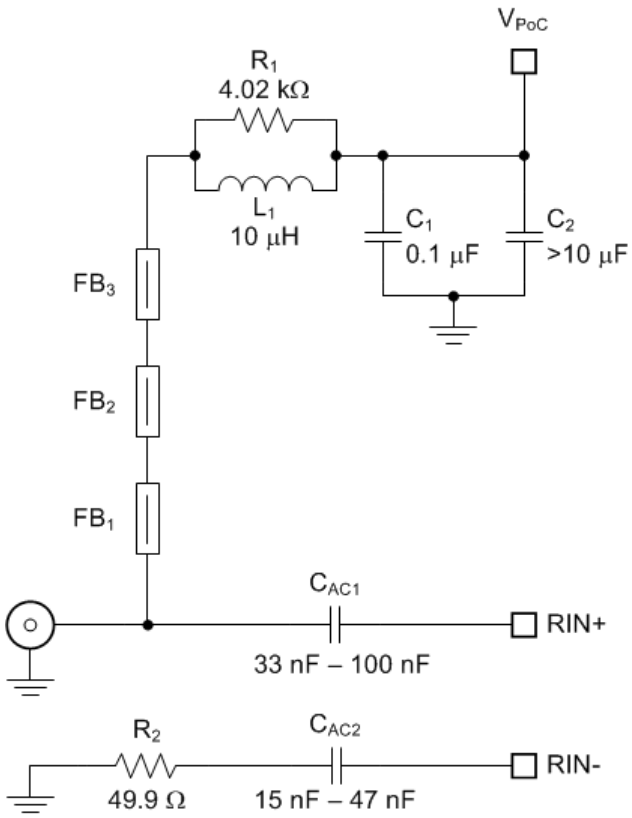


**Figure 5-1. PoC Network from FPD-Link III Data Sheet Schematic**

**Table 5-2. PoC Network from FPD-Link III Data Sheet Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 10µH, 0.288Ω max, 530mA MIN(Isat, Itemp) 30MHz SRF min, 3mm x 3mm, AEC-Q200 | LQH3NPZ100MJR | Murata |
| | Inductor, 10µH, 0.360Ω max, 450mA MIN(Isat, Itemp) 30MHz SRFmin, 3.2mm x 2.5mm, AEC-Q200 | NLCV32T-100K-EFD | TDK |
| | Inductor, 10µH, 0.400Ω typ, 550mA MIN(Isat, Itemp) 39MHz SRF typ, 3mm x 3mm, AEC-Q200 | TYS3010100M-10 | Laird |
| | Inductor, 10µH, 0.325Ω max, 725mA MIN(Isat, Itemp) 41MHz SRF typ, 3mm x 3mm, AEC-Q200 | TYS3015100M-10 | Laird |
| FB1 – FB3 | Ferrite Bead, 1.5kΩ at 1GHz, 0.5Ω max at DC500 mA at 85°C, 0603 SMD, AEC-Q200 | BLM18HE152SZ1 | Murata |
| C1 | 100nF | | |
| C2 | >10µF | | |

## 5.2 Murata Networks

### 5.2.1 Murata Network 1

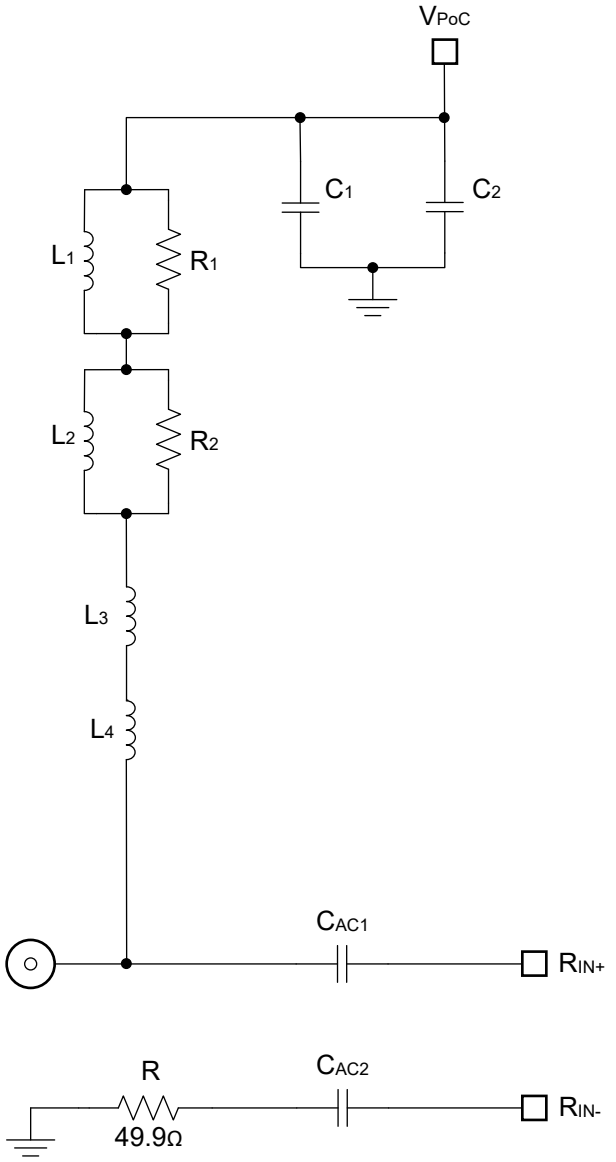


**Figure 5-2. Murata PoC Network 1 Schematic**

**Table 5-3. Murata PoC Network 1 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor,10 µH | LQH3NPH100MME | Murata |
| L2 | Inductor, 3.3µH | LQW32FT3R3 | |
| L3 | Inductor, 120nH | LQW18CNR12 | |
| L4 | | | |
| R1 | 1.5kΩ | | |
| R2 | 3kΩ | | |
| C1 | 100nF | | |
| C2 | >10µF | | |

### 5.2.2 Murata Network 2

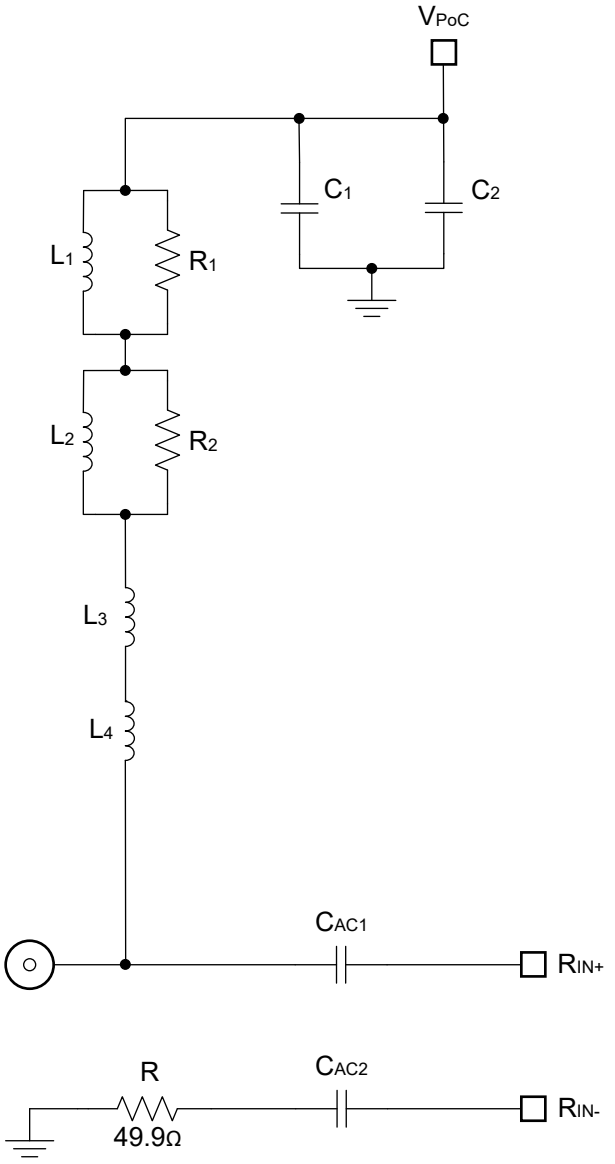


**Figure 5-3. Murata PoC Network 2 Schematic**

**Table 5-4. Murata PoC Network 2 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 6.8µH | LQH3NPH6R8MME | Murata |
| L2 | Inductor, 3.3µH | LQW32FT3R3 | |
| L3 | Inductor, 120nH | LQW18CNR12 | |
| L4 | | | |
| R1 | 1.5kΩ | | |
| R2 | 3kΩ | | |
| C1 | 100nF | | |
| C2 | >10µF | | |

### 5.2.3 Murata Network 3

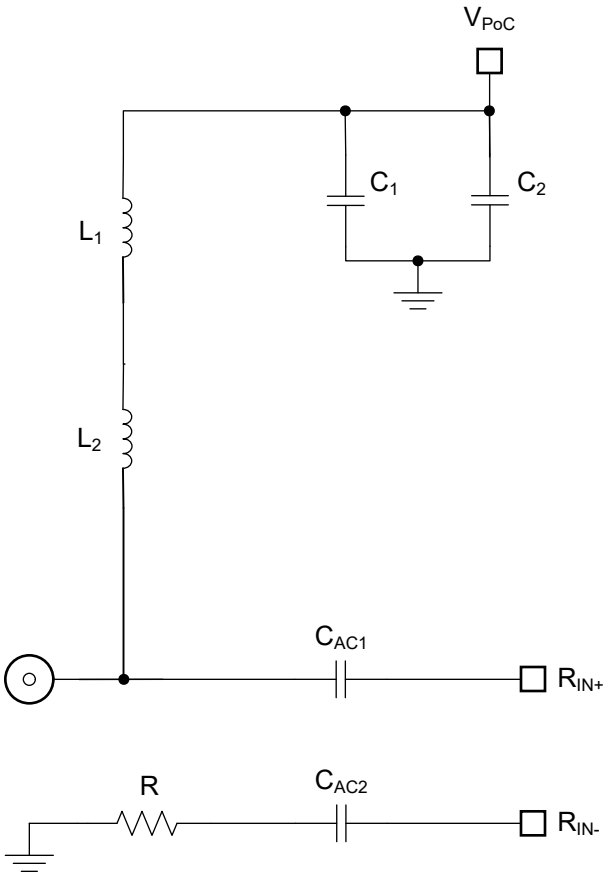


**Figure 5-4. Murata PoC Network 3 Schematic**

**Table 5-5. Murata PoC Network 3 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 47µH | LQW32FT470 | Murata |
| L2 | Inductor, 2µH | LQW21FT2R0 | |
| C1 | 100nF | | |
| C2 | >10µF | | |

## 5.3 TDK Networks

### 5.3.1 TDK Network 1

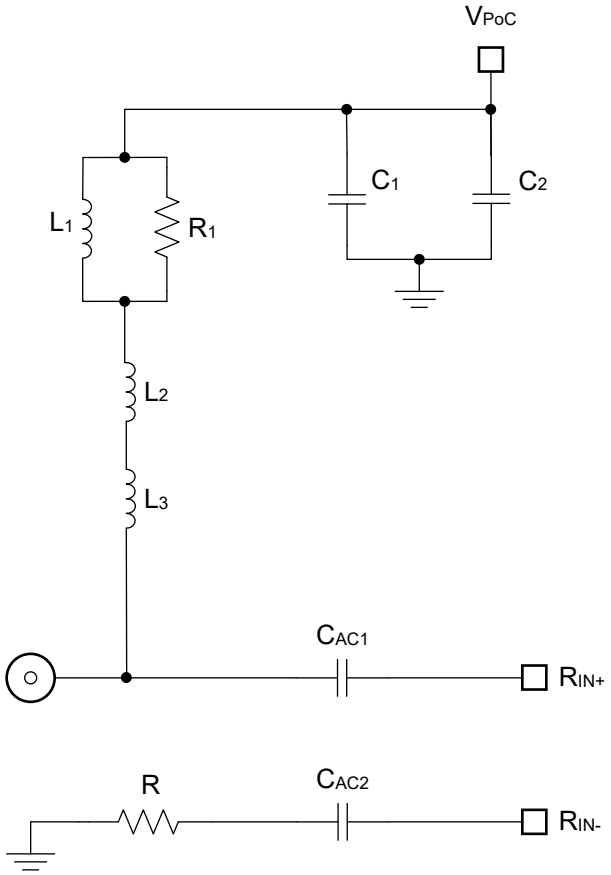


**Figure 5-5. TDK PoC Network 1 Schematic**

**Table 5-6. TDK PoC Network 1 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 10µH | ADL3225VT-100M | TDK |
| L2 | Inductor, 1.5µH | ADL2012-1R5M | |
| L3 | | | |
| R1 | 1.2kΩ | | |
| C1 | 100nF | | |
| C2 | >10µF | | |

### 5.3.2 TDK Network 2

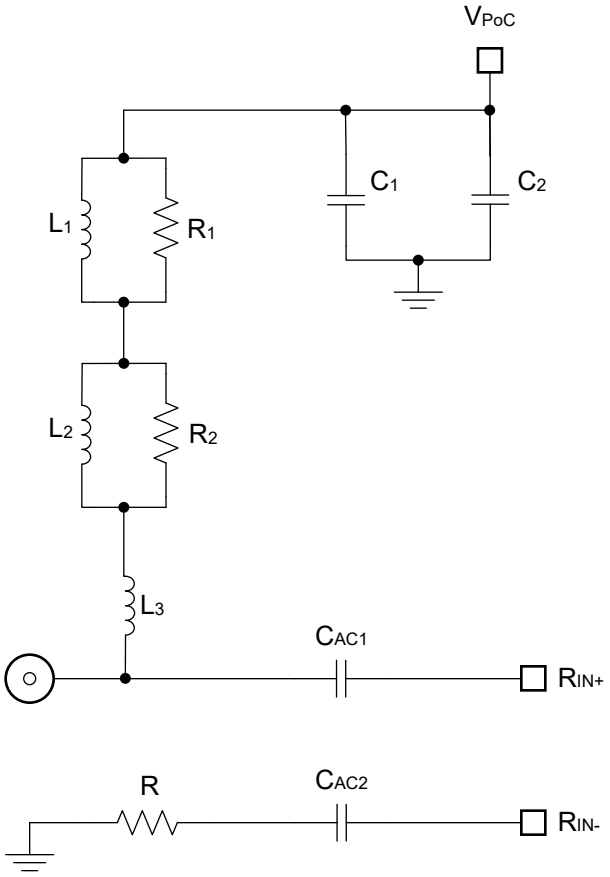


**Figure 5-6. TDK PoC Network 2 Schematic**

**Table 5-7. TDK PoC Network 2 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 10µH | ADM32FSC-100M | TDK |
| L2 | Inductor, 1.5µH | ADL2012-1R5M | |
| L3 | | | |
| R1 | 3kΩ | | |
| R2 | 1.5kΩ | | |
| C1 | 100nF | | |
| C2 | >10µF | | |

### 5.3.3 TDK Network 3

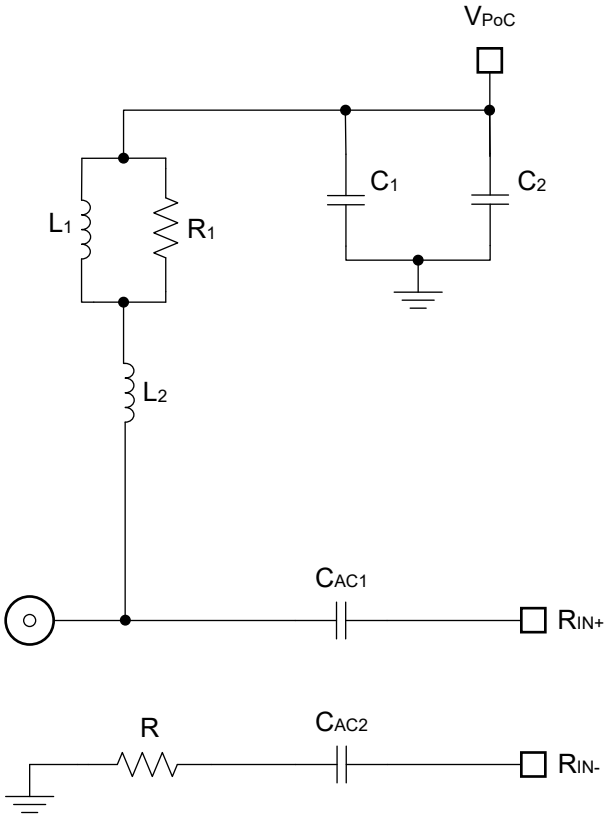


**Figure 5-7. TDK PoC Network 3 Schematic**

**Table 5-8. TDK PoC Network 3 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 10µH | ADL3225VT-100M | TDK |
| L2 | Inductor, 2.2µH | ADL2012-2R2M | |
| R1 | 1.2kΩ | | |
| C1 | 100nF | | |
| C2 | >10µF | | |

### 5.3.4 TDK Network 4

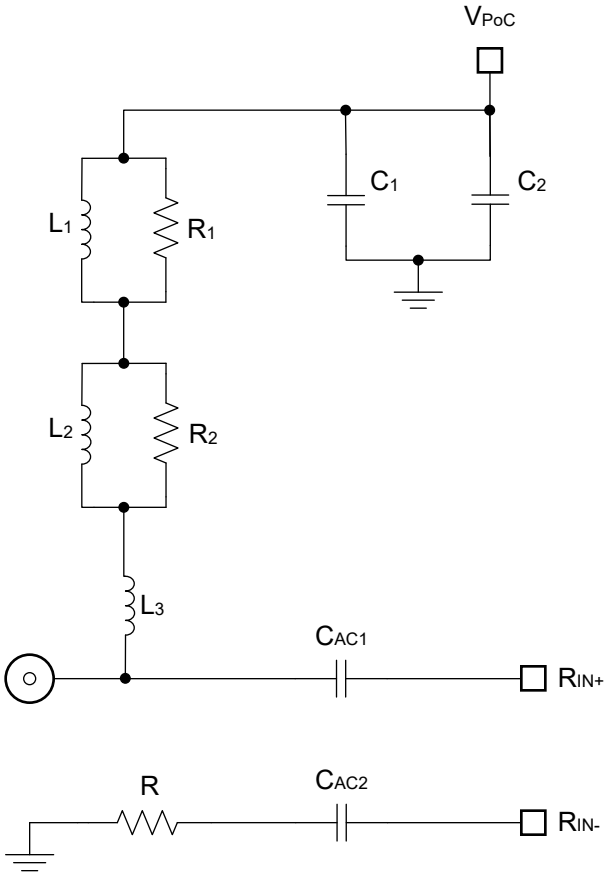


**Figure 5-8. TDK PoC Network 4 Schematic**

**Table 5-9. TDK PoC Network 4 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 10µH | ADM45FDC-100M | TDK |
| L2 | Inductor, 2.2µH | ADL3225VM-2R2M | |
| L3 | | | |
| R1 | 1kΩ | | |
| R2 | | | |
| C1 | 100nF | | |
| C2 | >10µF | | |

### 5.3.5 TDK Network 5

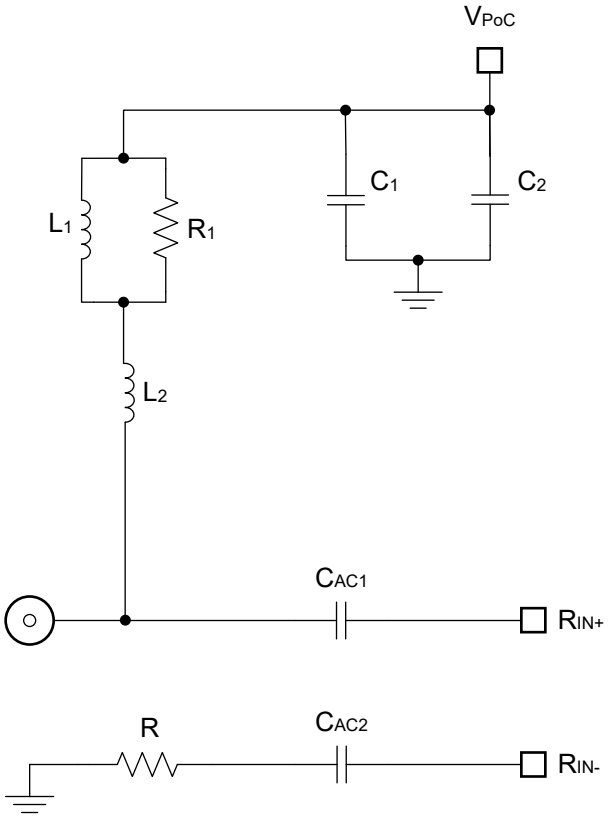


**Figure 5-9. TDK PoC Network 5 Schematic**

**Table 5-10. TDK PoC Network 5 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 10µH | ADM32FSC-100M | TDK |
| L2 | Inductor, 2.2µH | ADL3225VM-2R2M | |
| R1 | 1kΩ | | |
| C1 | 100nF | | |
| C2 | >10µF | | |

### 5.3.6 TDK Network 6

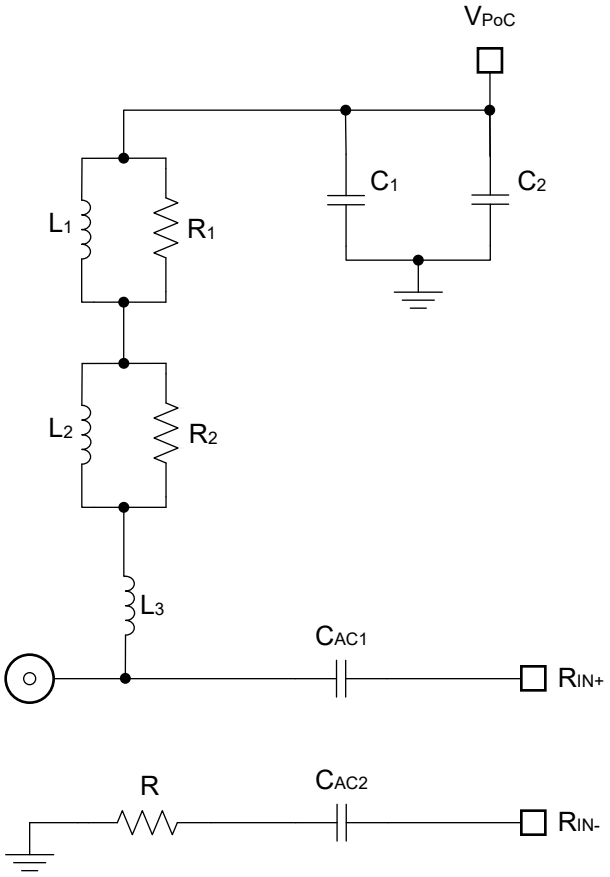


**Figure 5-10. TDK PoC Network 6 Schematic**

**Table 5-11. TDK PoC Network 6 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 10µH | ADM32FSC-100M | TDK |
| L2 | Inductor, 2.2µH | ADL3225VM-2R2M | |
| L3 | | | |
| R1 | 1kΩ | | |
| R2 | | | |
| C1 | 100nF | | |
| C2 | >10µF | | |

### 5.3.7 TDK Network 7

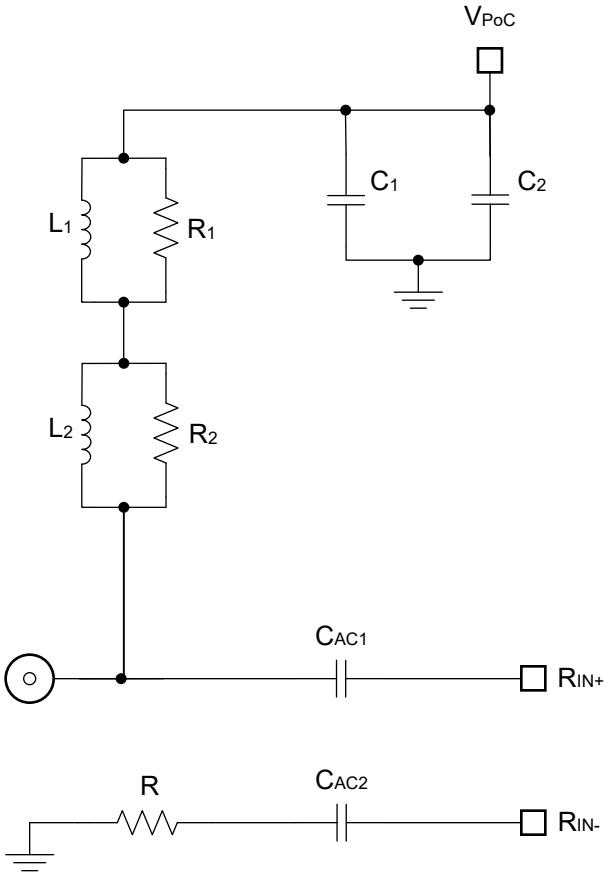


**Figure 5-11. TDK PoC Network 7 Schematic**

**Table 5-12. TDK PoC Network 7 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 47µH | VLS3015CX-470M-H | TDK |
| L2 | Inductor, 2.2µH | ADL2012-2R2M | |
| R1 | 1kΩ | | |
| R2 | 2kΩ | | |
| C1 | 100nF | | |
| C2 | >10µF | | |

### 5.3.8 TDK Network 8

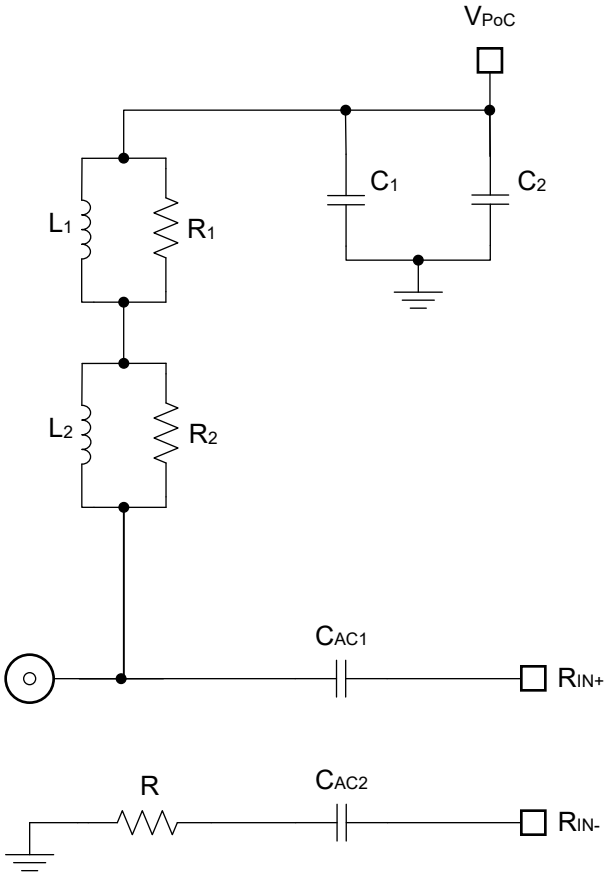


**Figure 5-12. TDK PoC Network 8 Schematic**

**Table 5-13. TDK PoC Network 8 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 100µH | VLS5045EX-101M-H | TDK |
| L2 | Inductor, 2.2µH | ADL2012-2R2M | |
| R1 | 1kΩ | | |
| R2 | 2kΩ | | |
| C1 | 100nF | | |
| C2 | >10µF | | |

## 5.4 Coilcraft Networks

### 5.4.1 Coilcraft Network 1

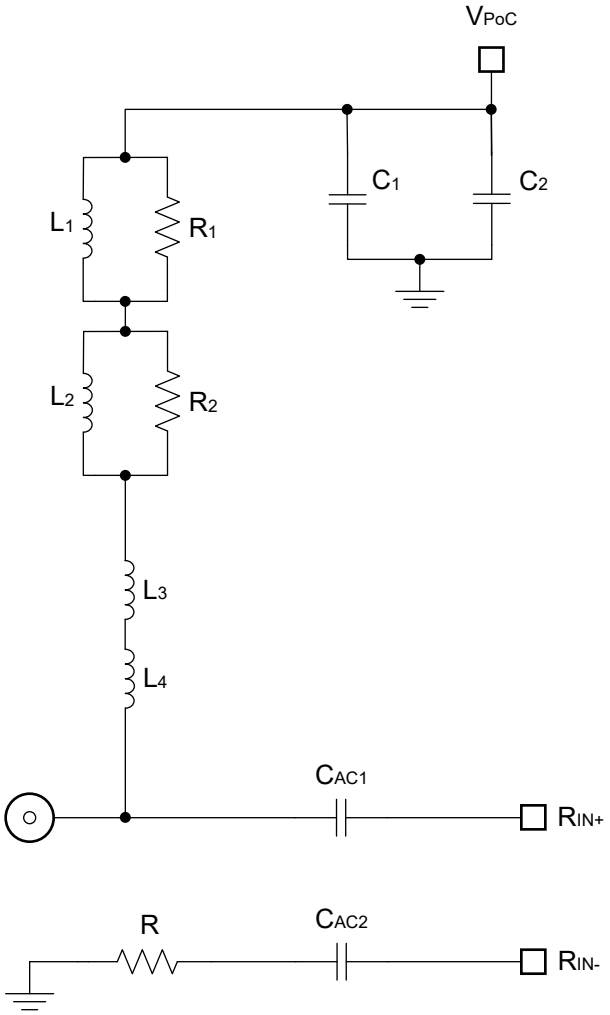


**Figure 5-13. Coilcraft PoC Network 1 Schematic**

**Table 5-14. Coilcraft PoC Network 1 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 100µH | MSS5131H-104 | Coilcraft |
| L2 | Inductor, 6.8µH | 1210POC-682 | |
| L3 | Inductor, 100nH | PFL1005-101 | |
| L4 | | | |
| R1 | 3kΩ | | |
| R2 | 3.6kΩ | | |
| C1 | 100nF | | |
| C2 | >10 µF | | |

### 5.4.2 Coilcraft Network 2

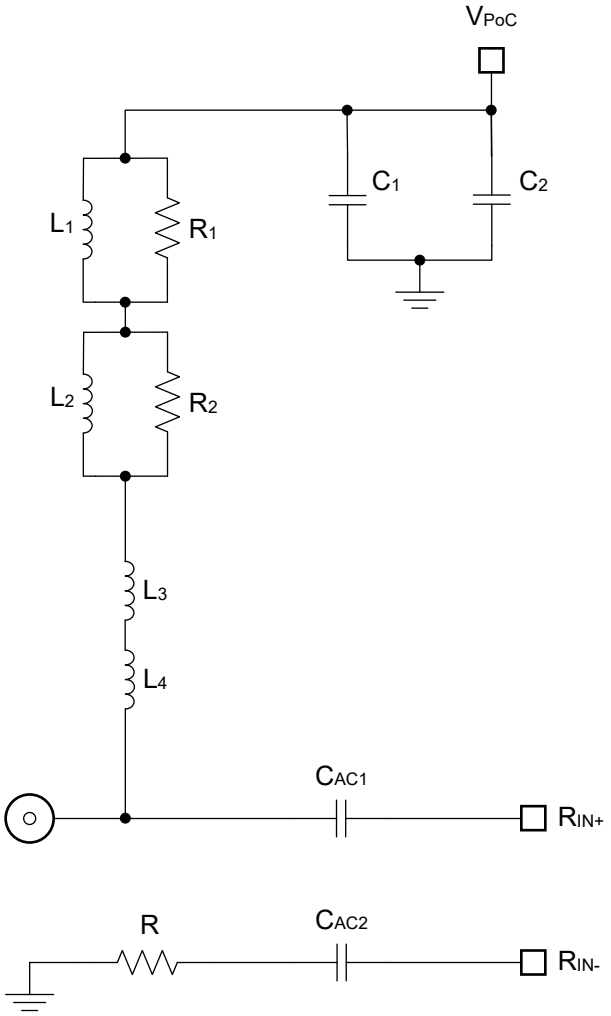


**Figure 5-14. Coilcraft PoC Network 2 Schematic**

**Table 5-15. Coilcraft PoC Network 2 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 100µH | LPS4018-104 | Coilcraft |
| L2 | Inductor, 6.8µH | 1205POC-682 | |
| L3 | Inductor, 180nH | PFL1005-181 | |
| L4 | | | |
| R1 | 2.61kΩ | | |
| R2 | 3.6kΩ | | |
| C1 | 100nF | | |
| C2 | >10µF | | |

### 5.4.3 Coilcraft Network 3

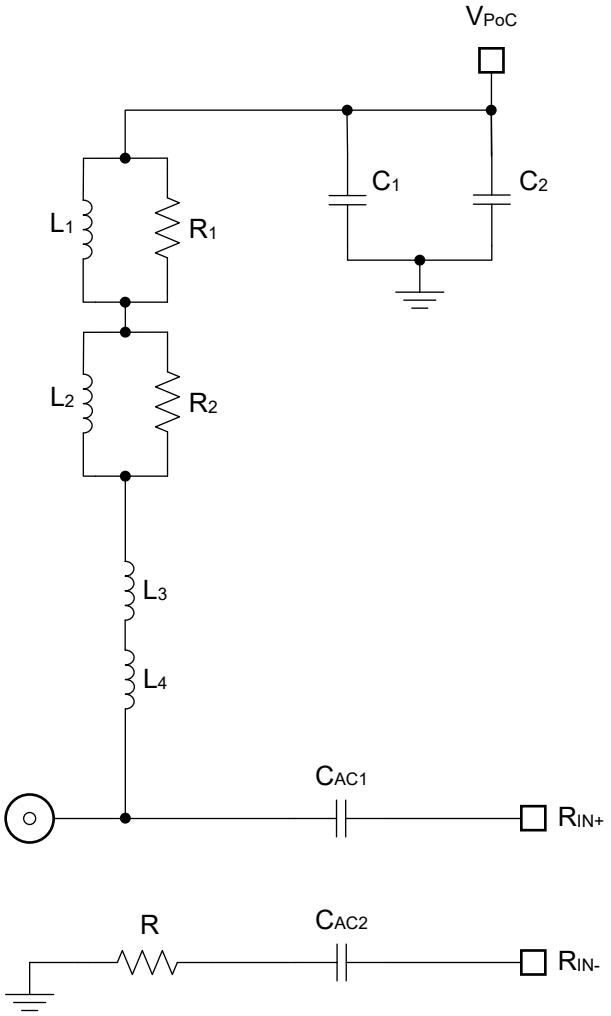


**Figure 5-15. Coilcraft PoC Network 3 Schematic**

**Table 5-16. Coilcraft PoC Network 3 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 100µH | MSS1048T-104 | Coilcraft |
| L2 | Inductor, 10µH | 1812PS-103 | |
| L3 | Inductor, 470nH | PFL2010-471 | |
| L4 | Inductor, 150nH | 0402DF-151 | |
| R1 | 2.55kΩ | | |
| R2 | 3kΩ | | |
| C1 | 100nF | | |
| C2 | >10µF | | |

### 5.4.4 Coilcraft Network 4

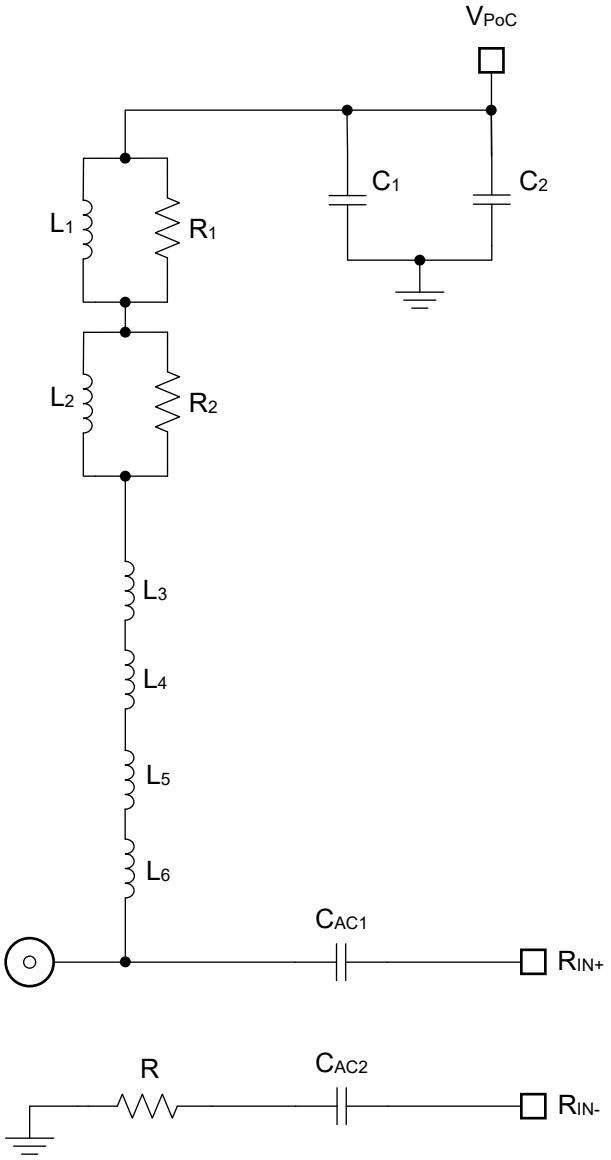


**Figure 5-16. Coilcraft PoC Network 4 Schematic**

**Table 5-17. Coilcraft PoC Network 4 Components**

| Designator | Description | Part Number | Vendor |
|---|---|---|---|
| L1 | Inductor, 100µH | MSS1048T-104 | Coilcraft |
| L2 | Inductor, 22µH | MSS6132T-223 | |
| L3 | Inductor, 5.6µH | 1812PS-562 | |
| L4 | Inductor, 470nH | PFL2010-471 | |
| L5 | Inductor, 20nH | 0402DF-200 | |
| L6 | | | |
| R1 | 3kΩ | | |
| R2 | 2kΩ | | |
| C1 | 100nF | | |
| C2 | >10µF | | |

## 6 Summary

PoC networks can be utilized in ADAS systems to send power from the deserializer board to the serializer board and camera, eliminating the need for a separate power cable. Although PoC networks simplify the overall system architecture, careful consideration must be given to the selected components and network design. Systems that implement a PoC network must be validated to meet TI's channel specifications and noise requirements. Additionally, the PoC network must be designed to properly filter the system's entire FPD-Link operating frequency range, while fulfilling all power consumption requirements of the system and temperature ratings of the individual components. These factors must be considered when selecting a PoC network to implement in an FPD-Link system to provide reliable communication across all operating conditions.

## 7 References


- Texas Instruments, *DS90UB960-Q1 Quad 4.16-Gbps FPD-Link III Deserializer Hub With Dual MIPI CSI-2 Ports*, data sheet.
- Texas Instruments, *DS90UB934-Q1 12 Bit,100-MHz FPD-Link III Deserializer for 1MP/60fps and 2MP/30fps Cameras*, data sheet.
- Texas Instruments, *FPD-Link learning center*.
- Texas Instruments, *Automotive 1-MP Camera Module Reference Design With YUV422, FPD-Link III, and 4-V to 36-V Power Over Coax*, design guide.
- Texas Instruments, *Automotive 2-MP Camera Module Reference Design With MIPI CSI-2 Video Interface, FPD-Link III and POC*, design guide.
- Texas Instruments, *Automotive 2.6-MP Camera Module Reference Design With POL PMIC, FPD-Link III, Supervisor, and POC*, design guide.
- Texas Instruments, *Automotive 8.3-MP POC Camera Module Reference Design with PMIC and FPD-Link III*, design guide.

# 8 Revision History

| Changes from Revision * (June 2014) to Revision A (January 2024) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Updated document to reflect latest PoC recommendations and requirements for all FPD-Link III devices | 2 |
| • Added *capacitor characteristics* section | 5 |
| • Added *ferrite bead characteristics* section | 5 |
| • Added *layout considerations* section | 7 |
| • Added *channel requirements* section | 8 |
| • Added *noise requirements* section | 9 |
| • Added additional recommended PoC network example schematics | 12 |

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