Description

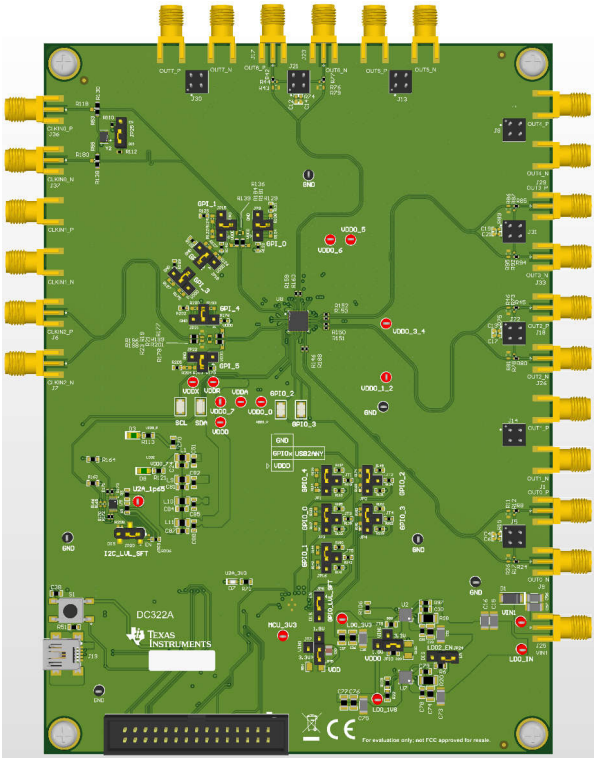
The LMK3H2108 Evaluation Module (LMK3H2108EVM) provides a complete clocking platform to evaluate the clock performance, pin configuration, software configuration, and features of the Texas Instruments LMK3H2108 Clock Generator with integrated BAW-based oscillator. The LMK3H2108 is an eight-output clock generator with an integrated BAW resonator and fractional output dividers, eliminating the need for an external reference clock. The LMK3H2108 accepts up to three input clocks, functioning as a buffer with dividers, or as an I2C clock multiplexer. The EVM includes SMA connectors for all clock outputs for interfacing with 50Ω test equipment. The EVM can be configured through the onboard USB microcontroller (USB2ANY) using a PC with TI's TICS Pro 2 software. TICS Pro 2 can be used to program the LMK3H2108 registers for live configurations. The LMK3H2108 device has a preprogrammed startup configuration that cannot be overwritten.

Features

- PCIe Gen 1 to Gen 7 compliant clock generator
- External and USB power supply options
- Programmability through TICS Pro 2 software graphical user interface (GUI)
- On-board control of device GPIO pins.

Applications

- High performance computing
- Server motherboard
- NIC/SmartNIC
- Hardware accelerator



LMK3H2108 EVM Default Settings

1 Evaluation Module Overview

1.1 Introduction

The EVM can be configured through an on-board USB microcontroller (USB2ANY) interface using a PC with TI's TICS Pro 2 Software GUI. TICS Pro 2 can also be used to import or export register data for flexible programming of the device. Inputs and outputs of the LMK3H2108 can be interfaced with external systems for evaluating compatibility and performance through coaxial cables. On-board LDOs provide an option for using the USB power supply to minimize the amount of external test equipment required.

1.2 Kit Contents

The LMK3H2108EVM box contains:

- One LMK3H2108EVM board (DC322A)
- 3ft mini-USB cable (MPN 3021003-03)

1.3 Specification

Some of the key specifications for the LMK3H2108 device and EVM are noted in the table below.

Table 1-1. LMK3H2108 Key Parameters

PARAMETER	VALUE
Ambient Temperature	-40°C to 105°C
Power Supply	1.8V ± 10%, 2.5V ± 10%, 3.3V ± 10%
Output Operating Frequency	LVCMOS: DC to 200MHz (625Hz to 200MHz from BAW)
	Differential: 2.5MHz to 400MHz
Output Format	LVCMOS, LP-HCSL, LVDS

1.4 Device Information

The LMK3H2108 is a high-performance PCIe compliant clock generator that supports PCIe Gen 1 to Gen 7. The LMK3H2108 can generate any frequency between 2.5MHz and 400MHz differential or any frequency up to 200MHz single-ended. The LMK3H2108 has fail-safe inputs, a flexible power-up sequence, individually controllable outputs through headers or USB2ANY control, and an I2C interface for configuration. The EVM has integrated LDOs for excellent power supply noise suppression with an operating supply voltage of 1.8V, 2.5V, or 3.3V.

2 Hardware

2.1 EVM Quick Start

Table 2-1 describes the default jumper configuration for the EVM to power the device from a USB supply using an on-board LDO. Configure the EVM as specified in the table for initial bring up. The EVM can also be configured to use an external power supply by changing the configuration of jumper JP17 to connect Pin 2 to Pin 3.

Table 2-1. Default Jumper and Switch Configuration

CATEGORY	REFERENCE DESIGNATOR	POSITION	DESCRIPTION
Power	JP24	1-2	On-board 1.8V LDO enabled
	JP5 + JT7	1-2	All VDD_x driven by on-board 3.3V LDO
	JP10 + JT8	1-2	All VDDO_x driven by on-board 3.3V LDO
GPI / Input Clock Pins	JP25	2-3	The on-board LMK6H oscillator is disabled
	JP9	Disconnected	Connects the GPI_0 pin to VDDD or GND
	JP15	Disconnected	Connects the GPI_1 pin to VDDD or GND
	JP18	Disconnected	Connects the GPI_2 pin to VDDD or GND
	JP19	Disconnected	Connects the GPI_3 pin to VDDD or GND
	JP21	Disconnected	Connects the GPI_4 pin to VDDD or GND
	JP22	Disconnected	Connects the GPI_5 pin to VDDD or GND
I^2C Control Pins	JP20	1-2	The I2C level shifter is enabled
GPIO Pins	JP1 + JT1	2-3	The GPIO_4 pin is connected to GND
	JP3 + JT3	2-3	The GPIO_0 pin is connected to GND
	JP16 + JT5	2-3	The GPIO_1 pin is connected to GND
	JP2 + JT2	2-3	The GPIO_2 pin is connected to GND
	JP4 + JT4	2-3	The GPIO_3 pin is connected to GND
	JP6	1-2	The on-board level shifter for the GPIO pins is enabled

2.1.1 Hardware Setup

LMK3H2108 EVM Default Settings shows the default jumper configuration for the EVM. Be sure to set the jumpers as shown for initial power-up using the USB supply.

To begin using the LMK3H2108EVM, follow the steps below.

1. Verify that the jumper configuration matches the default as shown in LMK3H2108 EVM Default Settings and Table 2-1.
2. Connect the USB cable to the USB port, J19.

2.1.2 Software Setup

The TICS Pro 2 software allows for simplification of programming device registers. The TICS Pro 2 software is used to:

- View the live device settings
- View the settings programmed on the four OTP pages
- Control the on-board GPIO pins and device registers for automated testing

2.2 EVM Configuration

The LMK3H2108EVM can be configured for multiple modes using the on-board USB2ANY and either USB power or external supply power. The following sections describe the power, logic, clock input, and clock output interfaces on the EVM, as well as setup and configuration of these modes.

2.2.1 Device Operational Modes

The LMK3H2108 can be configured to start up on one of four OTP pages when any combination of GPIO_0, GPIO_1, and GPIO_2 are configured as OTP Page Selection (OTP_SEL) pins on each page. If no GPIO are configured as OTP_SEL pins, the device loads the default OTP page selected in the configuration, most commonly OTP Page 0. On each OTP page, the I^2C interface is available.

The default configuration when using an LMK3H2108A00 device is eight 100MHz 100Ω LP-HCSL outputs. OTP Page 0 has no spread spectrum clocking (SSC) enabled, and each other OTP page uses spread spectrum:

- Page 0: No SSC
- Page 1: -0.1% downspread SSC
- Page 2: -0.3% down-spread SSC
- Page 3: -0.5% down-spread SSC

An LMK6H device is present on the board for optionally driving IN0 from a PCIe-compatible reference in buffer mode..

2.2.2 Power Supply

The LMK3H2108 has multiple VDD and VDDO pins that operate from 1.8V ± 10% to 3.3V ± 10%. For both 1.8V and 3.3V operation, the on-board LDOs can be used to control the supply voltage. Alternatively, external power can be supplied through the VIN1 SMA connector. Table 2-2 describes the multiple power supply configurations.

Table 2-2. EVM Power Modes

DESIGNATOR	DEFAULT POSITION	DESCRIPTION
JP24	1-2	1-2: Enable 1.8V LDO 2-3: Disable 1.8V LDO
JP10 + JT8	1-2	1-2: All VDDO_x sourced from 3.3V LDO 2-3: All VDDO_x sourced from 1.8V LDO 2-JT8: All VDDO_x sourced from VIN1
JP15+ JT7	1-2	1-2: All VDD_x sourced from 3.3V LDO 2-3: All VDD_x sourced from 1.8V LDO 2-JT7: All VDD_x sourced from VIN1

2.2.3 Logic Inputs and Outputs

The General Purpose Input (GPI) and General Purpose Input and Output (GPIO) pins on the LMK3H2108 provide options for selecting different device modes, output enable or disable control, Loss of Signal (LOS) detection, and I^2C device address selection. Table 2-3 describes the possible behaviors of each GPI and GPIO pin.

Table 2-3. GPI/GPIO Behaviors

PIN NAME	GLOBAL OE FUNCTION	OE_GROUP FUNCTION	INPUT CLOCK FUNCTION	STATUS OUTPUT FUNCTION	I2C ADDRESS FUNCTION	OTP PAGE SELECTION	POWERDOWN FUNCTION
GPI_0	Yes	Yes	IN0_P	N/A	Yes	No	N/A
GPI_1	Yes	Yes	IN0_N	N/A	Yes	No	N/A
GPI_2	Yes	Yes	IN1_P	N/A	Yes	No	Yes
GPI_3	Yes	Yes	IN1_N	N/A	Yes	No	Yes

Table 2-3. GPI/GPIO Behaviors (continued)

PIN NAME	GLOBAL OE FUNCTION	OE_GROUP FUNCTION	INPUT CLOCK FUNCTION	STATUS OUTPUT FUNCTION	I2C ADDRESS FUNCTION	OTP PAGE SELECTION	POWERDOWN FUNCTION
GPI_4	Yes	Yes	IN2_P	N/A	Yes	No	Yes
GPI_5	Yes	Yes	IN2_N	N/A	Yes	No	Yes
GPIO_0	Yes	Yes	No	Yes	Yes	Yes	Yes
GPIO_1	Yes	Yes	No	Yes	Yes	Yes	Yes
GPIO_2	Yes	Yes	No	Yes	Yes	Yes	Yes
GPIO_3	Yes	Yes	No	Yes	Yes	No	Yes
GPIO_4	Yes	Yes	No	Yes	Yes	No	Yes

All GPI and GPIO pins have weak internal pullup and pulldown resistors that can be configured in TICS Pro. The voltage that is seen by each GPIO pin can be controlled by either jumpers or the USB2ANY interface. The voltage on the GPI pins can only be controlled through jumpers.

PIN NAME	REFERENCE DESIGNATOR	POSITION	DESCRIPTION
GPI_0 (1)	JP9	1-2	1-2: Pulled to VDDD 2-3: Pulled to GND
GPI_1 (2)	JP15	1-2	1-2: Pulled to VDDD 2-3: Pulled to GND
GPI_2 (3)	JP18	1-2	1-2: Pulled to VDDD 2-3: Pulled to GND
GPI_3 (4)	JP19	1-2	1-2: Pulled to VDDD 2-3: Pulled to GND
GPI_4 (5)	JP21	1-2	1-2: Pulled to VDDD 2-3: Pulled to GND
GPI_5 (6)	JP22	1-2	1-2: Pulled to VDDD 2-3: Pulled to GND
GPIO_0	JP3 + JT3	2-JT3	1-2: Pulled to VDDD 2-3: Pulled to GND 2-JT3: Controlled by TICS Pro 2
GPIO_1	JP16 + JT5	2-JT5	1-2: Pulled to VDDD 2-3: Pulled to GND 2-JT6: Controlled by TICS Pro 2
GPIO_2	JP2 + JT2	2-JT2	1-2: Pulled to VDDD 2-3: Pulled to GND 2-JT2: Controlled by TICS Pro 2
GPIO_3	JP4 + JT4	2-JT4	1-2: Pulled to VDDD 2-3: Pulled to GND 2-JT4: Controlled by TICS Pro 2
GPIO_4	JP1 + JT1	2-JT1	1-2: Pulled to VDDD 2-3: Pulled to GND 2-JT1: Controlled by TICS Pro 2
PWRGD/PWRDN	JP26 + JT6	2-JT6	1-2: Pulled to VDDD 2-3: Pulled to GND 2-JT6: Controlled by TICS Pro 2

(1) The GPI pins are configured as clock input pins by default. For using GPI_0, move the R181 resistor to the R129 footprint.
(2) The GPI pins are configured as clock input pins by default. For using GPI_1, move the R184 resistor to the R139 footprint.
(3) The GPI pins are configured as clock input pins by default. For using GPI_2, move the R195 resistor to the R155 footprint.
(4) The GPI pins are configured as clock input pins by default. For using GPI_3, move the R197 resistor to the R167 footprint.
(5) The GPI pins are configured as clock input pins by default. For using GPI_4, move the R199 resistor to the R177 footprint.

(6) The GPI pins are configured as clock input pins by default. For using GPI_5, move the R201 resistor to the R178 footprint.

2.2.4 Configuring the Clock Outputs

The clock output pairs of the LMK3H2108 are routed via 50Ω single-ended traces to SMA ports (OUT[7:0]_P/OUT[7:0]_N). These outputs have series resistor (0Ω populated) options. The default output configuration for the LMK3H2108EVM is DC-coupled LP-HCSL for all outputs.. Each of these outputs can be configured for AC-LVDS, DC-LVDS, LP-HCSL, and LVCMOS output formats.

For 1.2V LVCMOS outputs, the logic high level is set by setting the OUTx_CMOS_1P2V_EN bit of the output channel to a '1'. When this bit is a 0, the logic high level of LVCMOS outputs is determined by the voltage on the VDDO supply for the output.

2.2.5 Using the USB Interface Connection

The on-board MSP430F5529 USB microcontroller (U6) provides an I2C host interface to the LMK3H2108 peripheral device. The device registers can be controlled with the USB using the TICS Pro 2 software running on a host PC. J20 can be used with an external USB2ANY as an alternative to using the on-board USB2ANY.

If the USB2ANY firmware needs to be updated, the S1 button serves as the BSL connection. Press the S1 button to mimic pressing the BSL button of an external USB2ANY. Release the button after updating the firmware.

3 Software

3.1 Software Installation

The TICS Pro 2 software allows for simplification of programming device registers. The TICS Pro 2 software is available at the TICSPRO2-GUI site. Note that the TICS Pro version 1.x software available on TI.com is **not** compatible with the LMK3H2108EVM.

3.2 Software Description

3.2.1 User Controls Page

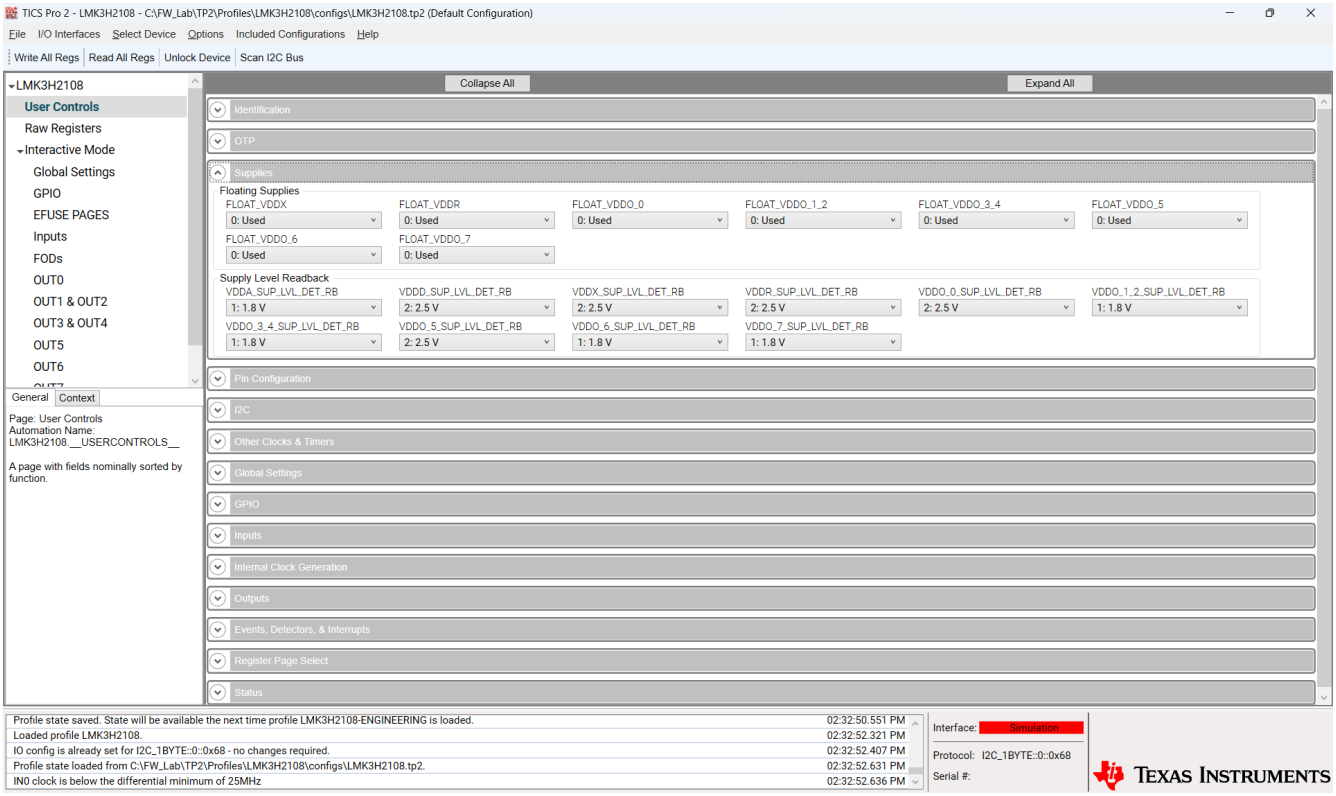


Figure 3-1. LMK3H2108 User Controls Page

The *User Controls* page contains each of the fields that are present in the GUI. Each field on the page is grouped by the respective device block.

3.2.2 Raw Registers Page

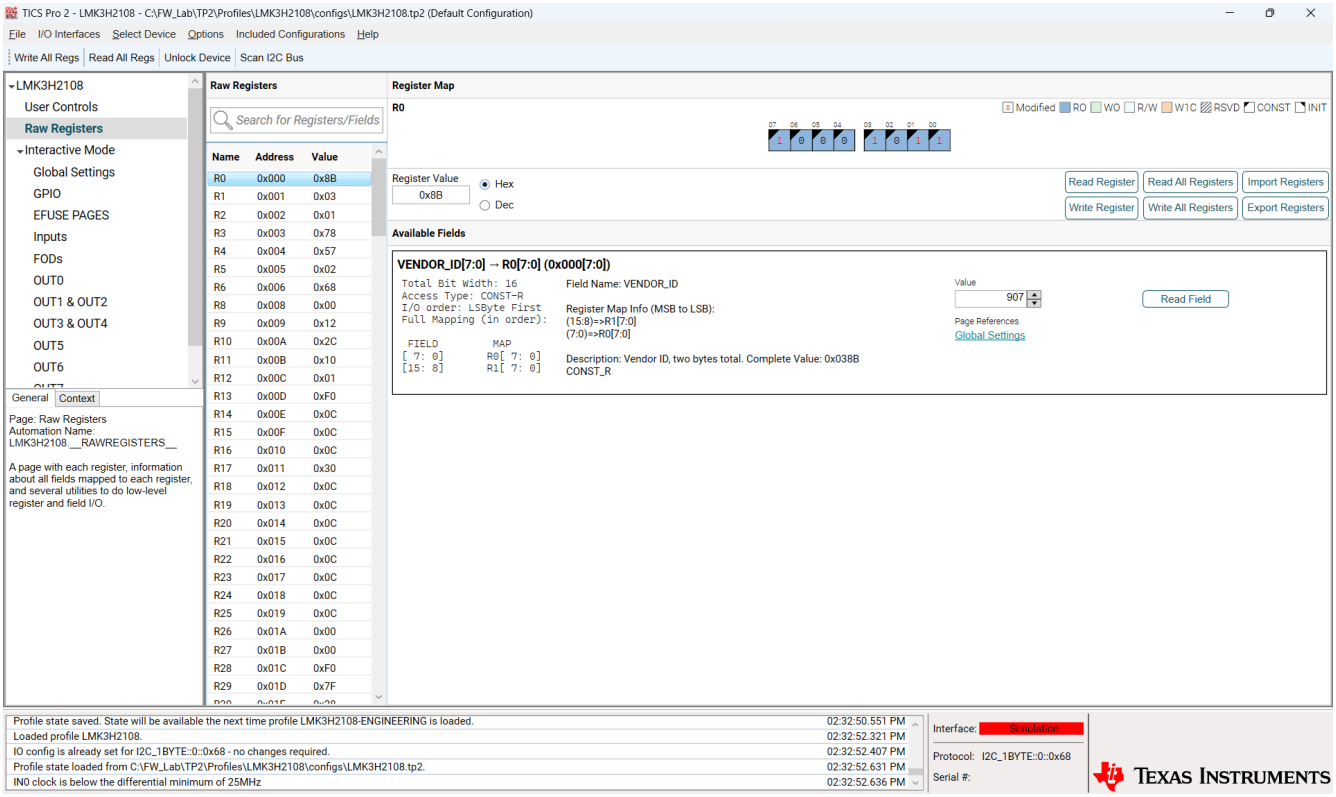


Figure 3-2. LMK3H2108 Raw Registers Page

The *Raw Registers* page organizes each of the device fields by the register. This page contains a search bar, which allows for searching for a field by name, or searching for a register by register number. Each bit in a register is marked with the accessibility type: Read Only, Write Only, Read & Write, Write 1 to Clear, Reserved, Constant, or Initialization. When a bit is changed, the text color changes to red until the field is read or written.

3.2.3 Global Settings Page

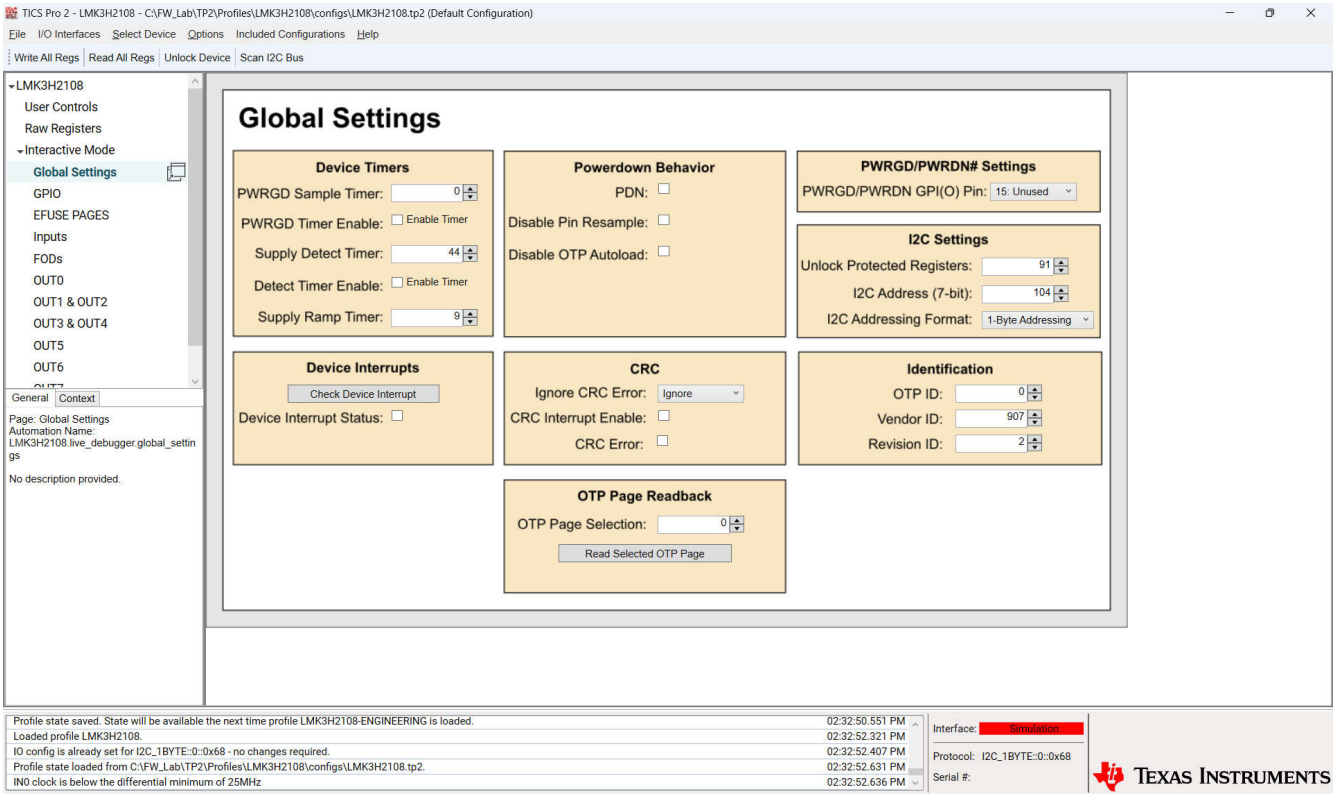


Figure 3-3. Global Settings Page

The *Global Settings* page contains an assortment of device settings for:

- Control of the device timers
- Powerdown behavior
- PWRGD/PWRDN# pin selection
- Device interrupt configuration
- EFUSE CRC behavior
- Device identification
- Readback from any OTP page to the live registers and the EFUSE Pages GUI page

3.2.4 EFUSE Pages Page

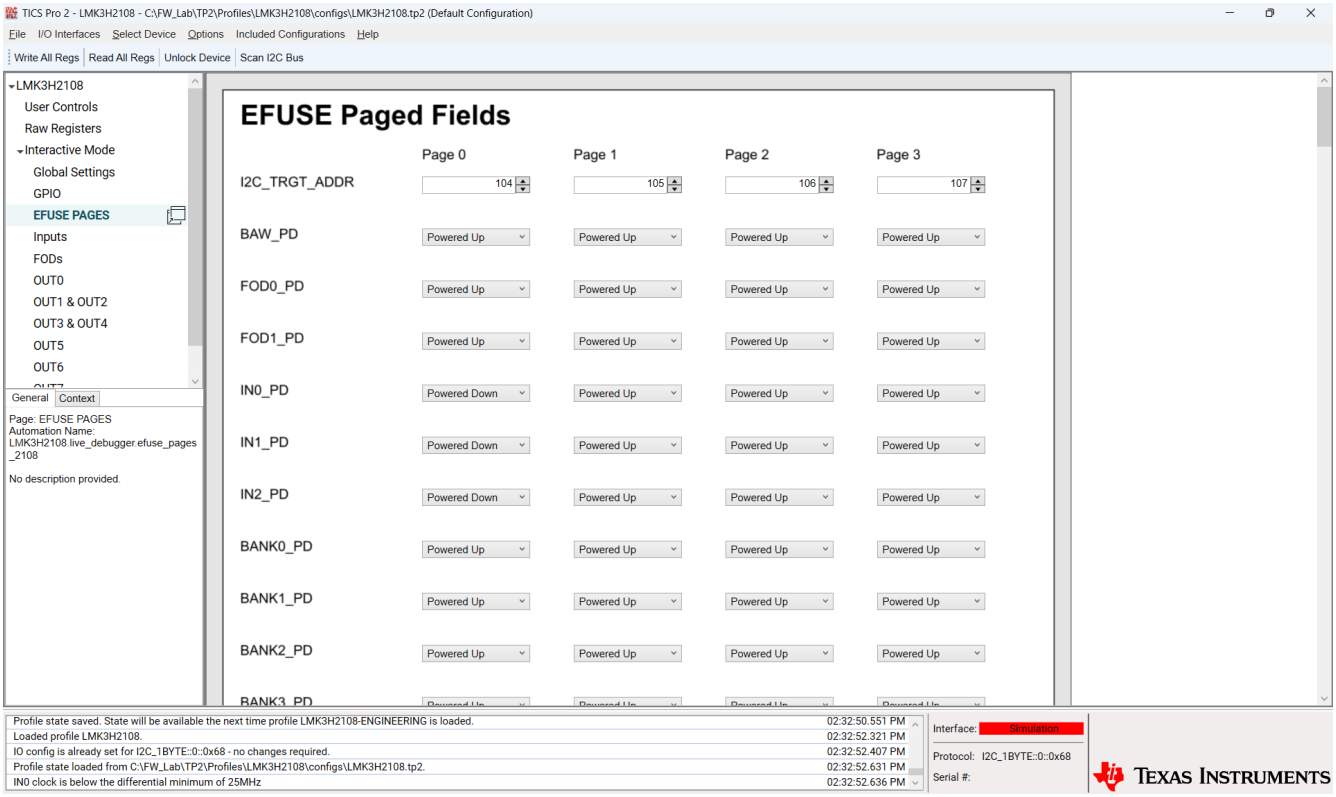


Figure 3-4. EFUSE Pages Page

The *EFUSE Pages* page allows for viewing the contents of the device EFUSE. To read the EFUSE contents of a particular device, click the button "Read Selected OTP Page" on the *Global Settings* page. This information is stored in the .tp2 file along with the rest of the GUI information. For requesting a new OTP configuration, please send a request with the .tp2 file to TI.

3.2.5 GPIO Page

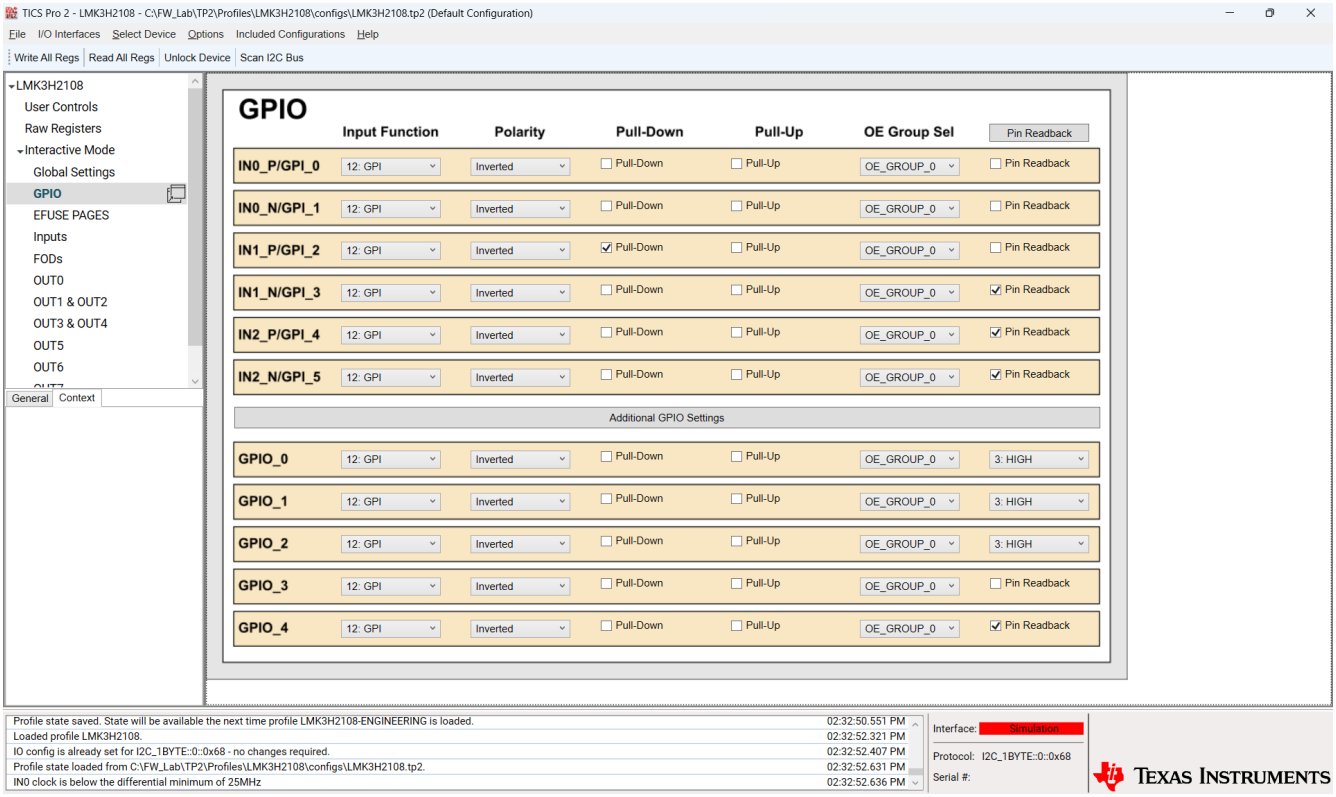


Figure 3-5. LMK3H2108 GPIO Page

The *GPIO* page contains the settings for configuring the GPI and GPIO pins of the LMK3H2108. Each GPI pin can have the input functionality disabled if not used. Each GPIO pin can have the input and output functionality disabled if not used. Each GPI and GPIO pin has pulldown and pullup resistors that can be individually enabled or disabled. Readback of the pin state is available for each GPI and GPIO pin.

GPIO pins, when configured as a status output, can provide a loss of signal status for each of the input clocks, or a clock ready signal when the device is ready to provide output clocks.

3.2.6 FODs Page

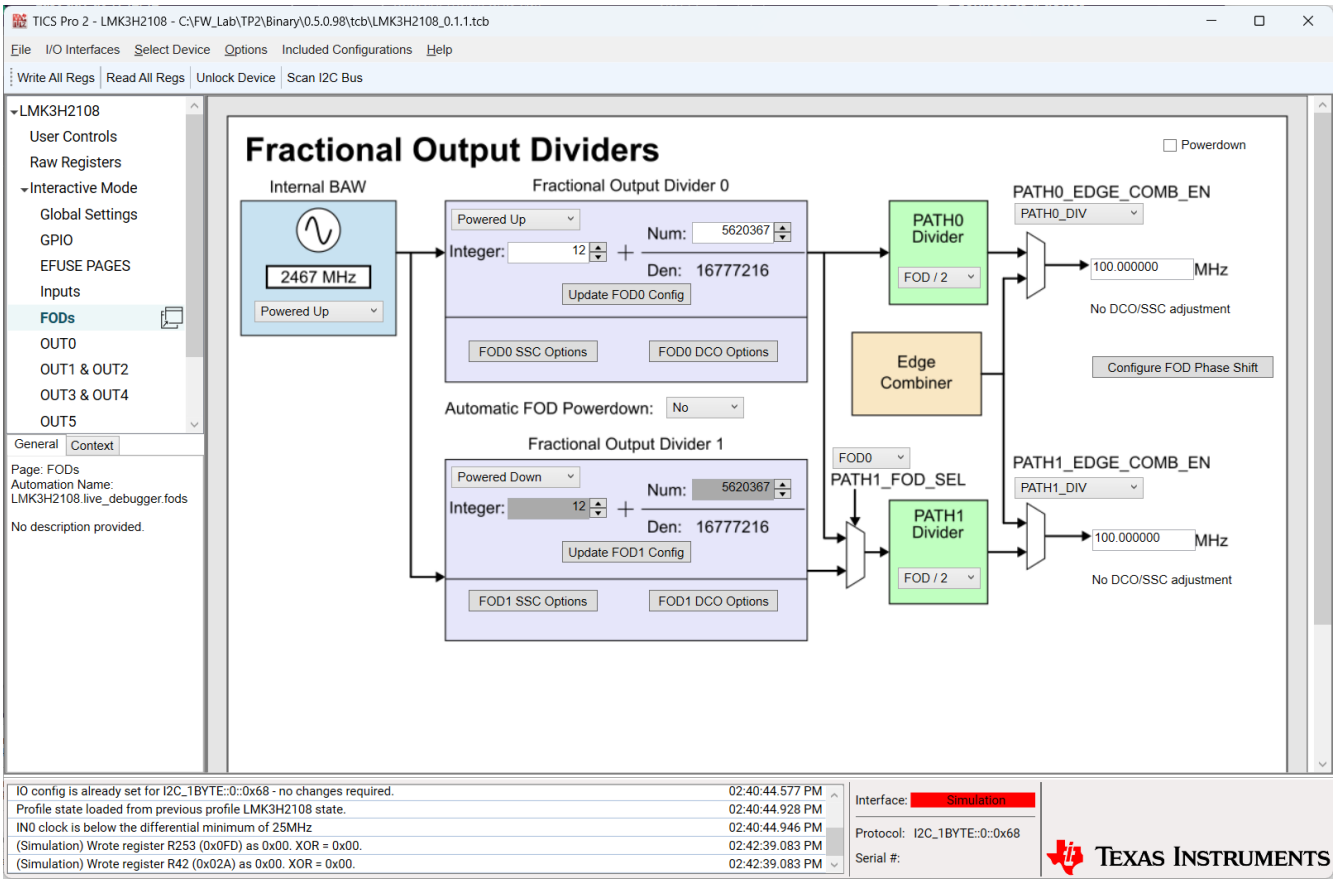


Figure 3-6. LMK3H2108 FODs Page

The *FODs* page allows for setting the FOD0 and FOD1 divider values. Each FOD has a path post-divider, allowing for the generation of frequencies between 2.5MHz and 200MHz after the post-divider. If the edge combiner is selected in place of the FOD post-divider, then frequencies between 200MHz and 400MHz can be generated. When either path selects the edge combiner, then the FOD1 divider values are ignored by the LMK3H2108, and both FODs use the FOD0 divider values.

The text-box to the right of each FOD post-divider allows for automatic calculation of the FOD divider values. Users have the option to select from each possible combination of FOD frequency and post-divider value for frequency generation. If the frequency cannot be generated, the box turns red, and an error message appears in the status bar. If the frequency requires usage of the edge combiner, then both frequency boxes are updated accordingly without the selection pop-up. If the FOD divider selection for the PATH1 frequency results in the same values as the FOD0 divider values, then FOD0 is automatically selected as the source for PATH1.

FOD and FOD1 both provide the option for Spread Spectrum Clocking (SSC). Four preconfigured SSC options are available, in addition to custom SSC options. The preconfigured SSC options are optimized for an FOD frequency of 200MHz. The custom SSC can be used with any FOD frequency. The GUI automatically calculates the values for the SSC_STEPS and SSC_STEP_SIZE fields when a value is entered for the SSC depth. Changing the modulation type between down-spread and center-spread also recalculates these values.

Both FODs support digitally-controlled oscillator (DCO) mode for adjusting the FOD frequency in terms of PPM adjustment. Once a PPM step is entered, the Up and Down buttons for each FOD increment or decrement the total PPM shift. If the edge combiner is used, then SSC and DCO must not be used.

3.2.7 Inputs Page

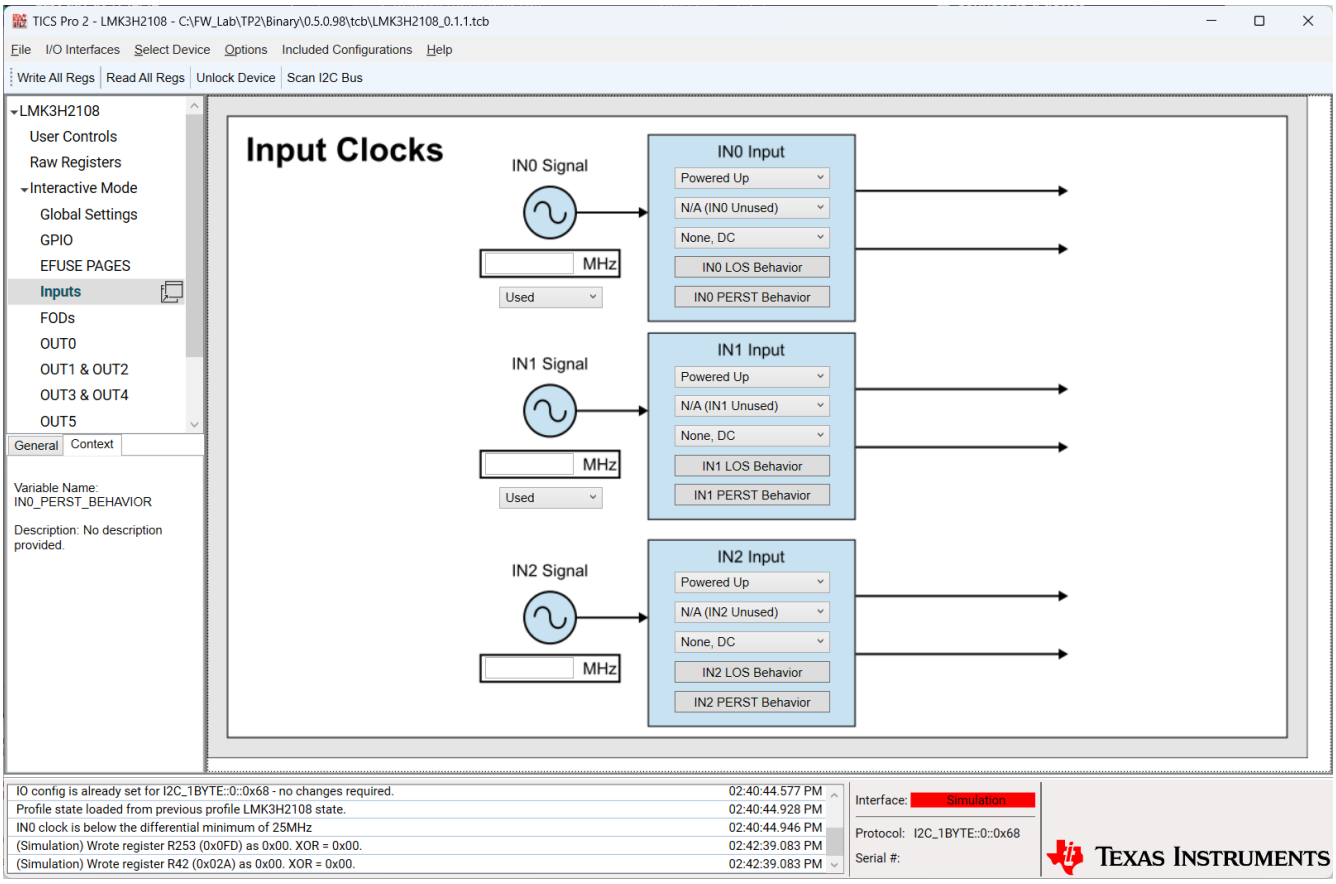


Figure 3-7. LMK3H2108 Inputs Page

The *Inputs* page allows for modification of the LMK3H2108 input buffers. Each input consists of the following fields:

- Input frequency: Used solely for calculation purposes on the output pages
- Power state: Whether the input path is enabled or disabled
- Input format: Disabled, INx_P LVCMOS, INx_N LVCMOS, or INx Differential
- Input termination, capable of supporting any input format
- Loss of signal behavior
- PCIe Reset (PERST) mode behavior

3.2.8 OUT0 Page

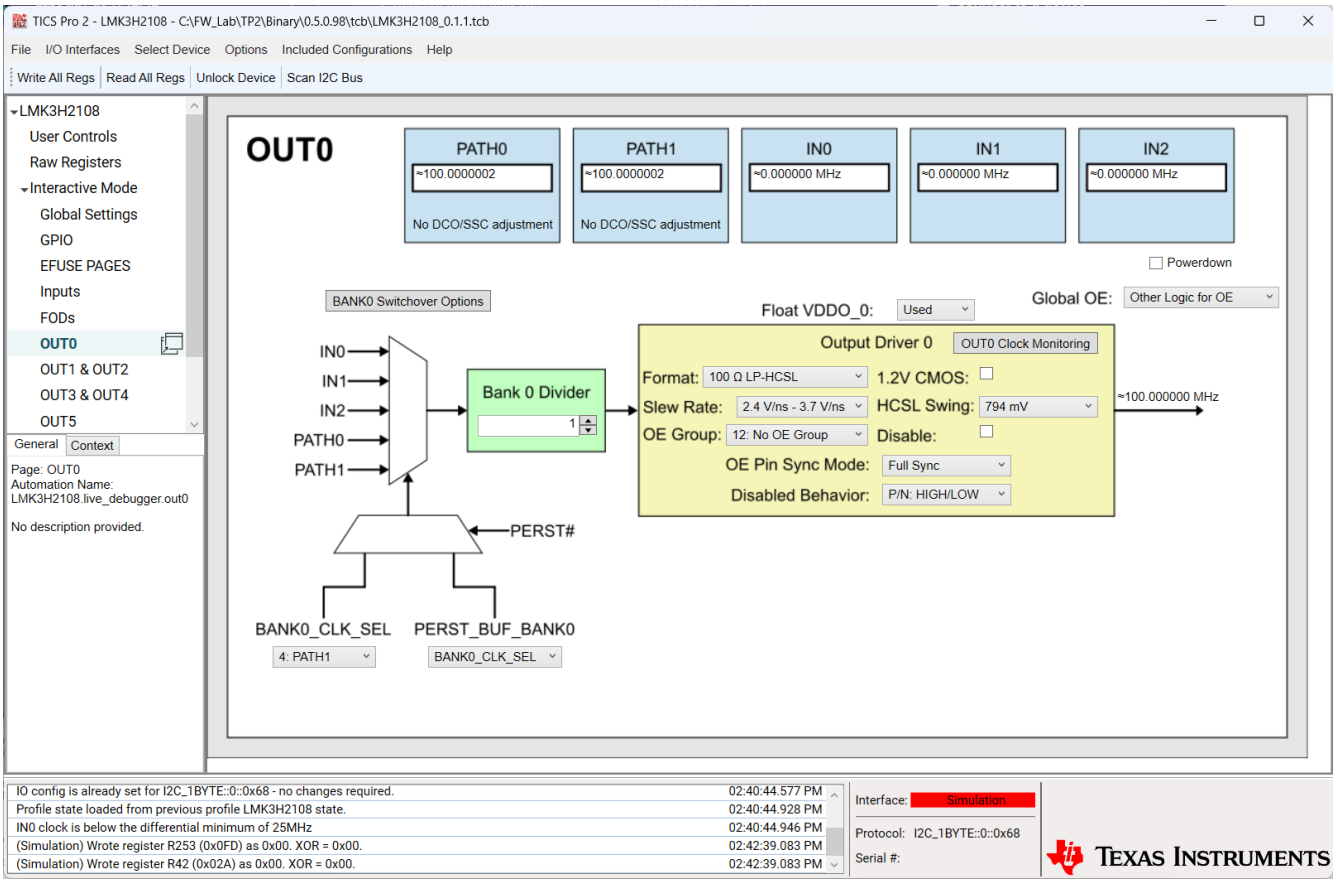


Figure 3-8. OUT0 Page

The *OUT0* page allows for configuration of OUT0. The GUI pages for OUT5, OUT6, and OUT7 function similarly to this page. This page allows for the configuration of the following options for OUT0:

- Bank clock selection
- PCIe Reset (PERST) mode behavior
- Bank divider: For OUT0 this allows for a maximum divide value of 65536 when selecting a divider value of 0, for all other outputs the maximum divider value is 16.
- Output format
- Slew rate
- Output enable group
- 1.2V LVCMOS enable: When 1.2V LVCMOS is enabled, and the output format field selects an LVCMOS output type, the output is LVCMOS with a swing of 1.2V. Otherwise, the output format field selects the output format.
- LP-HCSL swing
- Output disable
- Output enable pin synchronization mode
- Output disable behavior

3.2.9 OUT1 & OUT2 Page

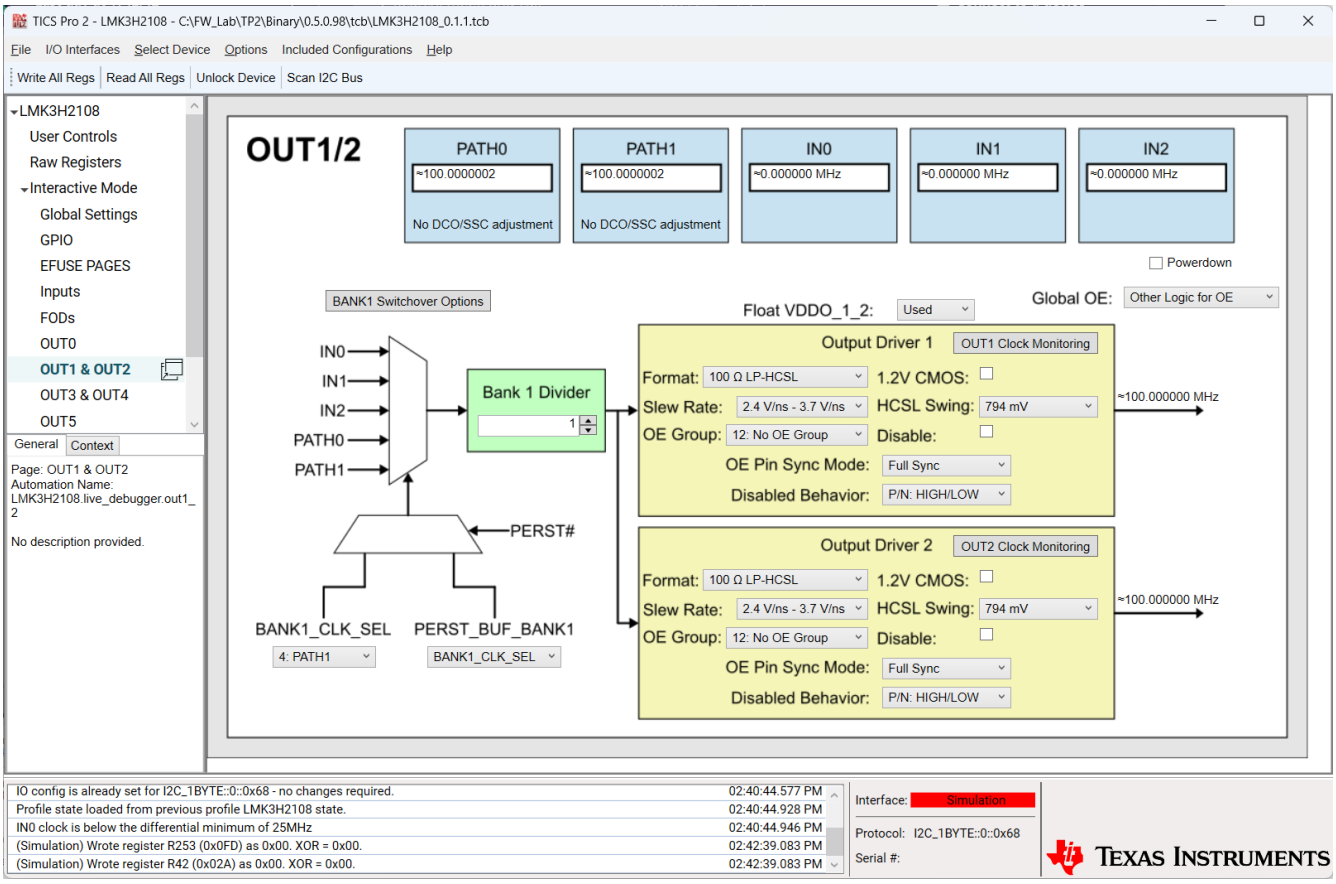


Figure 3-9. LMK3H2108 OUT1/2 Page

The *OUT1/2* page allows for configuring both OUT1 and OUT2, as these outputs are on the same bank. Outputs that are on the same bank share the same clock source, supply voltage source, and divider value. All other fields are independently controllable for both outputs. OUT3 and OUT4 share a similar structure, as these outputs also share a bank.

4 Implementation Results

4.1 Evaluation Setup

For test measurements, the evaluation module is configured in one of two modes:

1. Operation from the onboard LDOs in BAW + FOD mode
2. Operation from the onboard LDOs in input buffer mode

4.2 Performance Data and Results

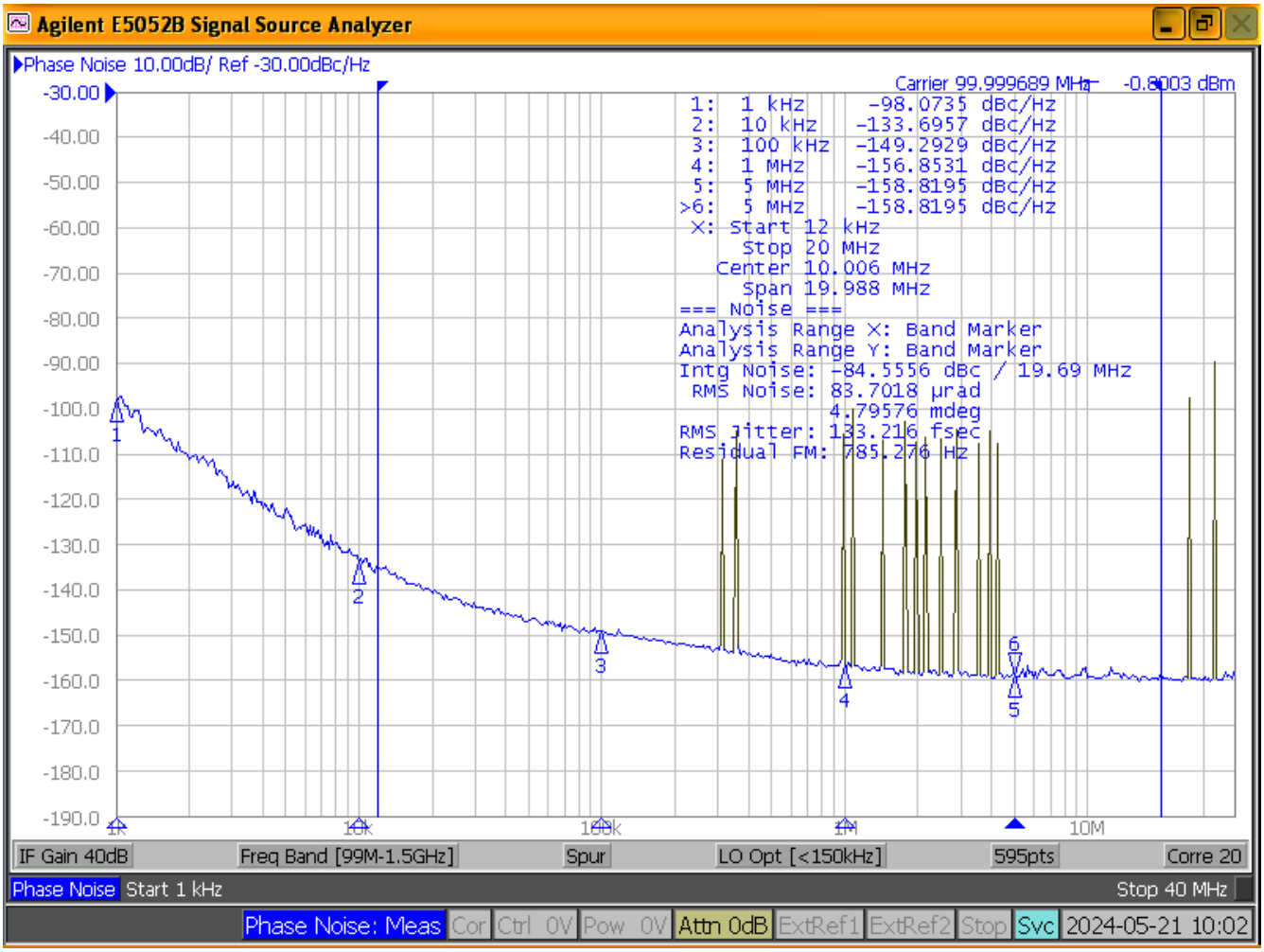


Figure 4-1. LMK3H2108EVM Typical Performance Using FOD0 Through PATH1, 100MHz

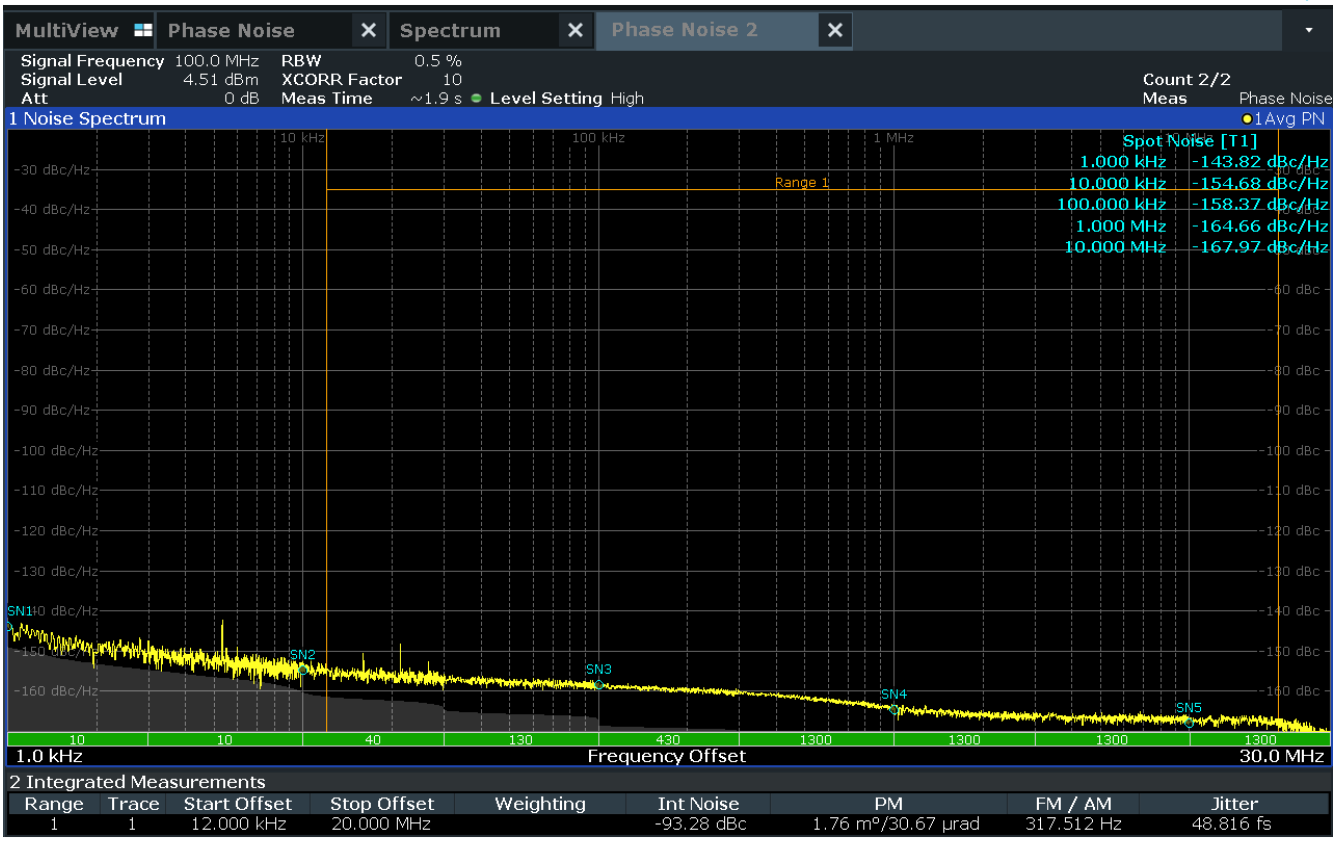


Figure 4-2. SMA100B 100MHz Input to LMK3H2108EVM for Buffer Mode Measurement

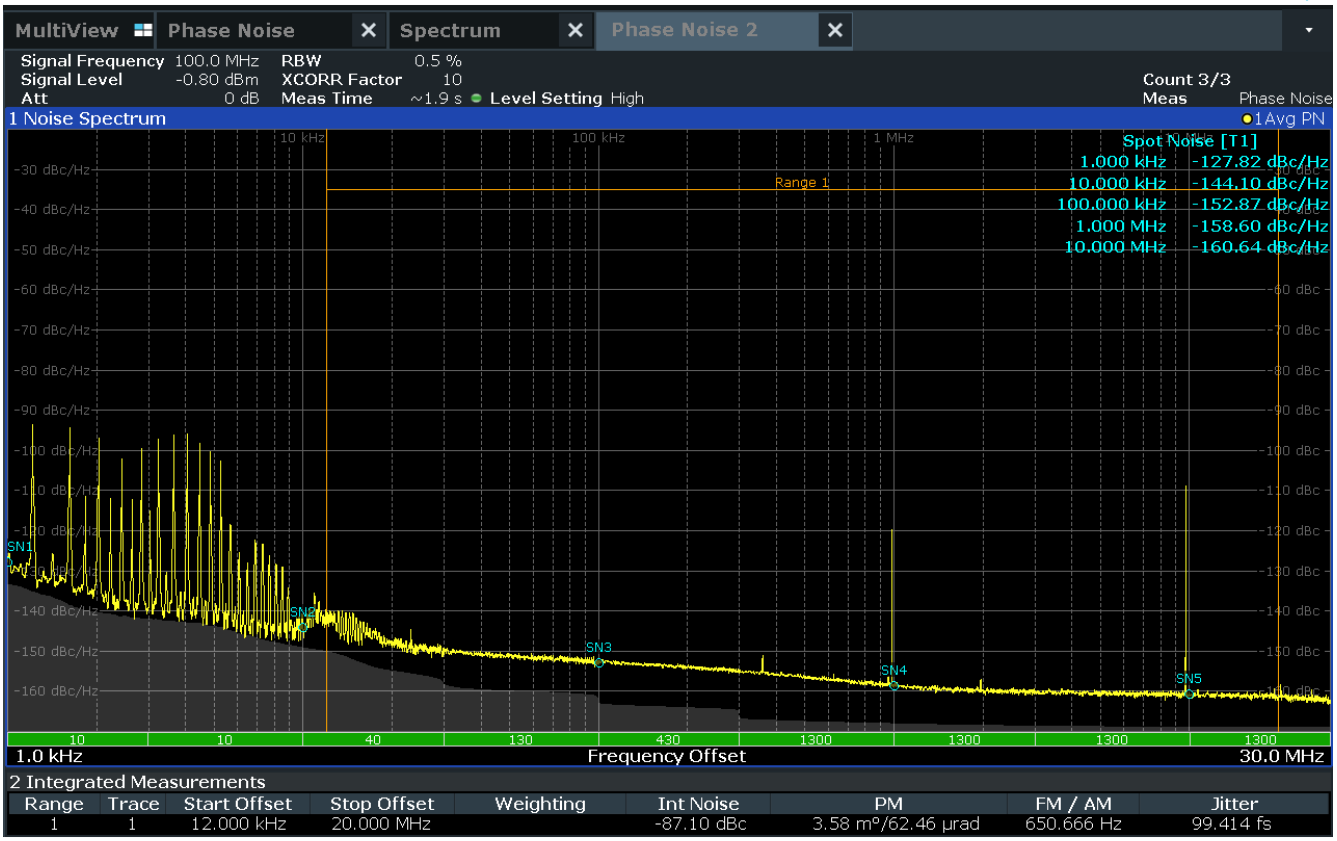


Figure 4-3. LMK3H2108 Typical Performance in Buffer Mode, SMA100B 100MHz Input

Figure 4-1 shows the typical performance of the LMK3H2108EVM when all outputs are 100MHz LP-HCSL using FOD0 routed through PATH1. TI has seen a small performance improvement when using PATH1 instead of PATH0 for the clock source, on the order of tens of femtoseconds.

Figure 4-3 shows the performance of the LMK3H2108EVM when used in buffer mode. Figure 4-2 shows the performance of the input provided to the evaluation module for buffer mode testing.

5 Hardware Design Files

5.1 Schematics

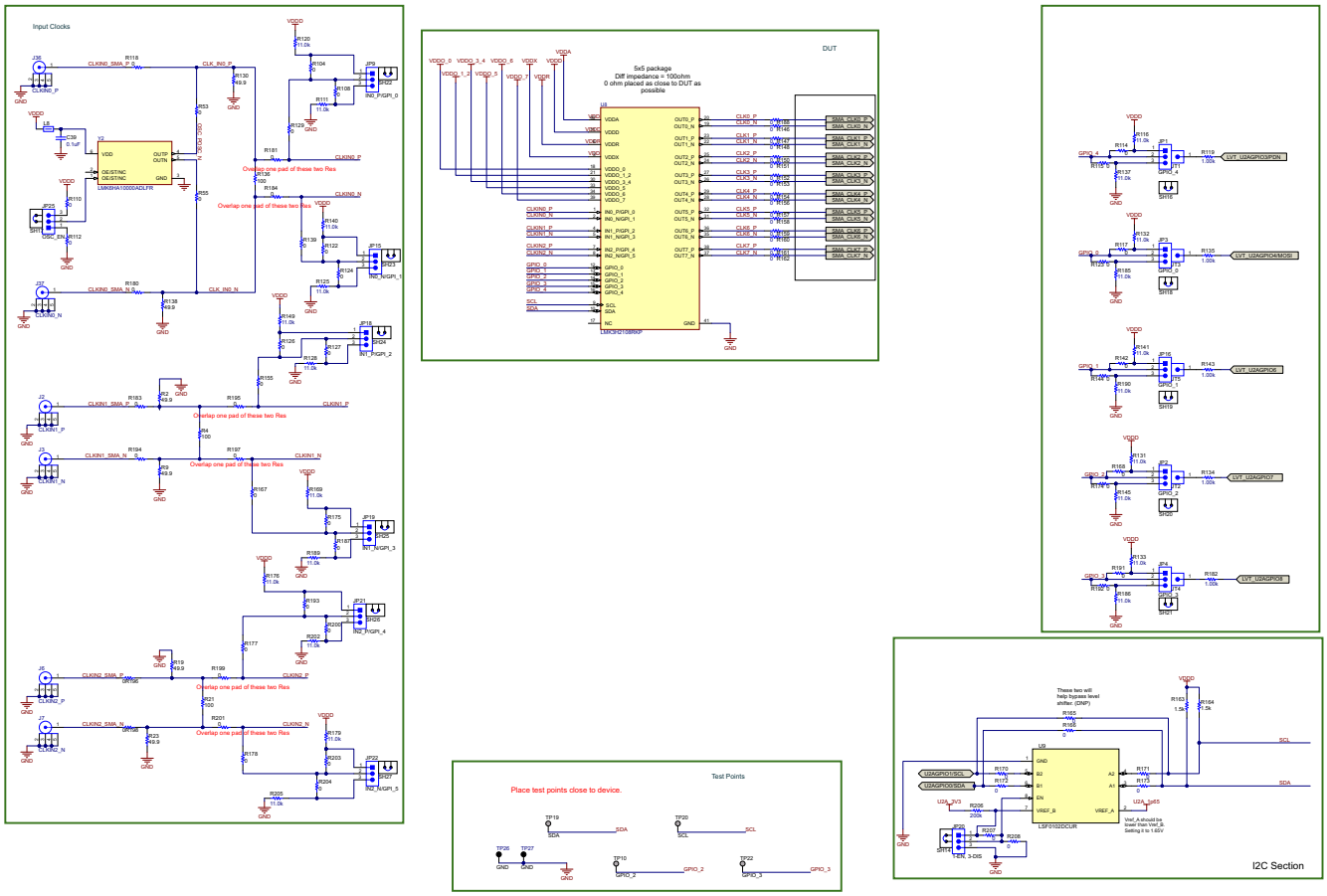


Figure 5-1. LMK3H2108EVM Device, Inputs, and GPI/GPIO

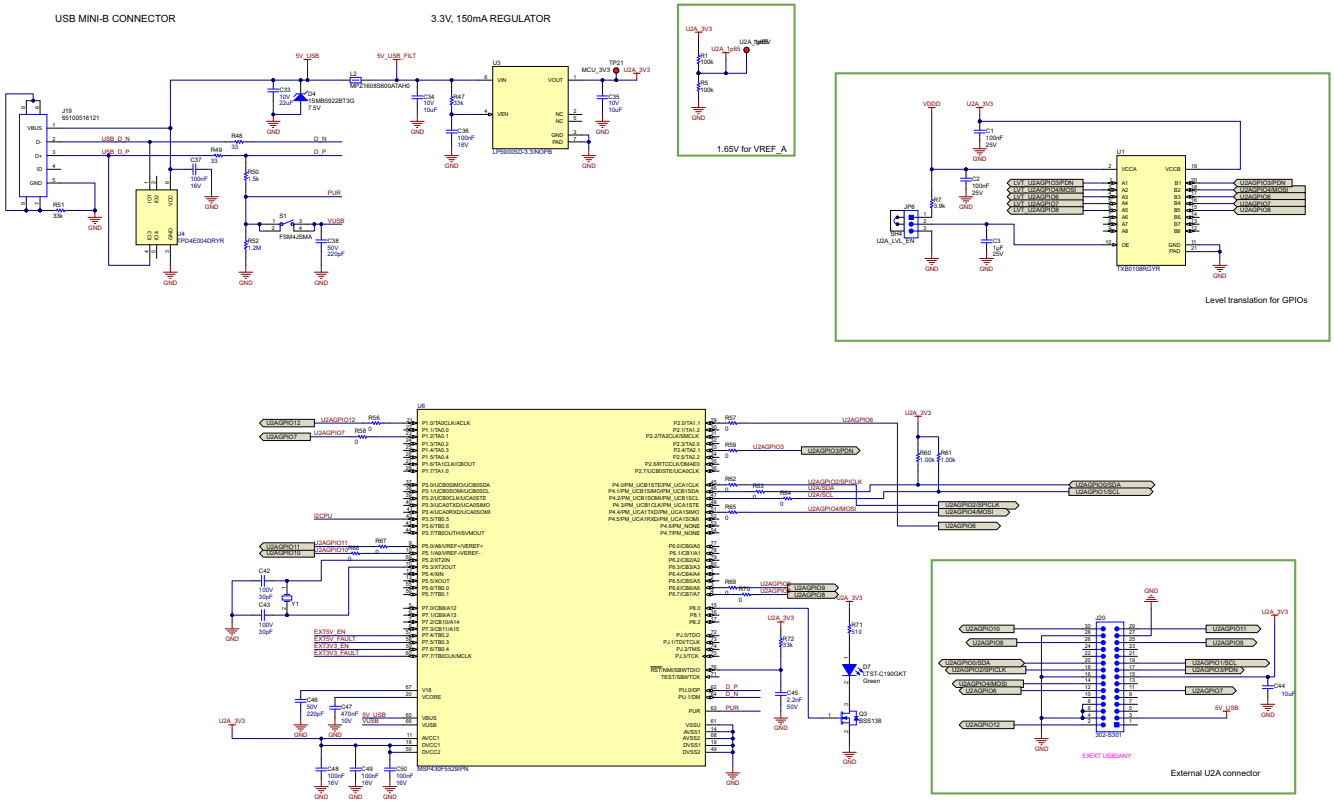


Figure 5-2. LMK3H2108EVM USB2ANY and USB Power

Note

When using a core supply voltage of 1.8V, R60 and R61 must be changed to 1kΩ resistors for successful I2C communication.

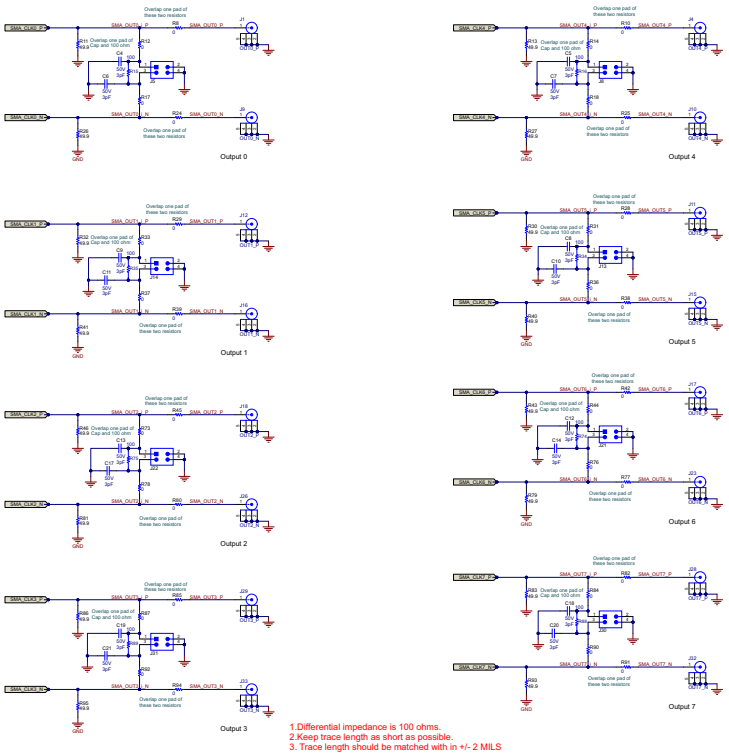


Figure 5-3. LMK3H2108EVM Outputs

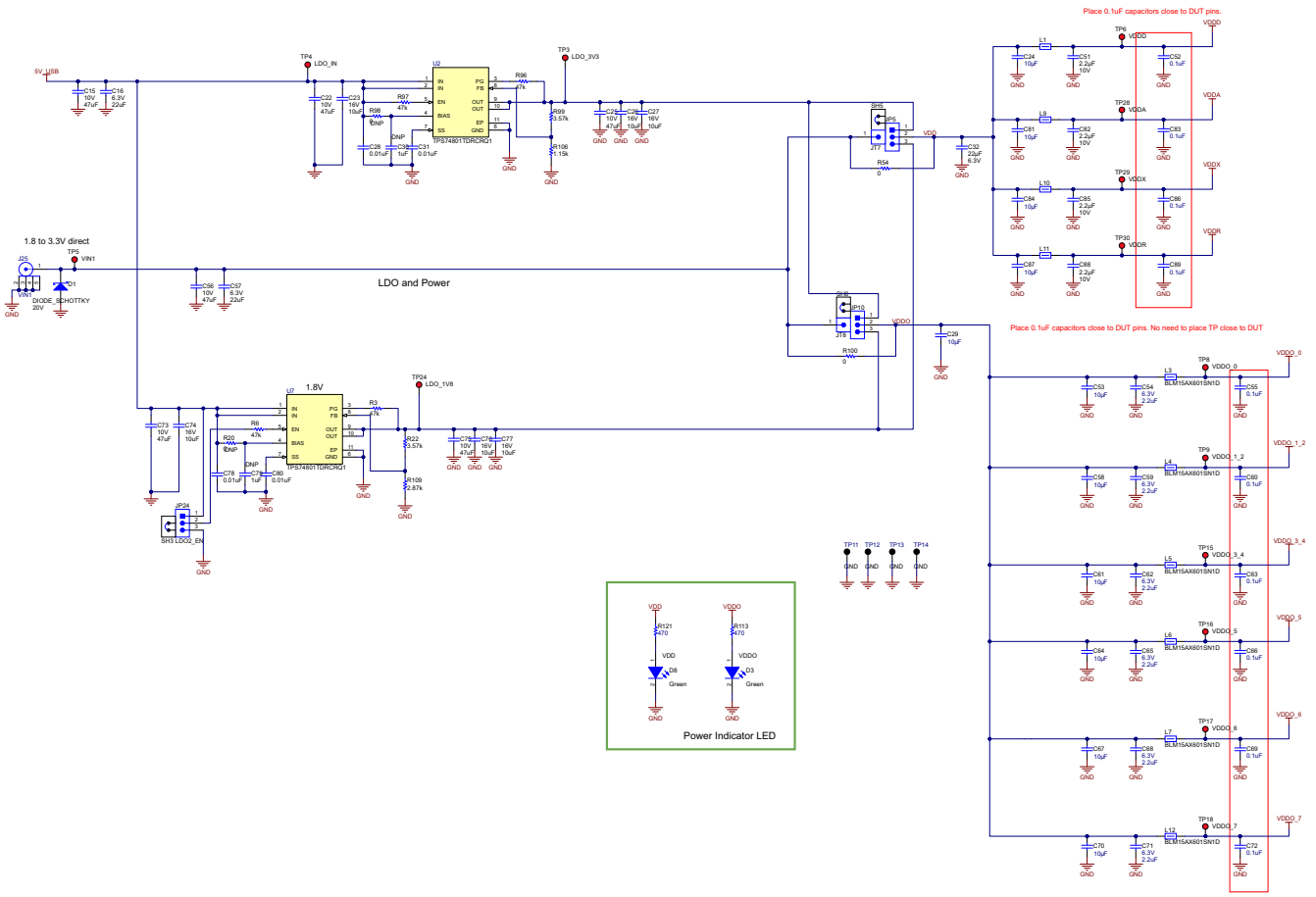


Figure 5-4. LMK3H2108EVM Power

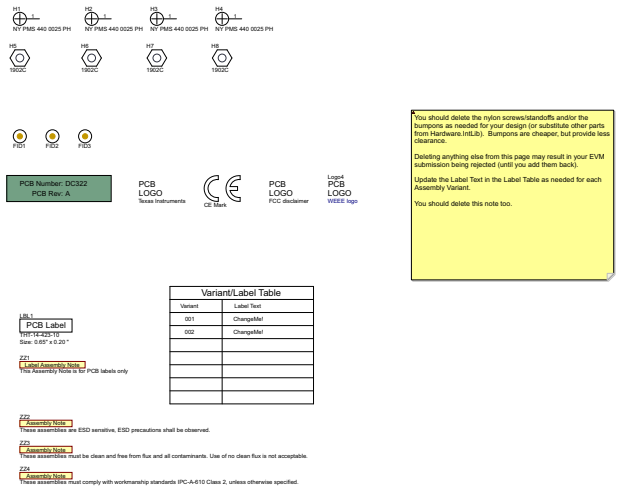


Figure 5-5. LMK3H2108EVM Hardware

5.2 PCB Layouts

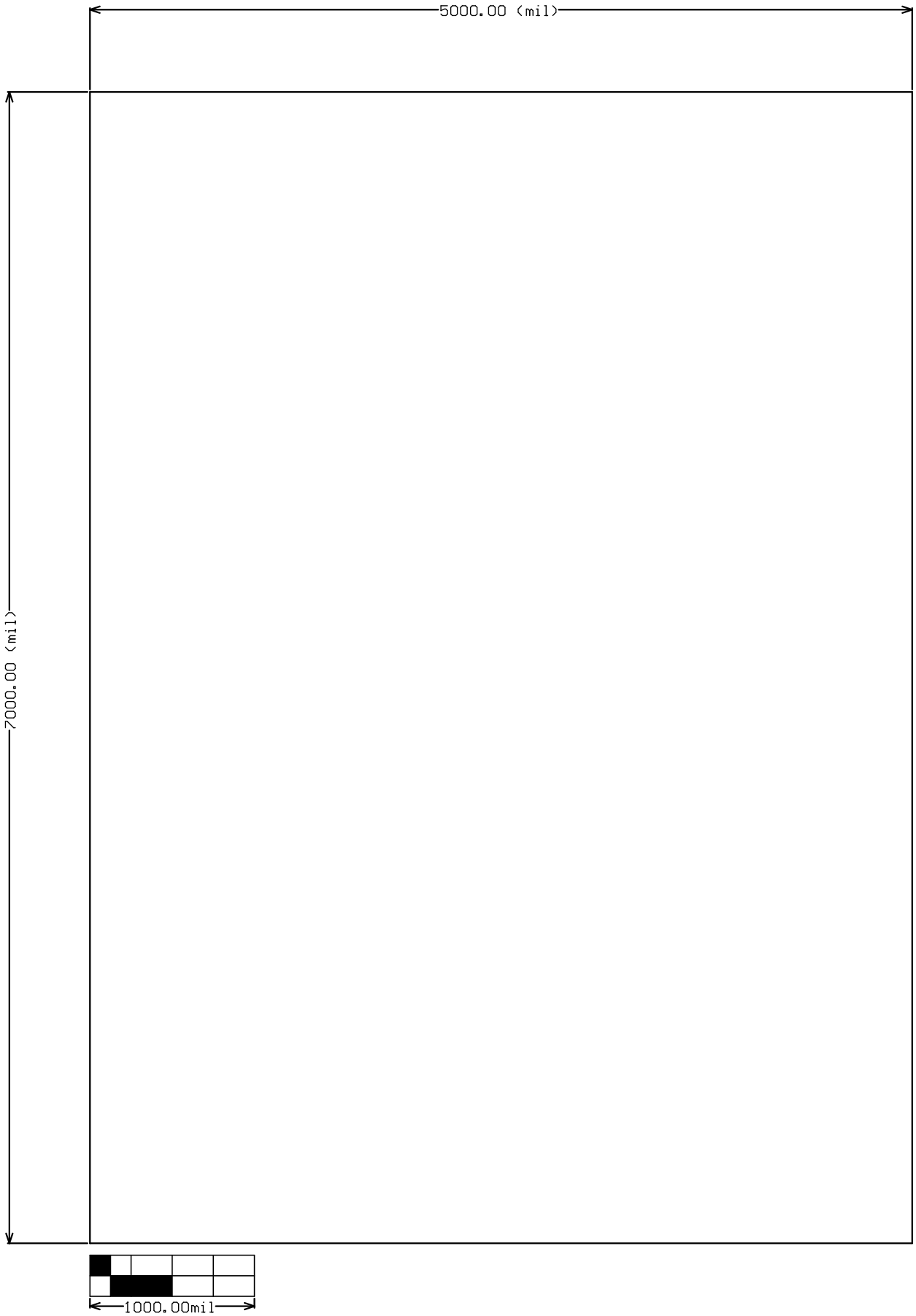


Figure 5-6. LMK3H2108EVM Board Dimensions

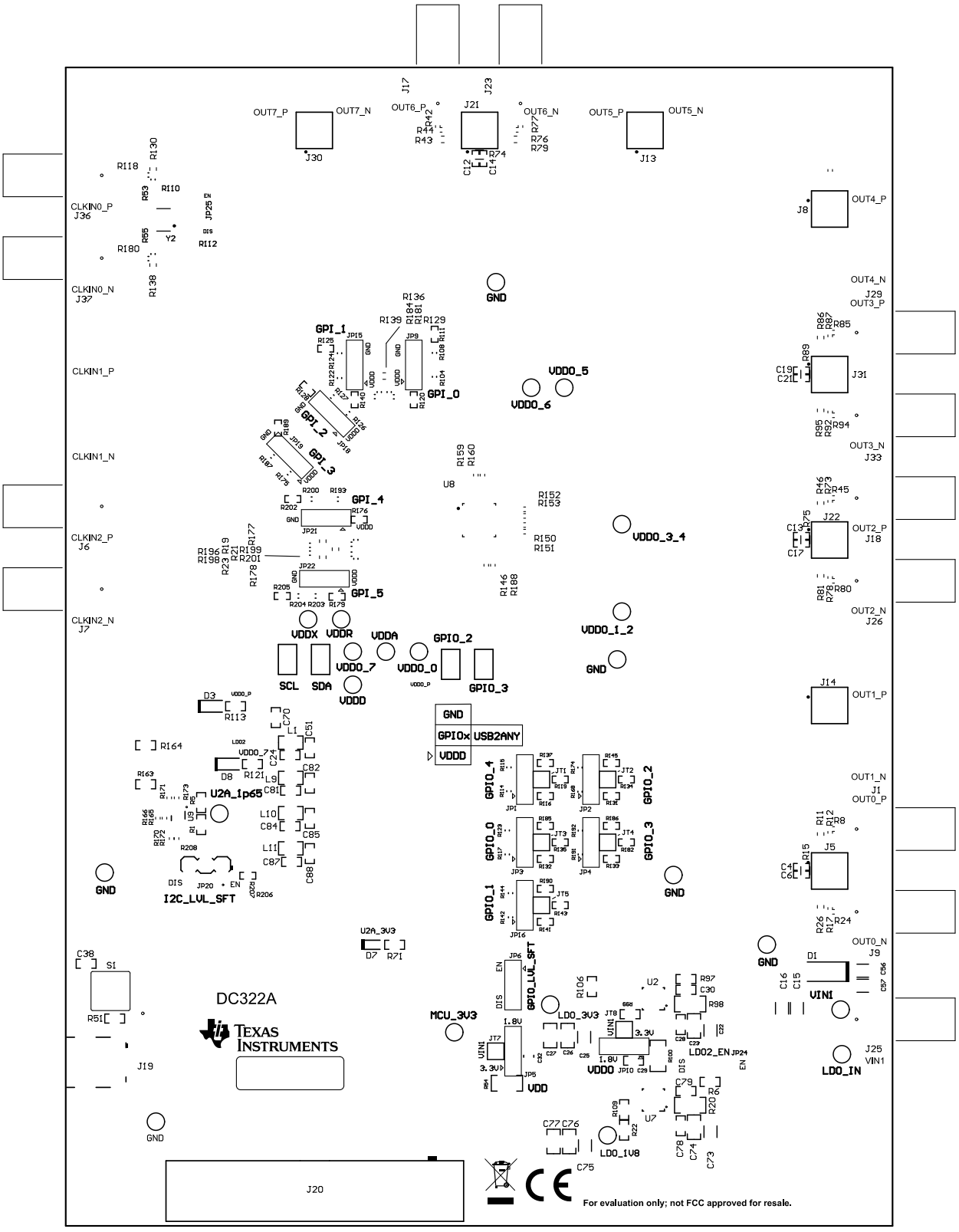


Figure 5-7. LMK3H2108EVM Top Overlay

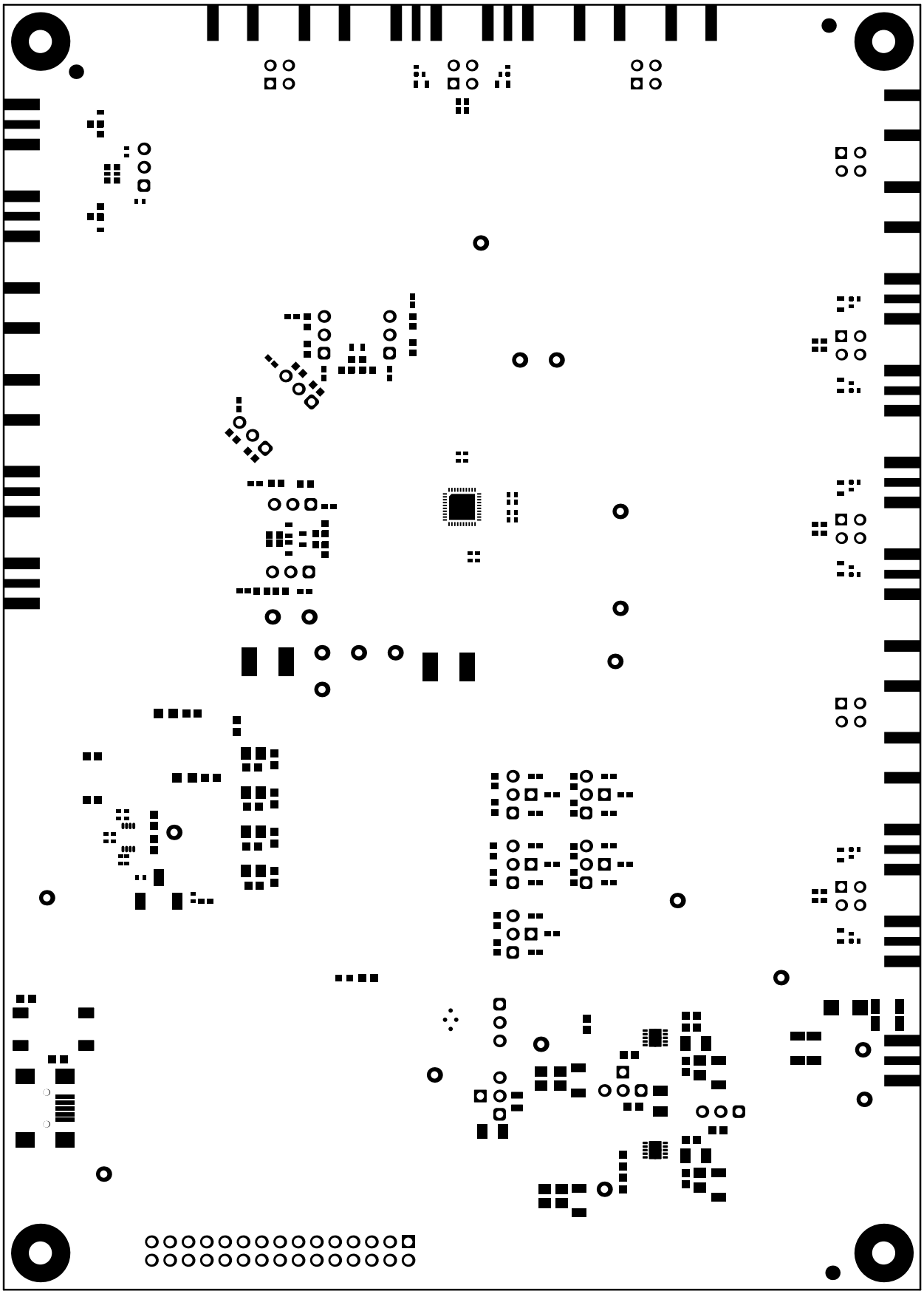


Figure 5-8. LMK3H2108EVM Top Solder Mask

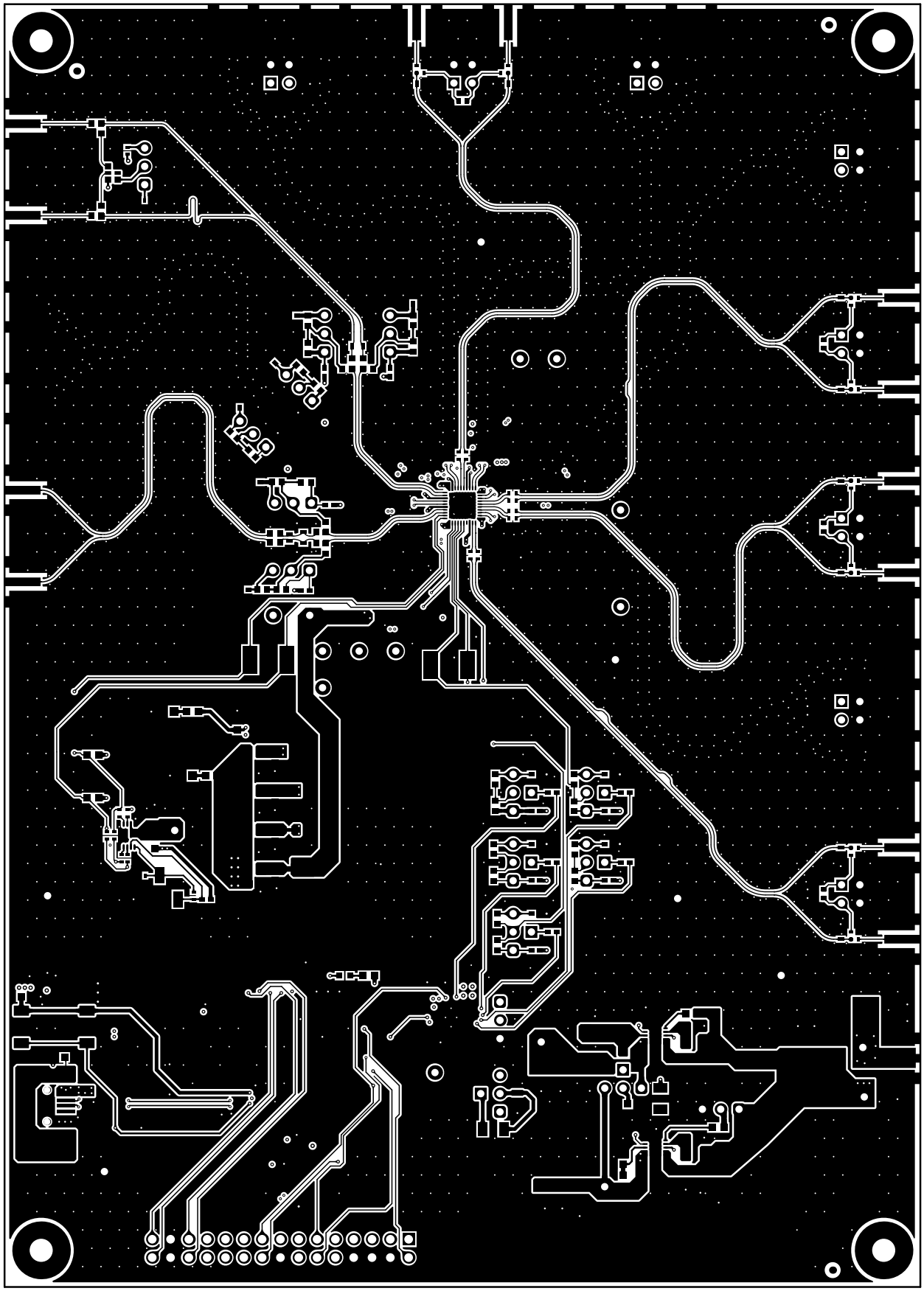


Figure 5-9. LMK3H2108EVM Top Layer

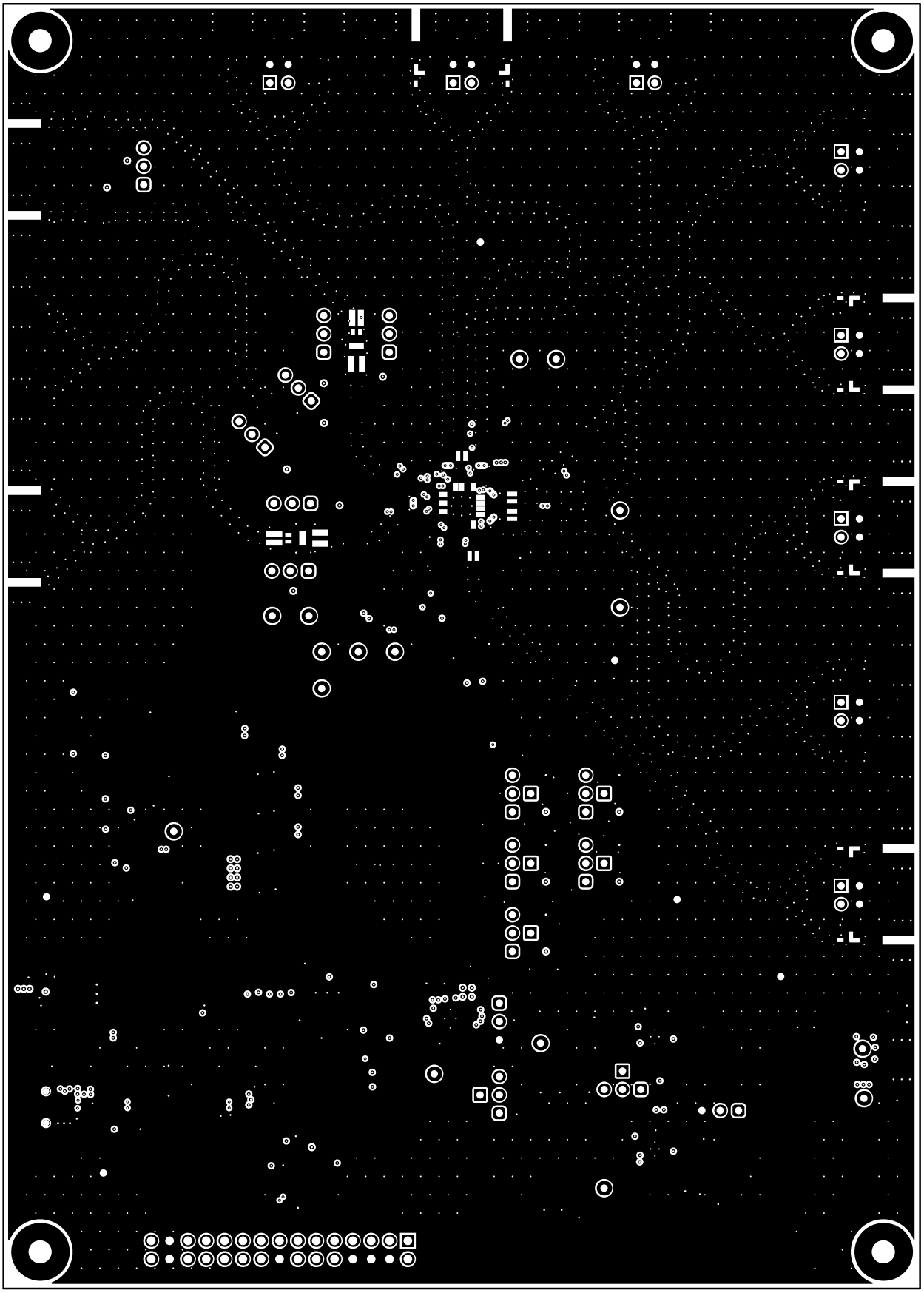


Figure 5-10. LMK3H2108EVM Signal Layer 1

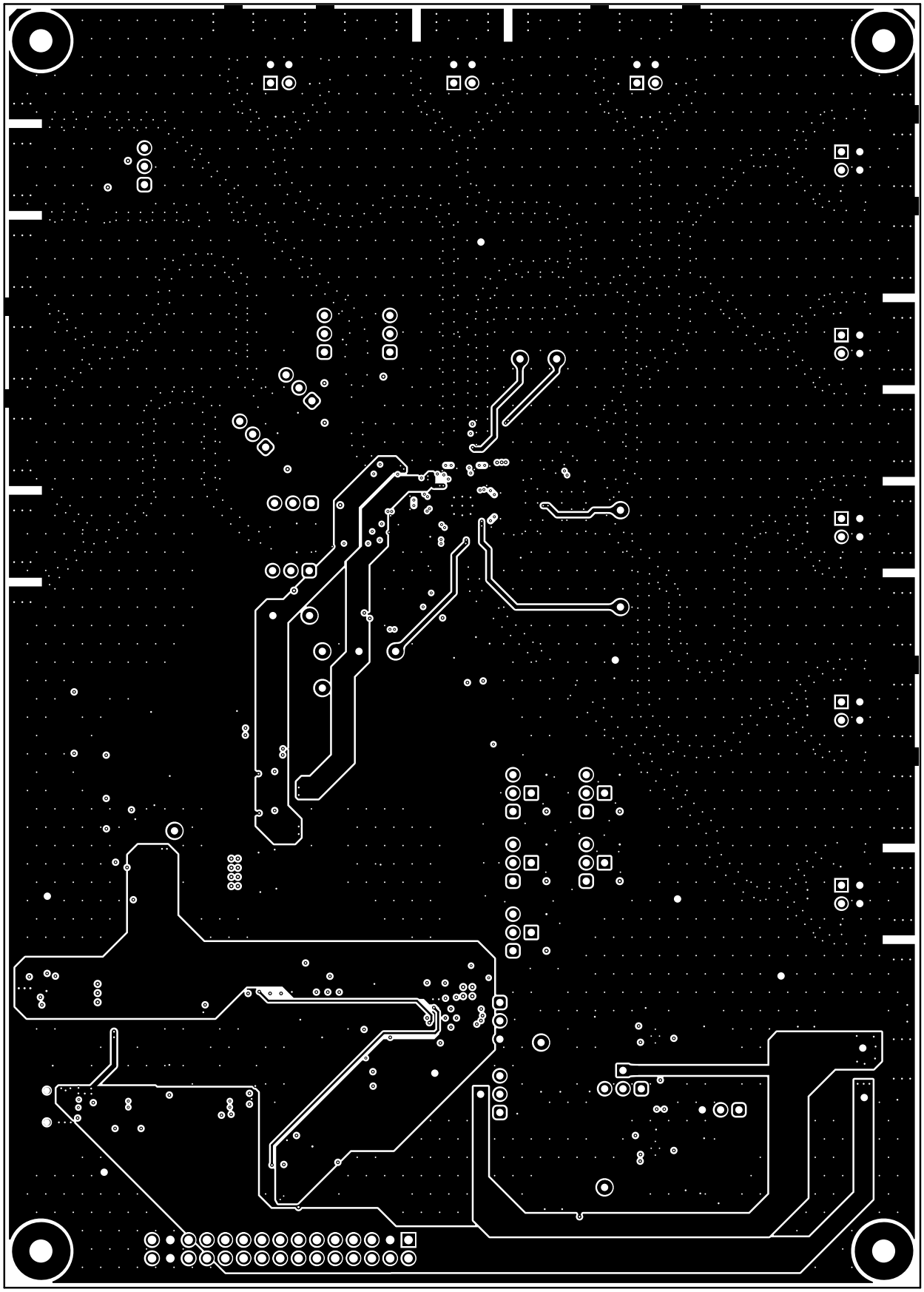


Figure 5-11. LMK3H2108EVM Signal Layer 2

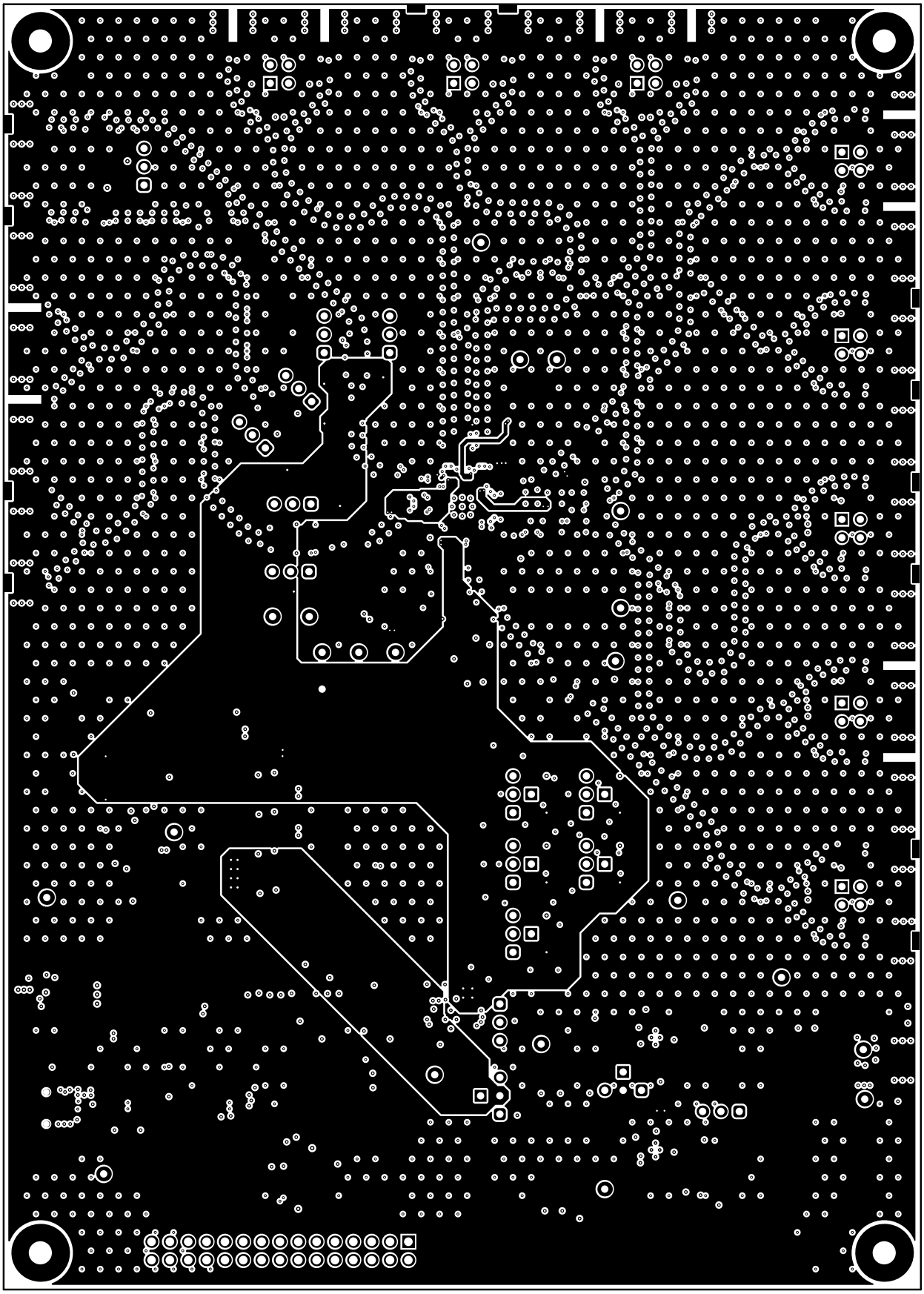


Figure 5-12. LMK3H2108EVM Signal Layer 3

Figure 5-13. LMK3H2108EVM Signal Layer 4

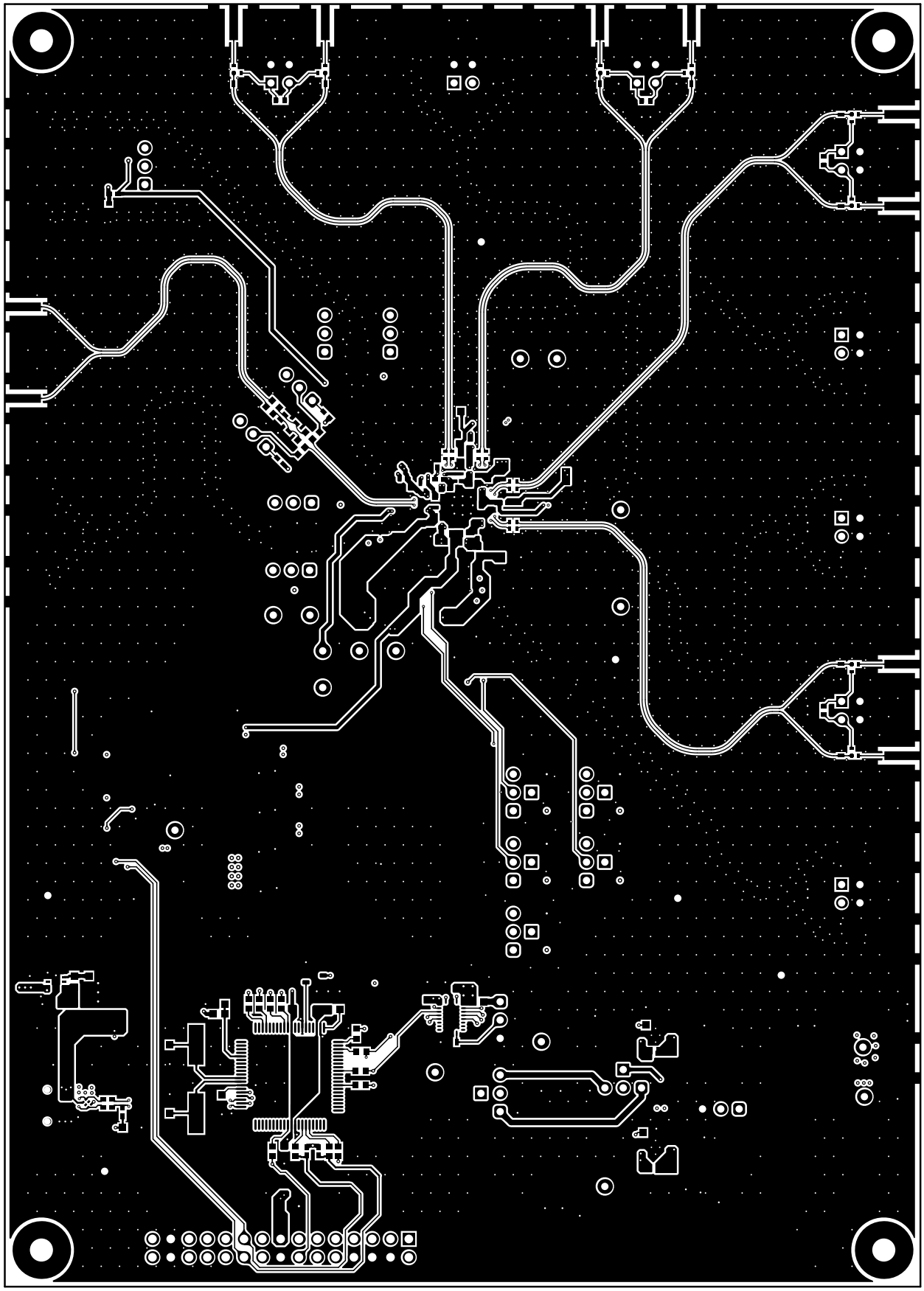


Figure 5-14. LMK3H2108EVM Bottom Layer

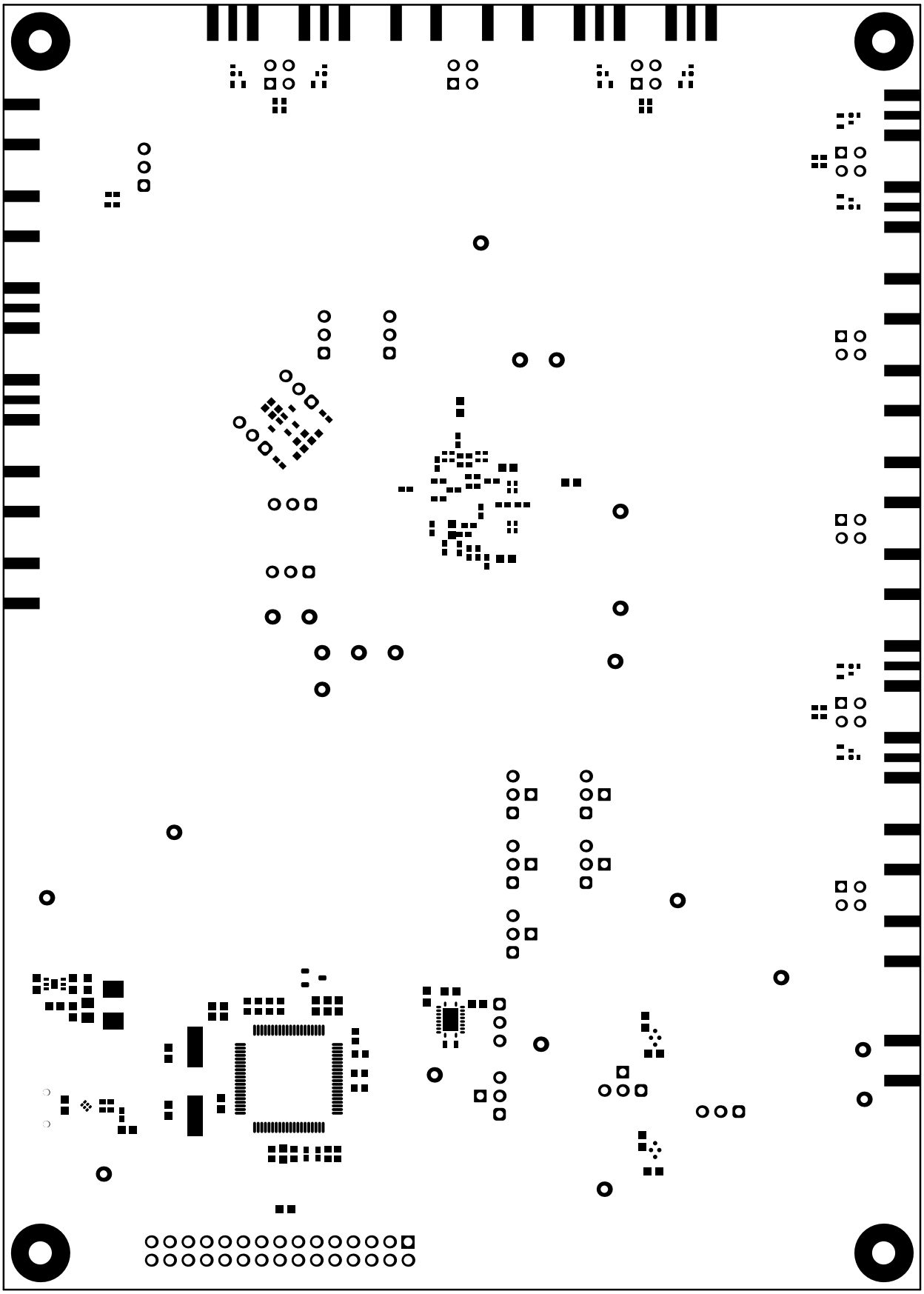


Figure 5-15. LMK3H2108EVM Bottom Solder Mask

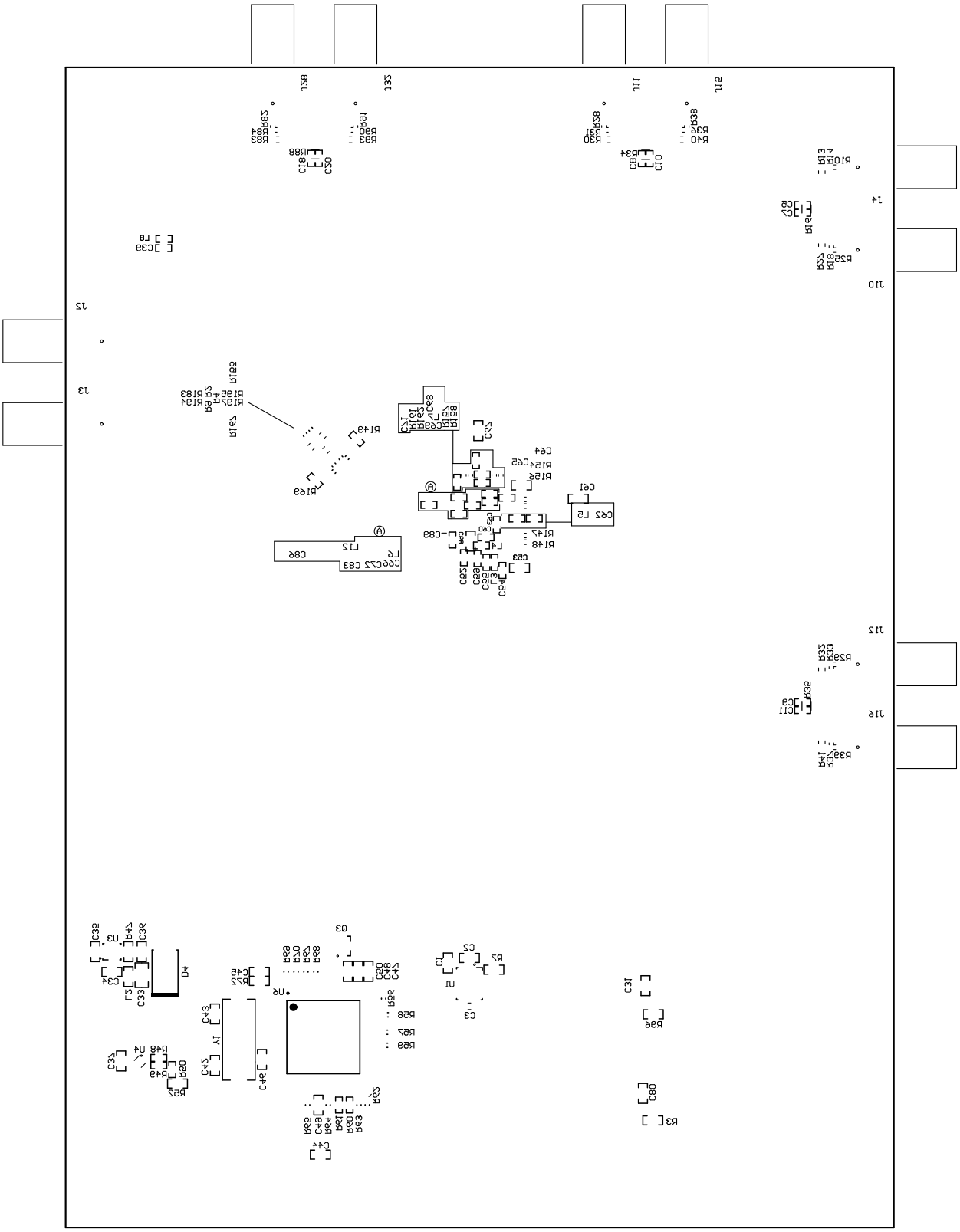
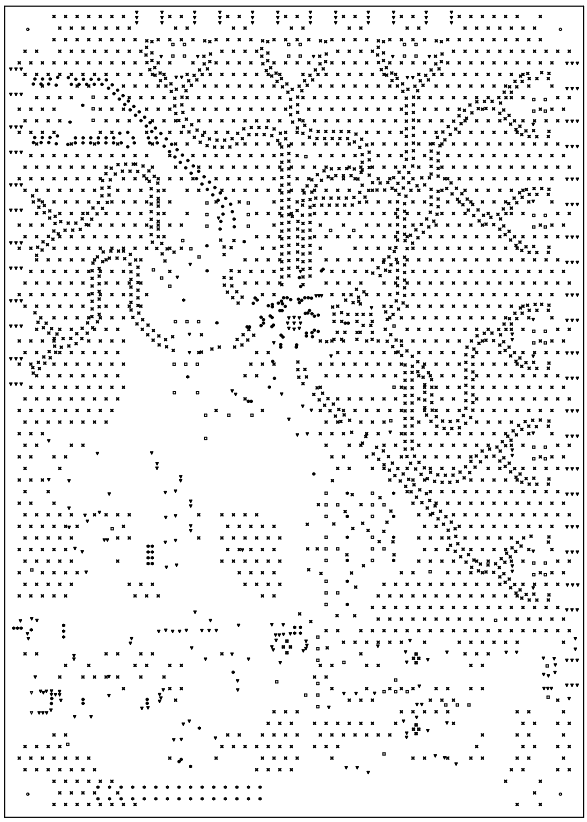


Figure 5-16. LMK3H2108EVM Bottom Overlay



DRILL TABLE

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
▽	2	35.43mil (0.900mm)	NPTH	Round	Top Layer - Bottom Layer	-0mil/+2mil
○	4	125.98mil (3.200mm)	NPTH	Round	Top Layer - Bottom Layer	-0mil/+2mil
⊠	12	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	-3mil/+3mil
⊗	170	8.00mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer	-3mil/+3mil
⊠	2641	8.10mil (0.206mm)	PTH	Round	Top Layer - Bottom Layer	-3mil/+3mil
▽	331	10.00mil (0.254mm)	PTH	Round	Top Layer - Bottom Layer	-3mil/+3mil
✱	39	12.00mil (0.305mm)	PTH	Round	Top Layer - Bottom Layer	-3mil/+3mil
□	109	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	-3mil/+3mil
☼	30	47.24mil (1.200mm)	PTH	Round	Top Layer - Bottom Layer	-3mil/+3mil
	3338 Total					

Figure 5-17. LMK3H2108EVM Drill Drawing

5.3 Bill of Materials (BOM)

FITTED	DESCRIPTION	DESIGNATOR	PARTNUMBER	QUANTITY	MANUFACTURER	PACKAGEREFERENCE	VALUE
Fitted	Printed Circuit Board	!PCB1	DC322	1	Any		
Fitted	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	C1, C2	CGA3E2X7R1E104K080AA	2	TDK	0603	0.1uF
Fitted	CAP, CERM, 1 µF, 25 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	C3	CGA3E1X7R1E105K080AC	1	TDK	0603	1uF
Fitted	CAP, CERM, 47 uF, 10 V, +/- 10%, X5R, AEC-Q200 Grade 1, 1206	C15, C22, C25, C56, C73, C75	GRT31CR61A476KE13L	6	MuRata	1206	47uF
Fitted	CAP, CERM, 22 uF, 6.3 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	C16, C57	GRT31CR70J226KE13L	2	MuRata	1206	22uF
Fitted	CAP, CERM, 10 uF, 16 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0805	C23, C26, C27, C74, C76, C77	CGA4J1X7S1C106K125AC	6	TDK	0805	10uF
Fitted	CAP, CERM, 10 µF, 16 V,+/- 20%, X6S, 0603	C24, C29, C53, C58, C61, C64, C67, C70, C81, C84, C87	GRM188C81C106MA73D	11	MuRata	0603	10uF
Fitted	CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0603	C28, C31, C78, C80	C0603C103J5RACTU	4	Kemet	0603	0.01uF
Fitted	CAP, CERM, 1 uF, 10 V, +/- 10%, X5R, 0603	C30, C79	C0603C105K8PACTU	2	Kemet	0603	1uF
Fitted	CAP, CERM, 22 µF, 6.3 V,+/- 20%, X7T, AEC-Q200 Grade 1, 0805	C32	CGA4J1X7T0J226M	1	TDK	0805	22uF
Fitted	CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0805	C33	LMK212BJ226MG-T	1	Taiyo Yuden	0805	22uF
Fitted	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0603	C34, C35, C44	C1608X5R1A106M080AC	3	TDK	0603	10uF
Fitted	CAP, CERM, 0.1 uF, 16 V, +/- 5%, X7R, 0603	C36, C37, C48, C49, C50	C0603C104J4RACTU	5	Kemet	0603	0.1uF
Fitted	CAP, CERM, 220 pF, 50 V, +/- 1%, C0G/NP0, 0603	C38, C46	06035A221FAT2A	2	AVX	0603	220pF
Fitted	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X7R, 0402	C39, C52, C55, C60, C63, C66, C69, C72, C83, C86, C89	GRM155R71A104KA01D	11	MuRata	0402	0.1uF
Fitted	CAP, CERM, 30 pF, 100 V, +/- 5%, C0G/NP0, 0603	C42, C43	GRM1885C2A300JA01D	2	MuRata	0603	30pF
Fitted	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603	C45	C0603C222K5RACTU	1	Kemet	0603	2200pF
Fitted	CAP, CERM, 0.47 uF, 10 V, +/- 10%, X7R, 0603	C47	GRM188R71A474KA61D	1	MuRata	0603	0.47uF
Fitted	CAP, CERM, 2.2 µF, 10 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	C51, C82, C85, C88	GRM188R71A225KE15J	4	MuRata	0603	2.2uF
Fitted	CAP, CERM, 2.2 uF, 6.3 V, +/- 20%, X5R, 0402	C54, C59, C62, C65, C68, C71	GRM155R60J225ME15D	6	MuRata	0402	2.2uF

FITTED	DESCRIPTION	DESIGNATOR	PARTNUMBER	QUANTITY	MANUFACTURER	PACKAGEREFERENCE	VALUE
Fitted	Diode, Schottky, 20 V, 2 A, SMA	D1	B220A-13-F	1	Diodes Inc.	SMA	20V
Fitted	LED, Green, SMD	D3, D8	LTST-C171GKT	2	Lite-On	0805 LED	Green
Fitted	Diode, Zener, 7.5 V, 550 mW, SMB	D4	1SMB5922BT3G	1	ON Semiconductor	SMB	7.5V
Fitted	LED, Green, SMD	D7	LTST-C190GKT	1	Lite-On	1.6x0.8x0.8mm	Green
Fitted	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	H1, H2, H3, H4	NY PMS 440 0025 PH	4	B&F Fastener Supply	Screw	
Fitted	Standoff, Hex, 0.5"L #4-40 Nylon	H5, H6, H7, H8	1902C	4	Keystone	Standoff	
Fitted	CONN SMA JACK STR EDGE MNT	J1, J2, J3, J4, J6, J7, J9, J10, J11, J12, J15, J16, J17, J18, J23, J25, J26, J28, J29, J32, J33, J36, J37	CON-SMA-EDGE-S	23	RF Solutions Ltd.	CONN_JACK	
Fitted	Header, 100mil, 2x2, Tin, TH	J5, J8, J13, J14, J21, J22, J30, J31	PEC02DAAN	8	Sullins Connector Solutions	Header, 2x2, 2.54mm, TH	
Fitted	Connector, Receptacle, USB Mini B 2.0, SMT	J19	65100516121	1	Wurth Elektronik	Connector, Receptacle, USB Mini B 2.0, 5 Position, SMT	
Fitted	Header(shrouded), 2.54mm, 15x2, Gold, TH	J20	302-S301	1	On-Shore Technology	Header(shrouded), 2.54mm, 15x2, TH	
Fitted	Header, 100mil, 3x1, Gold, TH	JP1, JP2, JP3, JP4, JP5, JP6, JP9, JP10, JP15, JP16, JP18, JP19, JP21, JP22, JP24, JP25	TSW-103-07-G-S	16	Samtec	3x1 Header	
Fitted	Header, 2.54mm, 3x1, Gold, SMT	JP20	M20-8770342	1	Harwin	Header, 2.54mm, 3x1, SMT	
Fitted	Header, 100mil, 1pos, Gold, TH	JT1, JT2, JT3, JT4, JT5, JT7, JT8	TSW-101-07-G-S	7	Samtec	Testpoint	
Fitted	Ferrite Bead, 600 ohm @ 100 MHz, 2 A, 0805	L1, L9, L10, L11	UPZ2012E601-2R0TF	4	Sunlord	0805	600 ohm
Fitted	Ferrite Bead, 60 ohm @ 100 MHz, 3.5 A, 0603	L2	MPZ1608S600ATAH0	1	TDK	0603	60 ohm
Fitted	Ferrite Bead, 600 ohm @ 100 MHz, 0.5 A, 0402	L3, L4, L5, L6, L7, L8, L12	BLM15AX601SN1D	7	MuRata	0402	600 ohm
Fitted	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	LBL1	THT-14-423-10	1	Brady	PCB Label 0.650 x 0.200 inch	

FITTED	DESCRIPTION	DESIGNATOR	PARTNUMBER	QUANTITY	MANUFACTURER	PACKAGEREFERENCE	VALUE
Fitted	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	Q3	BSS138	1	Fairchild Semiconductor	SOT-23	50V
Fitted	RES, 100 k, 0.5%, 0.1 W, AEC-Q200 Grade 0, 0603	R1, R5	CRCW0603100KDHEAP	2	Vishay-Dale	0603	100k
Fitted	RES, 47 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	R3, R6, R96, R97	CRCW060347K0JNEA	4	Vishay-Dale	0603	47k
Fitted	RES, 3.9 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	R7	CRCW06033K90JNEA	1	Vishay-Dale	0603	3.9k
Fitted	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	R8, R10, R24, R25, R28, R29, R38, R39, R42, R45, R77, R80, R82, R85, R91, R94, R110, R112, R146, R147, R148, R150, R151, R152, R153, R154, R156, R157, R158, R159, R160, R161, R162, R170, R171, R172, R173, R188	CRCW04020000Z0ED	38	Vishay-Dale	0402	0
Fitted	RES, 0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	R20, R98	CRCW12060000Z0EA	2	Vishay-Dale	1206	0
Fitted	RES, 3.57 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	R22, R99	CRCW06033K57FKEA	2	Vishay-Dale	0603	3.57k
Fitted	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	R47, R51, R72	CRCW06033K0JNEA	3	Vishay-Dale	0603	33k
Fitted	RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	R48, R49	CRCW040233R0JNED	2	Vishay-Dale	0402	33
Fitted	RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	R50	CRCW04021K50JNED	1	Vishay-Dale	0402	1.5k
Fitted	RES, 1.2 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	R52	CRCW06031M20JNEA	1	Vishay-Dale	0603	1.2Meg
Fitted	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	R53, R55, R56, R57, R58, R59, R62, R63, R64, R65, R67, R68, R69, R70, R181, R183, R184, R194, R195, R196, R197, R198, R199, R201	CRCW06030000Z0EA	24	Vishay-Dale	0603	0
Fitted	RES, 1.00 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	R60, R61, R119, R134, R135, R143, R182	CRCW04021K00FKED	7	Vishay-Dale	0402	1.00k
Fitted	RES, 510, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	R71	CRCW0603510RJNEA	1	Vishay-Dale	0603	510
Fitted	RES, 1.15 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	R106	CRCW06031K15FKEA	1	Vishay-Dale	0603	1.15k

FITTED	DESCRIPTION	DESIGNATOR	PARTNUMBER	QUANTITY	MANUFACTURER	PACKAGEREFERENCE	VALUE
Fitted	RES, 2.87 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	R109	CRCW06032K87FKEA	1	Vishay-Dale	0603	2.87k
Fitted	RES, 11.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	R111, R116, R120, R125, R128, R131, R132, R133, R137, R140, R141, R145, R149, R169, R176, R179, R185, R186, R189, R190, R202, R205	CRCW040211K0FKED	22	Vishay-Dale	0402	11.0k
Fitted	RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	R113, R121	CRCW0603470RJNEA	2	Vishay-Dale	0603	470
Fitted	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	R130, R138	CRCW060349R9FKEA	2	Vishay-Dale	0603	49.9
Fitted	RES, 1.5 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	R163, R164	CRCW06031K50JNEA	2	Vishay-Dale	0603	1.5k
Fitted	RES, 200 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	R206	CRCW040220 0KFKED	1	Vishay-Dale	0402	200k
Fitted	Switch, Tactile, SPST-NO, 0.05A, 12V, SMT	S1	FSM4JSMA	1	TE Connectivity	SW, SPST 6x6 mm	
Fitted	Shunt, 100mil, Gold plated, Black	SH3, SH4, SH5, SH8, SH14, SH16, SH17, SH18, SH19, SH20, SH21, SH22, SH23, SH24, SH25, SH26, SH27	SNT-100-BK-G	17	Samtec	Shunt	1x2
Fitted	Test Point, Miniature, Red, TH	TP3, TP4, TP5, TP6, TP8, TP9, TP15, TP16, TP17, TP18, TP21, TP24, TP28, TP29, TP30, U2A_1p65	5000	16	Keystone	Red Miniature Testpoint	
Fitted	Test Point, Miniature, SMT	TP10, TP19, TP20, TP22	5019	4	Keystone	Test Point, Miniature, SMT	
Fitted	Test Point, Miniature, Black, TH	TP11, TP12, TP13, TP14, TP26, TP27	5001	6	Keystone	Black Miniature Testpoint	
Fitted	8-Bit Bidirectional Voltage-Level Shifter with Auto Direction Sensing and +/-15-kV ESD Protect, RGY0020A (VQFN-20)	U1	TXB0108RGYR	1	Texas Instruments	RGY0020A	
Fitted	Single Output LDO, 1.5 A, Adjustable 0.8 to 3.6 V Output, 0.8 to 5.5 V Input, with Programmable Soft Start, 10-pin SON (DRC), -40 to 105 degC, Green (RoHS & no Sb/Br)	U2, U7	TPS74801TDRCRQ1	2	Texas Instruments	DRC0010A	

FITTED	DESCRIPTION	DESIGNATOR	PARTNUMBER	QUANTITY	MANUFACTURER	PACKAGEREFERENCE	VALUE
Fitted	150-mA Ultra-Low Noise LDO for RF and Analog Circuits Requires No Bypass Capacitor, NGF0006A (WSON-6)	U3	LP5900SD-3.3/NOPB	1	Texas Instruments	NGF0006A	
Fitted	4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	U4	TPD4E004DRYR	1	Texas Instruments	DRY0006A	
Fitted	25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	U6	MSP430F5529IPN	1	Texas Instruments	PN0080A	
Fitted	8-Output PCIe Gen 1-6 Compliant Low jitter General Purpose BAW Clock Generator	U8	LMK3H2108RKPR	1	Texas Instruments	QFN40	
Fitted	Dual Bidirectional Multi-Voltage Level Translator, DCU0008A (VSSOP-8)	U9	LSF0102DCUR	1	Texas Instruments	DCU0008A	
Fitted	Crystal, 24.000 MHz, 20pF, SMD	Y1	ECS-240-20-5PX-TR	1	ECS Inc.	Crystal, 11.4x4.3x3.8 mm	
Fitted	Low Jitter, High-Performance BAW Oscillator, 156.25MHz, 100MHz	Y2	LMK6HA10000ADLFR	1	Texas Instruments	VSON6	
Not Fitted	CAP, CERM, 3 pF, 50 V, +/-5%, C0G/NP0, 0402	C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C17, C18, C19, C20, C21	GRM1555C1H3R0CA01D	0	MuRata	0402	3pF
Not Fitted	Fiducial mark. There is nothing to buy or mount.	FID1, FID2, FID3	N/A	0	N/A	N/A	
Not Fitted	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	R2, R9, R11, R13, R19, R23, R26, R27, R30, R32, R40, R41, R43, R46, R79, R81, R83, R86, R93, R95	CRCW060349R9FKEA	0	Vishay-Dale	0603	49.9
Not Fitted	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	R4, R21, R136	CRCW060310 0RJNEA	0	Vishay-Dale	0603	100
Not Fitted	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	R12, R14, R17, R18, R31, R33, R36, R37, R44, R73, R76, R78, R84, R87, R90, R92, R165, R166, R207, R208	CRCW04020000Z0ED	0	Vishay-Dale	0402	0

FITTED	DESCRIPTION	DESIGNATOR	PARTNUMBER	QUANTITY	MANUFACTURER	PACKAGEREFERENCE	VALUE
Not Fitted	100 Ohms ±0.1% 0.05W, 1/20W Chip Resistor 0402 (1005 Metric) RF, High Frequency Thin Film	R15, R16, R34, R35, R74, R75, R88, R89	FC0402E1000BST0	0	Vishay Dale	0402	100
Not Fitted	RES, 0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	R54, R100	CRCW12060000Z0EA	0	Vishay-Dale	1206	0
Not Fitted	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	R104, R108, R114, R115, R117, R118, R122, R123, R124, R126, R127, R129, R139, R142, R144, R155, R167, R168, R174, R175, R177, R178, R180, R187, R191, R192, R193, R200, R203, R204	CRCW06030000Z0EA	0	Vishay-Dale	0603	0

6 Additional Information

6.1 Trademarks

All trademarks are the property of their respective owners.

7 Related Documentation

7.1 Supplemental Content

For details regarding implementation of all device behaviors, refer to the LMK3H2104 and LMK3H2108 4- and 8-Output PCIe Gen 1-7 Compliant Low jitter General Purpose BAW Clock Generator data sheet or the descriptions available by hovering over a field in TICS Pro 2.

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2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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