EVM User's Guide: LMH1239EVM

LMH1239 Evaluation Module

Description

The LMH1239 is a long reach adaptive cable equalizer with integrated reclocker, dual outputs, and 75Ω loop-through output. The device is designed to equalize data transmitted over 75Ω coaxial cable and operates across SMPTE data rates ranging from 125Mbps to 11.88Gbps.

Features

- User configurable adaptive cable equalizer or cable driver with integrated reclocker
- Supports ST-2082-1(12G), ST-2081-1(6G), ST-424(3G), ST-292(HD), and ST-259(SD)
- Integrated reclocker locks to SMPTE video rates of 11.88Gbps, 5.94Gbps, 2.97Gbps, 1.485Gbps or divide-by-1.001 sub-rates and 270Mbps
- Dual adaptive cable equalizer at 75Ω single-ended input ports SDI_IN± and SDI_IN1±
- Dual 100Ω output driver with de-emphasis output port OUT0± and OUT1±
- Line-side reclocked 75Ω loop-through output on port SDI_OUT±
- Programmable by pin, SPI, or SMBus interface
- Single supply operation: VDD = 2.5 V ± 5%
- Operating temperature: –40°C to +85°C
- High-speed signal flow-through pinout package: 5mm × 5mm 32-pin WQFN package

Applications

- SMPTE compatible serial digital interface
- UHDTV, 4K, 8K, HDTV, SDTV video
- Broadcast video routers, switches, distribution amplifiers, and monitors
- Digital video processing and editing

1 Evaluation Module Overview

1.1 Introduction

The LMH1239EVM is an evaluation module designed for high-speed performance and functional evaluation of the Texas Instruments LMH1239 12G UHD long reach cable equalizer with integrated reclocker and input mux.

With this kit, users can quickly evaluate the cable reach and output signal integrity supported by the LMH1239. High performance edge mount BNC connectors are used at the 75Ω port for the SDI_IN and SDI_OUT signals, while 100Ω differential output ports are routed to edge mount SMA connectors. These connectors facilitate connection to lab equipment or user systems for performance evaluation.

An onboard MSP430 MCU is included to support an optional SMBus or SPI serial control interface when configuring the LMH1239 operating modes.

- LMH1239 features:
  - Dual adaptive cable equalizer at 75Ω single-ended input ports SDI_IN± and SDI_IN1±
  - Dual 100Ω output driver with de-emphasis output port OUT0± and OUT1±
  - Line-side reclocked 75Ω loop-through output on port SDI_OUT±

1.2 Kit Contents

- LMH1239EVM board

1.3 Device Information

Table 1-1. LMH1239 Ordering Information

EVM ID	DEVICE ID	DEVICE PACKAGE
LMH1239EVM	LMH1239RTV	WQFN (32)

2 Hardware

2.1 Setup

The LMH1239EVM can be used in one of three modes:

1. **Pin Mode (Default)** – Provides general access to the LMH1239 signal integrity and I/O control settings with IC pin-level logic.
2. **SPI Mode** – Provides full access to the LMH1239 signal integrity and control settings through the POCI, PICO, SCK, and CS pins.
3. **SMBus Mode** – Provides full access to the LMH1239 signal integrity and control settings through the SDA, SCL, and GND pins. ADDR0 and ADDR1 pins are used for SMBus address strap.

Using either SPI or SMBus mode, users have full access to all register controls in the LMH1239. For convenience, the LMH1239EVM features an on-chip MSP430 that is configured as a USB2ANY interface between the LMH1239 and PC through the mini-USB port header on J31.

Note

Currently, the interface from the PC to the onboard MSP430 can only support SMBus communication.

The external control pins on the LMH1239EVM are used to configure the default device settings. A 4-level input scheme across the control pin interface increases the amount of control levels available to the device with fewer physical pins. The channel settings and controls are configurable in pin mode for the LMH1239 4-logic levels (L, R, F, H). The four logic levels correspond to the following voltages in Table 2-1.

Table 2-1. Description of 4-Level Voltage Inputs and Jumper Ties

LEVEL	SETTING	NOMINAL PIN VOLTAGE
H	Tie 1kΩ to VIN	VIN
F	Float (leave pin open)	2/3 × VIN
R	Tie 20kΩ to GND	1/3 × VIN
L	Tie 1kΩ to GND	0

Typical 4-level input thresholds:

- Internal threshold between L and R = 0.2 × VIN
- Internal threshold between R and F = 0.5 × VIN
- Internal threshold between F and H = 0.8 × VIN

To set these 4-level voltage inputs, each input is controlled by a group of 6 jumper pins set in Figure 2-1.

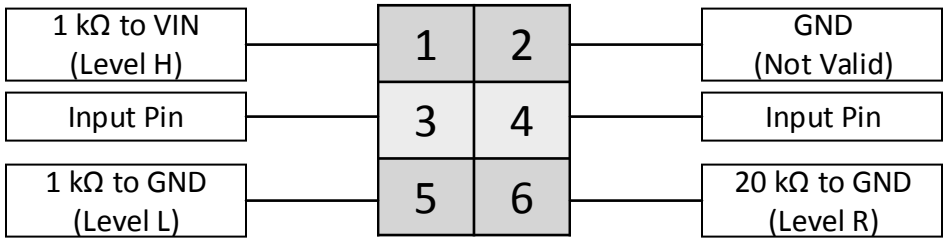

Figure 2-1. Jumper Orientation for User Configuration

Therefore, the following jumper positions allow access to each of the four logic levels:

LEVEL	JUMPER TIES
H	Pin 1-3
F	Pin 3-4 (or no connect)
R	Pin 4-6
L	Pin 3-5

The following jumpers have 4-level input control: J10, J11, J12, J13, J14, J15, J16, J17, J18, and J19.

In Pin Mode, the OUT0_OUT1_SEL, LOOP_BW_SEL, VOD_DEM_SEL, MODE_SEL, OUT_CTRL, SDI_VOD, SDI_OUT_ENA and SDI_IN_SEL pins control different LMH1239 settings. Using SPI or SMBus, these initial pin control values can be overridden by setting the appropriate override bits through register control. Both SPI and SMBus interfaces allow full control over a wide range of device settings. See Table 2-2 and Table 2-3 for jumper descriptions and differences.

Table 2-2. Description of Connections in SPI Mode (MODE_SEL = Level F)

COMPONENT	NAME	COMMENTS
J1	GND	GND power supply
J2	VIN	2.5 V VIN power supply
J5	ENABLE	Enable pin for the LMH1239. Shunt Pin 1 and 2 for proper operation. Refer to LMH1239 data sheet for detailed information.
J6	POCI	Shunt Pin 1 and 2 to connect POCI signal to J8 for proper SPI mode operation.
J7	LOCK_N	Reclocker lock indicator for the selected input. Shunt Pin 1 and 2 for proper operation. Refer to LMH1239 data sheet for detailed controls.
J8	SPI Access	SPI access pins. See data sheet and EVM schematic for detailed pin-out information.
J9	SPI Access	For SPI mode, install pin 1-2, 3-4, and 5-6 for SPI 3.3 V to 2.5 V level shift. Leave pin 7-10 open. See data sheet for additional information on SPI operation.
J10	OUT0_OUT1_SEL	OUT0_OUT1_SEL pin selects the SMA outputs. H: OUT0 and OUT1 muted. F and L: OUT0 enabled and OUT1 muted. R: OUT0 and OUT1 enabled.
J11	LOOP_BW_SEL	LOOP_BW_SEL- H: 13 MHz/7 MHz/5 MHz/3 MHz/1 MHz. F: 13 MHz/7 MHz/5 MHz/3 MHz/1 MHz. R: 800 KHz/437 KHz/312 KHz/187 KHz/62 KHz. L: 400 KHz/219 KHz/156 KHz/94 KHz/31 KHz. **Note** These are for 12 Gbps/6 Gbps/3 Gbps/HD/SD data rates. External caps are needed for H, R and L cases.
J12	VOD_DEM_SEL	VOD_DEM_SEL- H:410 mVpp, 0dB DEM F:560 mVpp, -0.9dB R: 635 mVpp, -2.4dB L: 810 mVpp, -4.0dB See data sheet and EVM schematic for additional operation information.
J13	MODE_SEL	Level F: SPI Mode
J14	OUT_CTRL	OUT_CTRL selects the signal flow from the selected IN port to the enabled outputs. OUT_CTRL selects reclocked data, reclocked data and clock, bypass reclocker (equalized data route to output driver), or both equalizer and reclocker bypassed.
J15	SDI_VOD	SDI VOD - H: About +5% (nominal) F: 800 mVpp (nominal) R: About 10% of nominal L: About -5% of nominal
J16	CS_N_ADDR0	Chip select. When CS_N is at logic low, CS_N enables SPI access to the LMH1239 peripheral device.
J17	POCI_ADDR1	POCI is the SPI serial control data output from the LMH1239 peripheral device. POCI is a 2.5V LVCMOS output.

Table 2-2. Description of Connections in SPI Mode (MODE_SEL = Level F) (continued)

COMPONENT	NAME	COMMENTS
J18	SDI_OUT_ENA	SDI_OUT_ENA pin enables or disables the SDI_OUT 75Ω output. H: SDI_OUT Disabled F and R: Do not use L: SDI_OUT Enabled See data sheet and EVM schematic for additional operation information.
J19	SDI_IN_SEL	SDI_IN_SEL pin determines the SDI-IN 75Ω input that is enabled. Level F: SDI-IN0. See data sheet and EVM schematic for additional operation information.

Table 2-3. Description of Connections in SMBus Mode (MODE_SEL = Level L)

COMPONENT	NAME	COMMENTS
J6	POCI	Leave Pin 1 and 2 open for proper SMBus operation.
J7	LOCK_N	Reclocker lock indicator for the selected input. Shunt Pin 1 and 2 for proper operation. Refer to the LMH1239 data sheet for detailed controls.
J8	SMBus Access	SMBus access pins. See the data sheet and EVM schematic for detailed pinout information.
J9	SMBus Access	External 2kΩ pullup resistor to 3.3 V supply. Install shunt jumpers on pins 7-8 and 9-10 for proper operation. Leave pins 1-6 open. See the data sheet for additional information on SMBus operation.
J13	MODE_SEL	Level L: SMBus mode.
J16	ADDR0	4-Level strap pins to determine up to 16 unique SMBus address with J17 to create AD[1:0].
J17	ADDR1	4-Level strap pins to determine up to 16 unique SMBus address with J16 to create AD[1:0]. See Table 2-5 for different SMBus address combinations.

Table 2-4. Input and Output Channel Connections

SIGNAL INPUTS AND OUTPUTS	
JUNCTION NUMBERS	**FUNCTION**
J4, J32	SDI_OUT+, SDI_OUT- (BNC single-ended)
J22, J3	SDI_IN+, SDI_IN1+ (BNC single-ended)
J22, J23	OUT0+, OUT0– (SMA)
J24, J25	OUT1+, OUT1– (SMA)

Note

Jumpers not listed in Table 2-3 are identical to the functions mentioned in Table 2-2.

2.1.1 Default Configuration of the LMH1239EVM

The default configuration for the LMH1239EVM has SDI_IN enabled while SDI_OUT and OUT1 are disabled. Figure 2-2 shows the labeled outputs and default pin shunt configuration.

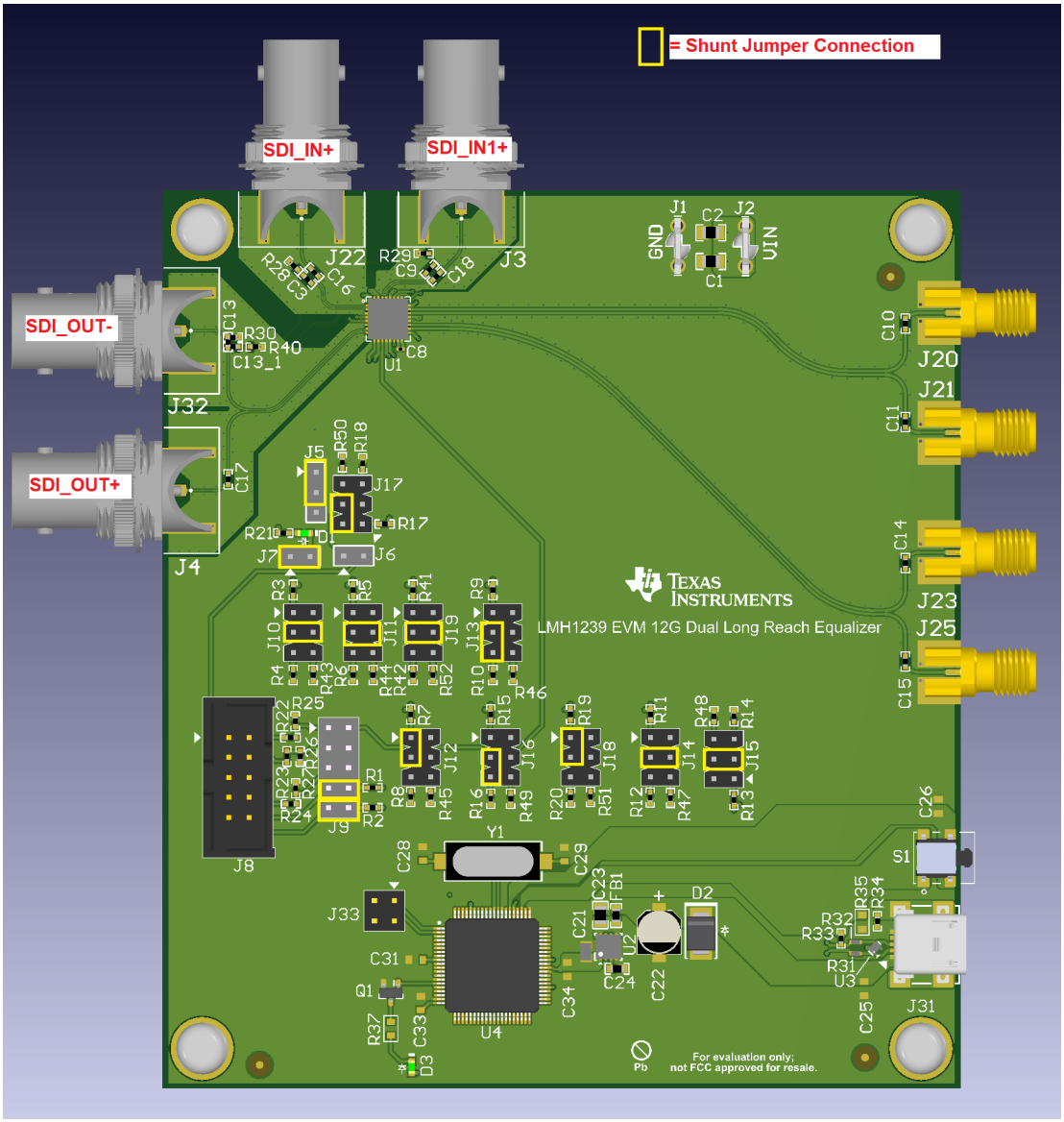

Figure 2-2. LMH1239 EVM Inputs, Outputs and Default Pin Shunt Configurations

2.1.2 Hardware and Software: Description and Setup

By factory default, the LMH1239EVM is configured to accept a valid SDI signal on SDI_IN and output the retimed data on OUT0.

The general procedure for setting up and testing with the LMH1239EVM is as follows. For pin configurations, reference the illustrations in Figure 2-3 and Figure 2-4.

1. Connect 2.5V power (0.5A maximum) to the EVM and install the appropriate shunt jumpers to operate in SMBus Mode:
   a. Connect J2: VIN = 2.5V and J1: GND.
      i. Install shunt jumper on J7 pins 1-2(H).
   b. Set the following control switches for appropriate operation:
      i. Install shunt jumper on J5 pins 1-2(H).
      ii. Install shunt jumper on J17 pins 3-5(L).
      iii. Install shunt jumpers on J9 pins 7-8 and pins 9-10.
      iv. Install shunt jumper on J10 pins 3-4(F).
      v. Install shunt jumper on J11 pins 3-4(F).
      vi. Install shunt jumper on J19 pins 3-5(L).
      vii. Install shunt jumper on J13 pins 3-5(L).
      viii. Install shunt jumper on J12 pins 1-3(H).
      ix. Install shunt jumper on J16 pins 3-5(L).
      x. Install shunt jumper on J18 pins 1-3(H).
      xi. Install shunt jumpers on J14 and J15 pins 3-4(F)
2. The LMH1239 control and signal integrity settings are programmable through the LMH1239EVM GUI. For more information about the configuration for the LMH1239EVM with the EVM GUI see Section 2.1.2.2.
3. If operating without software, then leave the mini-USB port on J31 unconnected, and refer to the LMH1239 data sheet and LMH1239EVM schematic for detailed information on how to properly set up the J11, J12, J14, J15, and J18 to the test needs.
4. SDI_OUT enabled: Connect the LMH1239EVM to the system under test.
   a. The input signal on J22 can be connected to a video signal generator over a 75Ω coax cable. Alternatively, the LMH1218EVM can be used as a 100Ω differential-to-75Ω single-ended converter. Then, the 75Ω OUT0+ of the LMH1218 can be used as an input to the SDI_IN+ of the LMH1239.
   b. The output signal on J20, J21, J23 and J25 can be connected with matched 100Ω differential cables to a high-speed scope to view the output eye diagram.
   c. The output signal on J32 can be connected with a 75Ω coax cable to a video pattern analyzer as a loop-through output because the signal is enabled in the shunt jumper settings shown in the figure below.

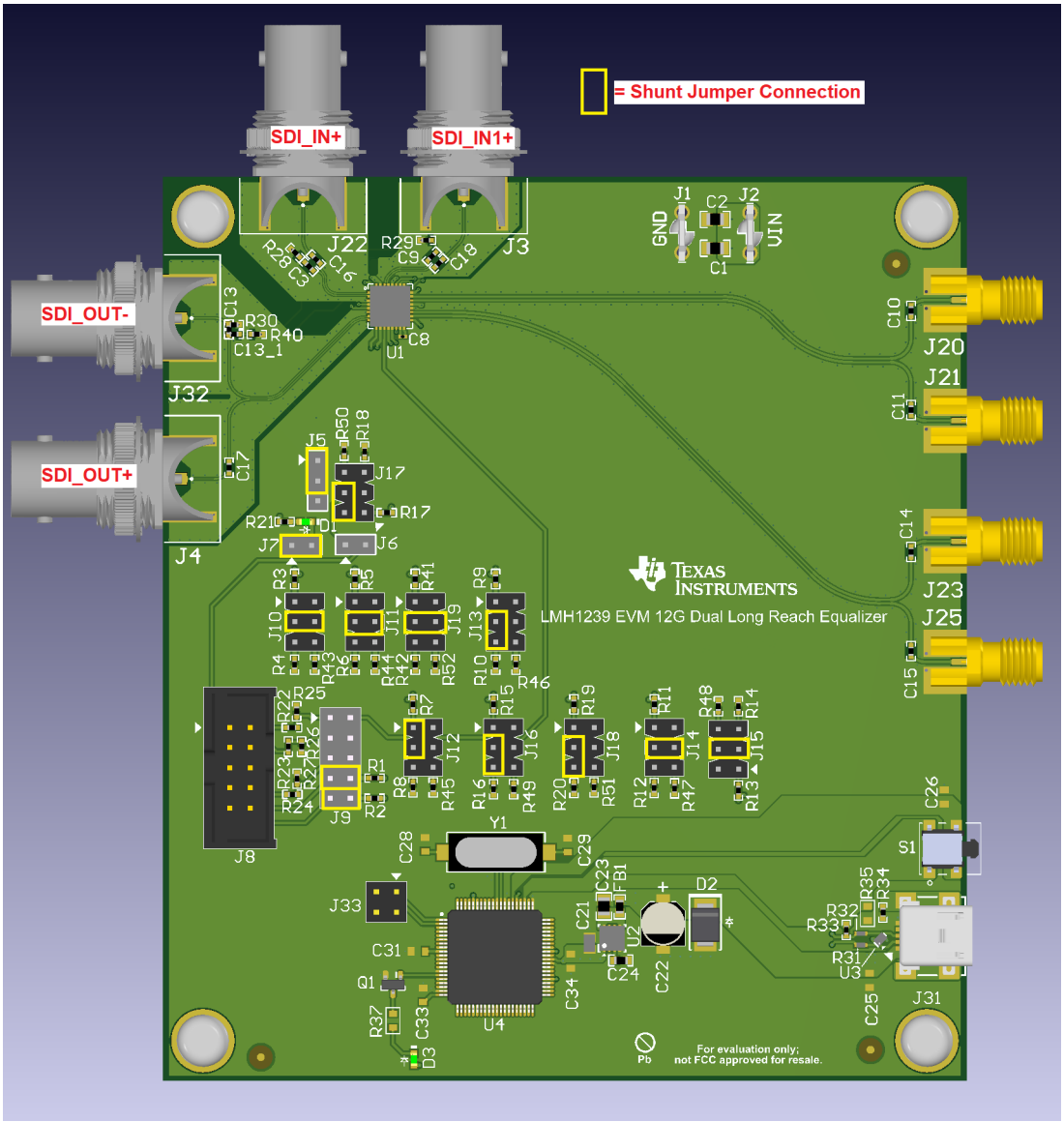

Figure 2-3. LMH1239EVM SDI_OUT Enabled for SMBus Operation

2.1.2.1 SDI_IN1 Selected

1. Connect the LMH1239EVM to the system under test.
   a. The input signal on J3 can be connected to a video signal generator over a 75Ω coax cable.
   b. The output signals on J20, J21, J23 and J25 can be connected with matched 100Ω differential cables to a high-speed scope to view the output eye diagram. Alternatively, this 100Ω output can be used as the source for another SDI cable driver.
   c. The output signal on J32 can be connected with 75Ω coax cable to a video pattern analyzer.

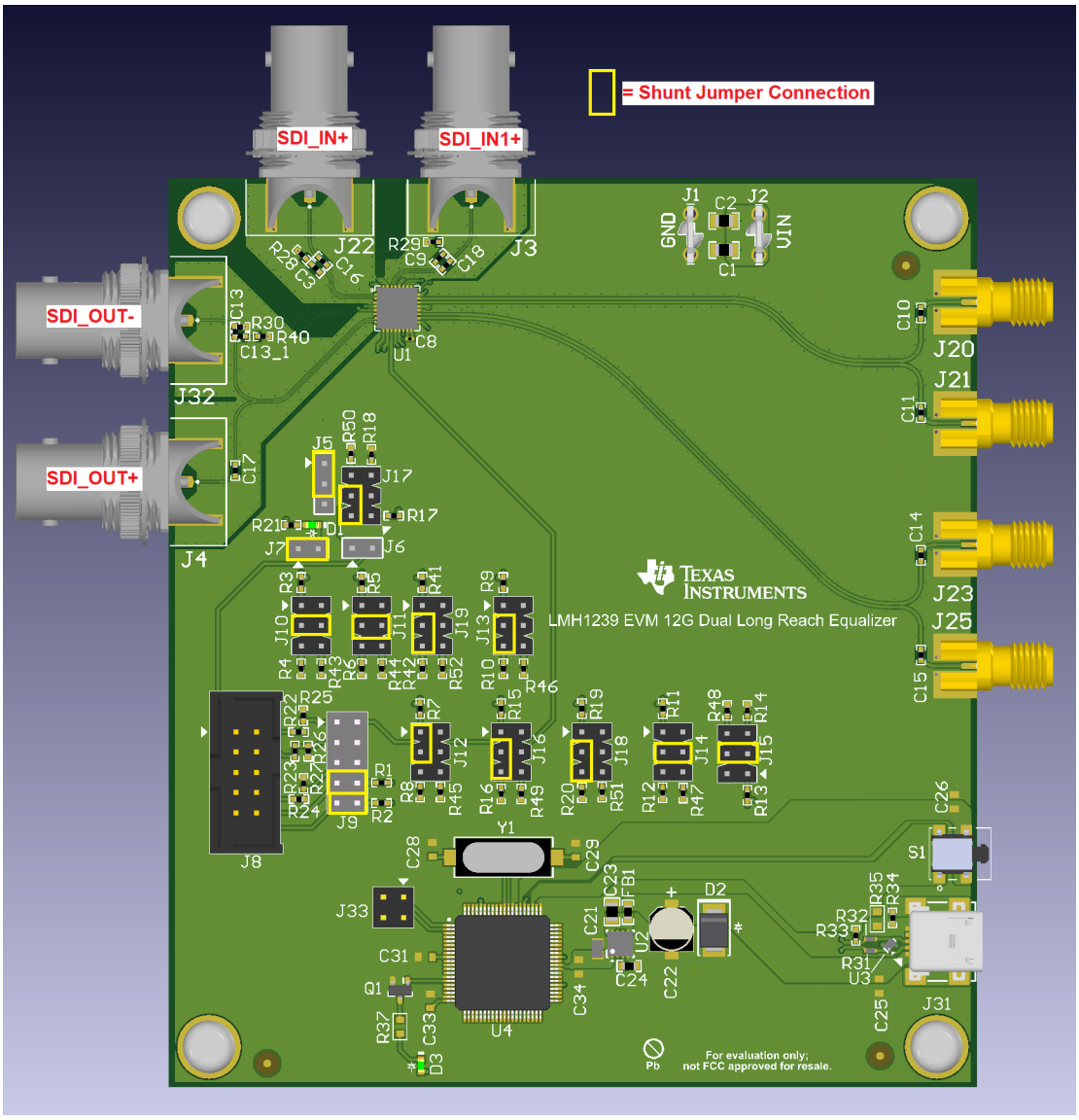

Figure 2-4. LMH1239EVM SDI_OUT and SDI_IN1 Enabled for SMBus Operation

2.1.2.2 SMBus/I²C Secondary Mode Configuration for the LMH1239EVM GUI

Users can select the device mode through the MODE_SEL pins on header J13. To select SMBus mode, ensure that the J13 header is set to L. When the device mode is configured, it is possible to set a unique SMBus address by adjusting the address headers J16 and J17 to various combinations of H, F, R, and L. When using multiple devices, each device must have a unique SMBus address to communicate along the same bus.

When the SMBus Address is configured, there are two options to connect the LMH1239EVM through the SMBus. The first option is through the pin header on J8. This is a typical configuration for the USB2ANY adapter. The second option is to connect to the LMH1239EVM with a USB-to-mini-USB cable through the mini-USB port located on J31.

Table 2-5. SMBus Address Configuration

J16-ADDR 0	J17-ADDR1	7 Bit SMBus Address	8-Bit SMBus Write Address
L	L	3D	7A
L	R	3E	7C
L	F	3F	7E
L	H	40	80
R	L	41	82
R	R	42	84
R	F	43	86
R	H	44	88
F	L	45	8A
F	R	46	8C
F	F	47	8E
F	H	48	90
H	L	49	92
H	R	4A	94
H	F	4B	96
H	H	4C	98

When there is a connection between the device and the PC, launch the LMH1239EVM GUI from the device page resources. The GUI is a multifunctional tool that includes low level and high level functionality with an eye monitoring tool and register map section. The following image is the home page of the GUI. Input the target address and click the Connect button to establish a connection to the device. If using a USB2ANY adapter, click the toggle LED button to illuminate the USB2ANY adapter module onboard LED. When the device is connected, use the side bar on the left to navigate to the other pages of the GUI.

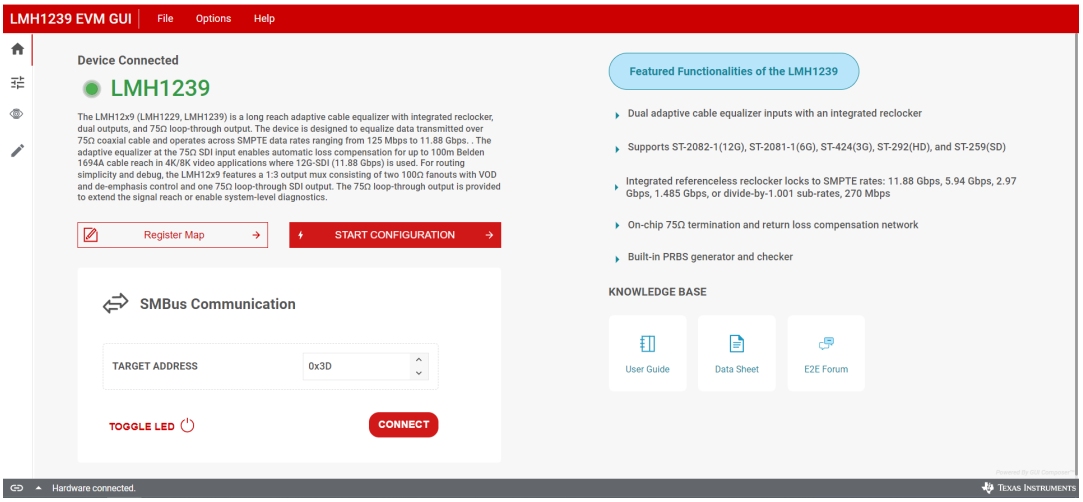

Figure 2-5. LMH1239EVM GUI With Device Connection (J16:L, J17:L)

2.1.2.3 High Level Page for the LMH1239EVM GUI

The *Configuration* page offers a high level view of the LMH1239EVM functionality. The many functionalites of the page include but are not limited to: selecting the starting and ending enable rates, overriding mux selection pin controls, VOD and de-emphasis control, and independent output control. The ending enable rate is the lowest date rate that the device can lock to and the starting enable rate is the highest. To lock to the updated range, click the relock CDR button.

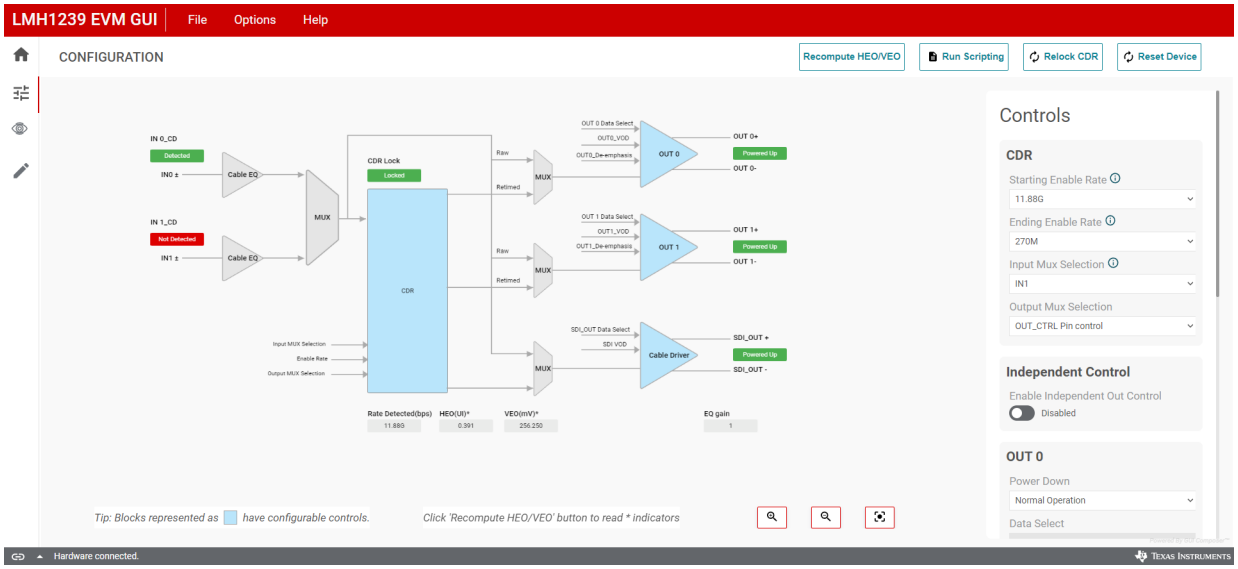

Figure 2-6. LMH1239EVM *Configuration* Page

2.1.2.4 Eye Monitor for the LMH1239EVM GUI

The *Eye Monitoring* page for the LMH1239EVM GUI allows the user to capture the output eye. The functionality of the page can be divided into three segments, namely, the status panel, the eye opening values and the capture/plot section. The status panel is a useful indicator of the input signal location and the CDR lock status. The eye opening values section includes the detected data rate, the HEO (horizontal eye opening) in UI and the VEO (vertical eye opening) in mV. Note that it is possible to recompute the HEO/VEO and any time, and that after each single eye capture, the HEO and VEO are recalculated. Finally, there is the capture/plot section which is used to start the eye capturing process. A *single capture* captures a single sample of the eye whereas the *continuous capture* samples and plots the eye continuously.

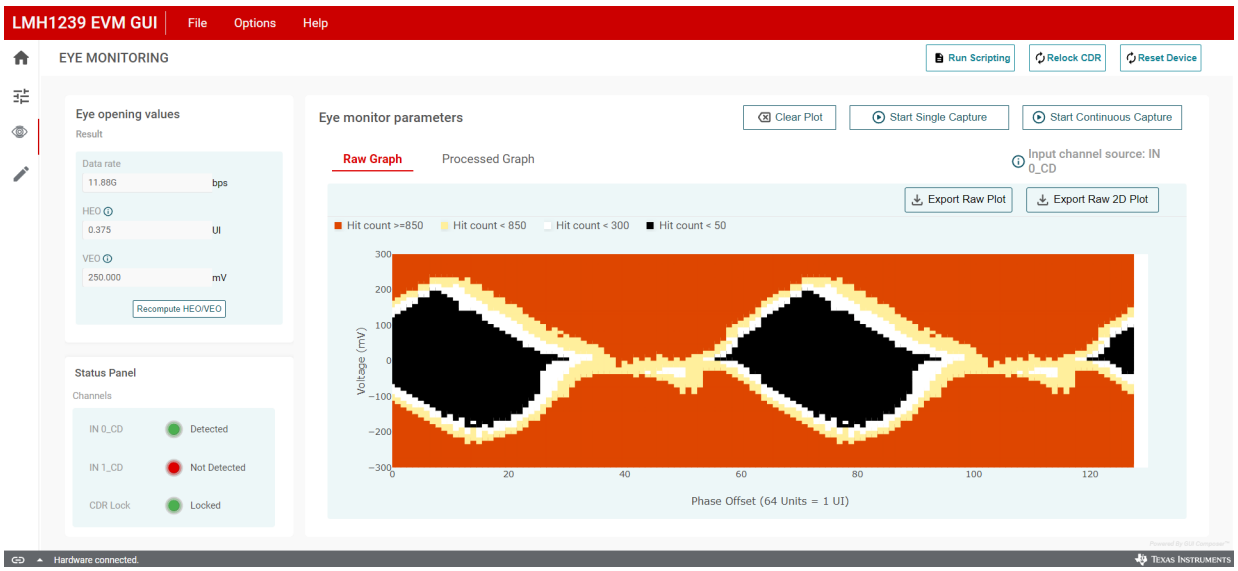

Figure 2-7. LMH1239EVM GUI *Eye Monitoring* Page

2.1.2.4.1 Register Map for the LMH1239EVM GUI

The *Register Map* page for the LMH1239EVM GUI is useful for register level programming. When auto read is enabled, the registers for the selected register page are re-read based on the auto-read delay. Users can write register commands in immediate mode and deferred mode. If deferred mode is selected, the register writes do not occur until the user presses the *Write* button. When the write mode is immediate, registers can be written on a bit-by-bit level by double-clicking on the bit. For example, to select the CDR register page, double-click bit 2 of the first register in the share page 0xFF. Additionally, the registers support interaction from the *Field View*. The *Field View* drop-down menu and checkbox options are congruent to the register architecture to simplify device configuration.

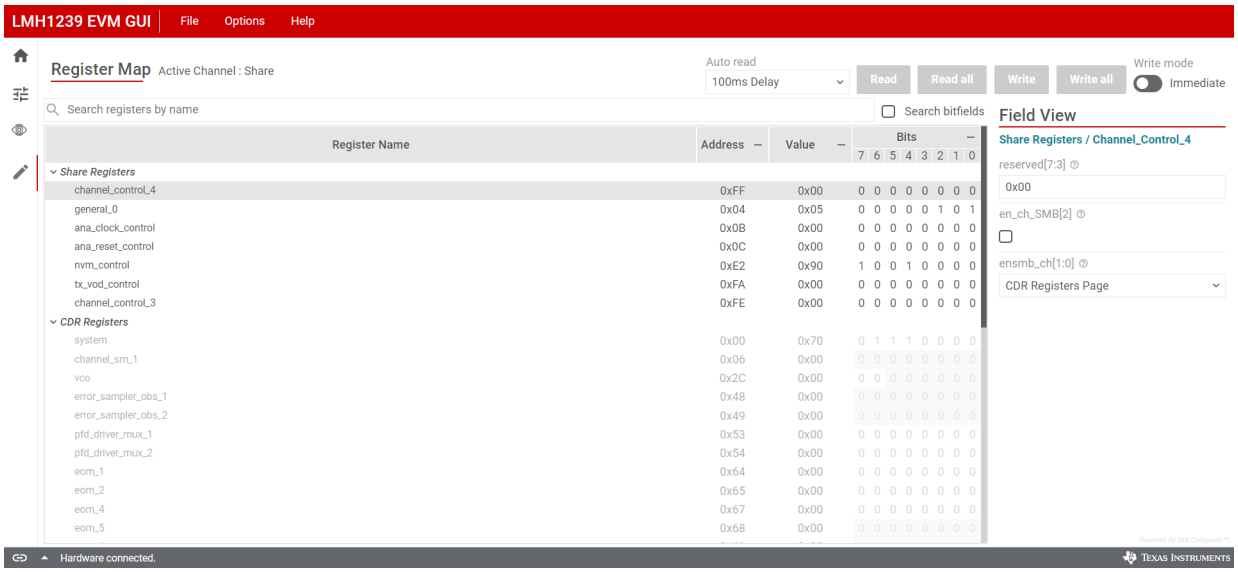

Figure 2-8. LMH1239EVM GUI *Register Map*

2.1.2.5 Scripting for the LMH1239EVM GUI

The LMH1239 GUI supports Javascript scripting with the EVM. Users can upload a script by pressing the *Upload Script File* button. Users can press the *Run* button to execute the script that is currently selected in the file input and press the *Stop* button to terminate the current script. The supported commands are *read, write,* and *log*. The user can only apply read and write commands to the registers present in the *Register Map* page. See the code block below for an example.

```
/** Texas Instruments Javascript sample script for reading registers, writing registers and
checking CDR lock.*/

const SCRIPT_START_MESSAGE = 'Script Started';
const SCRIPT_END_MESSAGE = 'Script Ended';

function main() {
/* Log to text file */
log(SCRIPT_START_MESSAGE);

/* Select the CDR Registers Page by writing to register 0xFF (channel_control4) */
write('channel_control_4', 0x04);

/* Defines a variable */
let CDRLockValue;

/* Read the CDR lock value register and log the value. If the CDR is locked the output will read
0x39 (57 in decimal).*/
CDRLockValue = read("channel_sm_1");
log("The CDR lock value register reads " + CDRLockValue + " in decimal");

/* Log to text file */
log(SCRIPT_END_MESSAGE)
}
```

3 Hardware Design Files

3.1 Schematics

Figure 3-1 shows the schematic for LMH1239EVM.

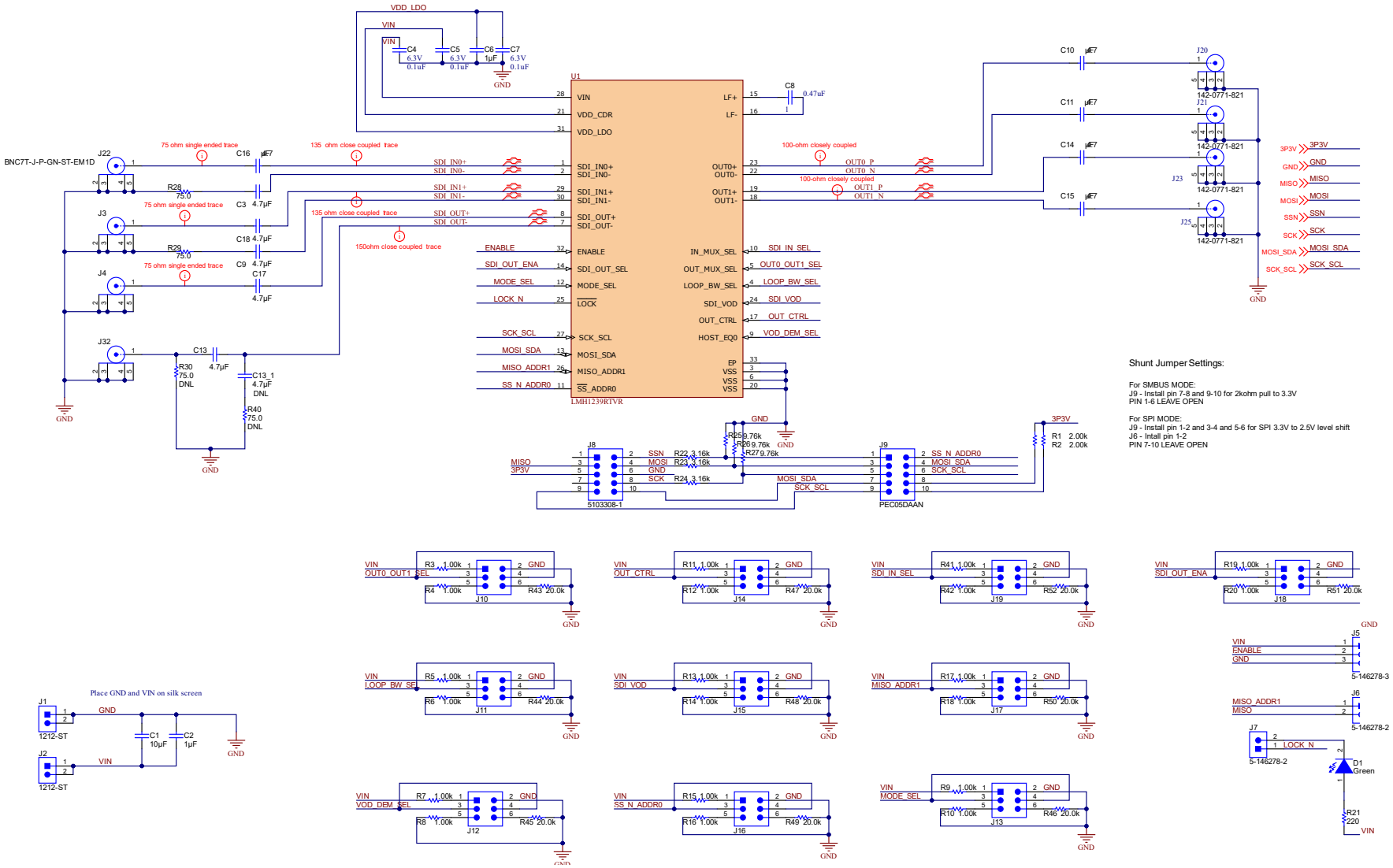

Figure 3-1. LMH1239EVM Schematic Page

3.2 PCB Layout

The following figures show the LMH1239EVM layout. The evaluation board controls signal integrity control settings through jumper pins.

The LMH1239EVM allows access to all input channels (SDI_IN and SDI_IN1) and output channels (OUT0, OUT1, and SDI_OUT).

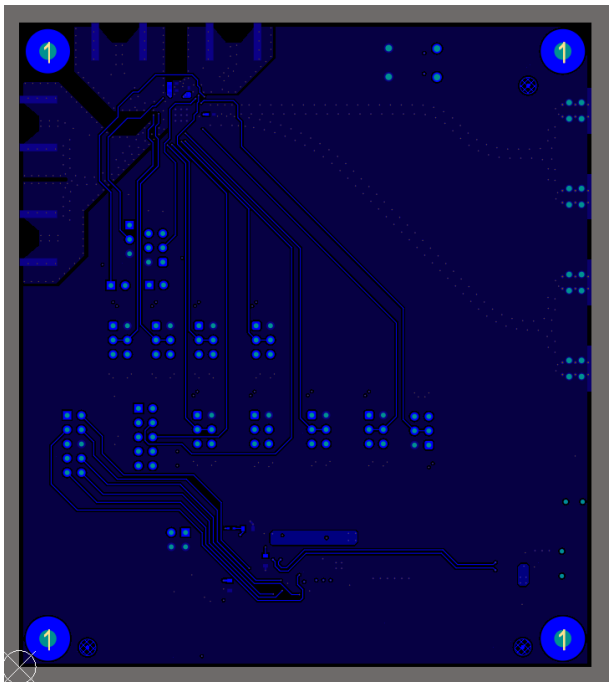

Figure 3-2. LMH1239EVM Bottom Layer

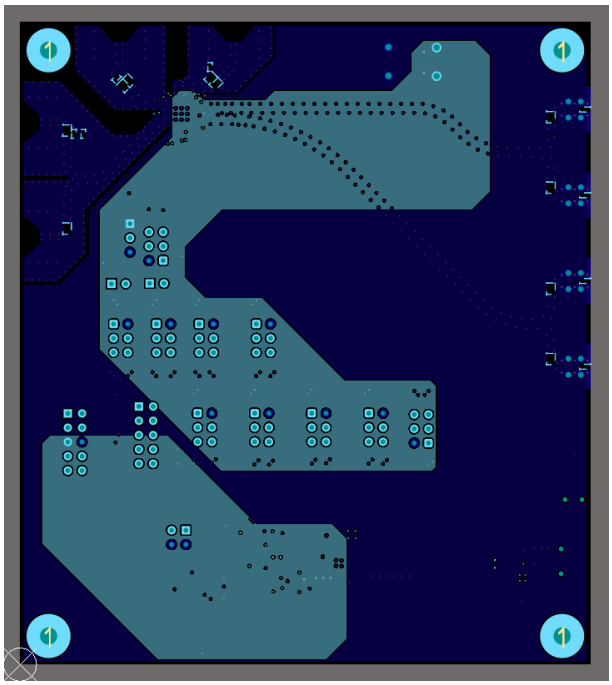

Figure 3-3. LMH1239EVM Layer 3 Power

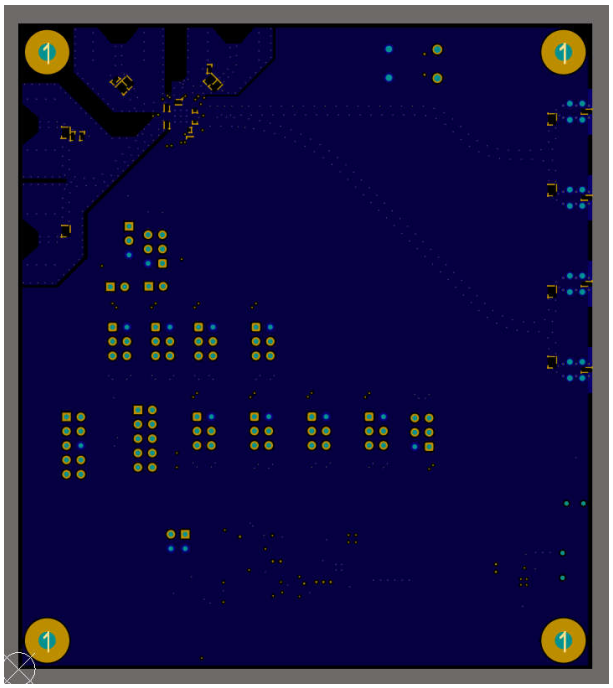

Figure 3-4. LMH1239EVM Layer 2 Ground

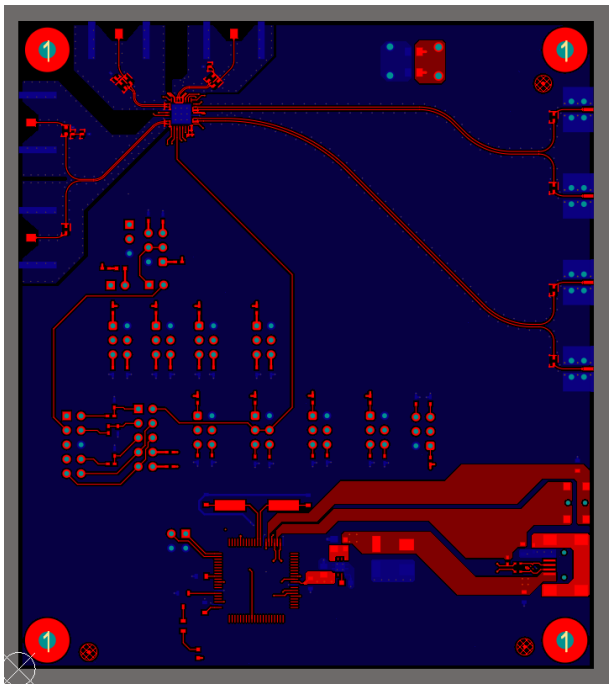

Figure 3-5. LMH1239EVM Top Layer

3.3 Bill of Materials (BOM)

Table 3-1. Bill of Materials (BOM)

Number	Designator	Quantity	Description	Manufacturer	Part Number
1	!PCb	1	Printed-Circuit Board	Any	HSDC150
2	C1	1	CAP, CERM, 10µF, 16V, +/-20%, X5R, 0805	AVX	0805YD106MAT2A
3	C2, C23	2	CAP, CERM, 1µF, 16V, +/-10%, X5R, 0805	AVX	0805YD105KAT2A
4	C3, C9, C10, C11, C13_1, C14, C15, C16, C17, C18	10	CAP, CERM, 4.7µF, 10V, +/-10%, X5R, 0402	TDK	C1005X5R1A475K050BC
5	C4, C5, C7	1	CAP, CERM, 0.1µF, 6.3V, +/-10%, X5R, 0402	TDK	C1005X5R0J104K050BA
6	C6	1	CAP, CERM, 1µF, 6.3V, +/-20%, X5R, 0402	Kemet	C0402C105M9PAC
7	C8(Unfitted), C33	2	CAP, CERM, 0.47µF, 16V, +/-10%, X7R, 1206	Taiyo Yuden	EMK063BBJ474KPLF
8	C21	1	CAP, CERM, 2.2µF, 16V, +/-10%, X5R, 0805	AVX	0805YD225KAT2A
9	C22	1	CAP, AL, 22µF, 10V, +/- 20%, ohm, SMD	Nichicon	UWZ1A220MCL1GB
10	C23	1	CAP, CERM, 1µF, 16V, +/-10%, X5R, 0805	AVX	0805YD105KAT2A
11	C24	1	CAP, CERM, 0.01µF, 50V, +/-10%, X7R, 0603	TDK	C1608X7R1H103K080AA
12	C25, C31, C32, C34	4	CAP, CERM, 0.1µF, 16V, +/-5%, X7R, 0603	AVX	0603YC104JAT2A
13	C26, C27	2	CAP, CERM, 220pF, 50V, +/-1%, C0G/NP0, 0603	AVX	06035A221FAT2A
14	C28, C29	2	CAP, CERM, 30pF, 100V, +/-5%, C0G/NP0, 0603	MuRata	GRM1885C2A300JA01D
15	C30	1	CAP, CERM, 2200pF, 50V, +/-10%, X7R, 0603	Kemet	C0603X222K5RACTU
16	D1,D3	2	LED, Green, SMD	Lumex	SML-LX0603GW-TR

Table 3-1. Bill of Materials (BOM) (continued)

Number	Designator	Quantity	Description	Manufacturer	Part Number
17	D2	1	Diode, Zener, 7.5V, 550mW, SMB	ON Semiconductor	SML-LX0603GW-TR
18	FB1	1	FERRITE BEAD 60 OHM 0603 1LN	Laird-Signal Integrity Products	MI0603J600R-10
19	FID1, FID2, FID3, FID4, FID5, FID6	6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
20	H1, H2, H3, H4	4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH
21	H5, H6, H7, H8	4	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	NY PMS 440 0025 PH
22	J1, J2	2	Disconnect Terminal, 5.08mm, 2x1, Tin, TH	Keystone	1212-ST
23	J3, J4	2	Connector, BNC Edge Mount, SMD	Samtec	BNC7T-J-P-GN-ST-EM1D
24	J5, J6, J7	3	Header, 100mil, 3x1, Tin, TH	TE Connectivity	5-146278-3
25	J8	1	Header (shrouded), 100mil, 5x2, Gold, TH	TE Connectivity	5103308-1
26	J9	1	Header, 100mil, 5x2, Tin, TH	Sullins Connector Solutions	PEC05DAAN
27	J10, J11, J12, J13, J14, J15, J16, J17, J18, J19	10	Header, 100mil, 3x2, Tin, TH	TE Connectivity	5-146254-3
28	J20, J21	2	Connector, End launch SMA 50 ohm, TH	Cinch Connectivity	142-0771-821
29	J22	1	Connector, BNC Edge Mount, SMD	Samtec	BNC7T-J-P-GN-ST-EM1D
30	J23, J25	2	Connector, End launch SMA 50 ohm, TH	Cinch Connectivity	142-0771-821
31	J31	1	Connector, Receptacle, Mini-USB Type B, R/A, Top Mount SMT	TE Connectivity	1734035-2
32	J33	1	Header, 100mil, 2x2, Gold, TH	Samtec	TSW-102-07-G-D
33	Q1	1	MOSFET, N-CH, 50V, 0.22A, SOT-23	Fairchild Semiconductor	BSS138

Table 3-1. Bill of Materials (BOM) (continued)

Number	Designator	Quantity	Description	Manufacturer	Part Number
34	R1, R2	2	RES, 2.00k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04022K00FKED
35	R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R41, R42	20	RES, 1.00k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04021K00FKED
36	R21	1	RES, 220 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW0402220RJNED
37	R22, R23, R24	3	RES, 3.16k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04023K16FKED
38	R25, R26, R27	3	RES, 9.76k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04029K76FKED
39	R28, R29, R30, R40	4	RES SMD 75 OHM 1% 1/5W 0402	Panasonic Electronic Components	ERJ-PA2F75R0X
40	R31, R32	2	RES, 33 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW040233R0JNED
41	R33	1	RES, 1.5 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021K50JNED
42	R34	1	RES, 33k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW040233K0JNED
43	R35	1	RES, 1.2Meg ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031M20JNEA
44	R36	1	RES, 33k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW040233K0JNED
45	R37	1	RES, 200 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603200RFKEA
46	R41, R42	2	RES, 1.00k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04021K00FKED
47	R43, R44, R45, R46, R47, R48, R49, R50, R51, R52	10	RES, 20.0k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040220K0FKED
48	S1	1	Switch, Tactile, SPST-NO, SMT	E-Switch	TL3901AGQF180

Table 3-1. Bill of Materials (BOM) (continued)

Number	Designator	Quantity	Description	Manufacturer	Part Number
49	SH-J2, SH-J3, SHJ4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SHJ11, SH-J12, SH-J13, SH-J14, SH-J15	14	Shunt, 100mil, Gold plated, Black	Sullins Connector Solutions	QPC02SXGN-RC
50	U1	1	12G UHD-SDI Long Reach Adaptive Cable Equalizer with Integrated Reclocker Product Requirement Specifications (PRS), WQFN32	Texas Instruments	LMH1239RTVR
51	U2	1	500mA, Low Quiescent Current, Ultra-Low Noise, High PSRR Low-Dropout Linear Regulator, DRB0008A	Texas Instruments	TPS73533DRBR
52	U3	1	ESD-Protection Array for High-Speed Data Interfaces, 4 Channels, -40 to +85 degC, 6-pin SON (DRY), Green (RoHS & no Sb/Br)	Texas Instruments	TPD4E004DRYR
53	U4	1	25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	Texas Instruments	MSP430F5529IPN
54	Y1	1	Crystal, 24.000MHz, 20pF, SMD	ECS Inc.	ECS-240-20-5PX-TR

4 Additional Information

4.1 Trademarks

All trademarks are the property of their respective owners.

5 Related Documentation

- Texas Instruments, *LMH12x9 12G UHD Long Reach Cable Equalizer with Integrated Reclocker* data sheet

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2024) to Revision A (September 2024)	Page
• Added Bill of Materials, Specification, and all sections for the GUI	1
• Updated schematic image and improved quality on PCB images	13

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265