User's Guide

LMK5C33414A Programmer's Guide

Abstract

This programming guide lists the device registers of the LMK5C33414A.

Trademarks

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1 Device Registers

Table 1-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 1-1 should be considered as reserved locations and the register contents should not be modified.

Table 1-1. DEVICE Registers

<table>
<tr><th>Offset</th><th>Acronym</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td>0x0</td><td>R0</td><td colspan="8">VNDRID_15:8</td></tr>
<tr><td>0x1</td><td>R1</td><td colspan="8">VNDRID</td></tr>
<tr><td>0x2</td><td>R2</td><td colspan="8">PRODID</td></tr>
<tr><td>0x3</td><td>R3</td><td colspan="8">REVID</td></tr>
<tr><td>0x4</td><td>R4</td><td colspan="8">PRTID_47:40</td></tr>
<tr><td>0x5</td><td>R5</td><td colspan="8">PRTID_39:32</td></tr>
<tr><td>0x6</td><td>R6</td><td colspan="8">PRTID_31:24</td></tr>
<tr><td>0x7</td><td>R7</td><td colspan="8">PRTID_23:16</td></tr>
<tr><td>0x8</td><td>R8</td><td colspan="8">PRTID_15:8</td></tr>
<tr><td>0x9</td><td>R9</td><td colspan="8">PRTID</td></tr>
<tr><td>0x10</td><td>R16</td><td colspan="8">NVMCNT</td></tr>
<tr><td>0x12</td><td>R18</td><td colspan="3">RESERVED</td><td colspan="5">TARGET_ADR_MSB</td></tr>
<tr><td>0x13</td><td>R19</td><td colspan="8">EEREV</td></tr>
<tr><td>0x14</td><td>R20</td><td>ROM_PLUS_EE</td><td colspan="4">EE_ROM_PAGE_SEL</td><td colspan="3">RESERVED</td></tr>
<tr><td>0x15</td><td>R21</td><td>SPI_3WIRE_DIS</td><td>SYNC_SW</td><td colspan="6">RESERVED</td></tr>
<tr><td>0x16</td><td>R22</td><td colspan="2">RESERVED</td><td>DPLL3_EN</td><td>APLL3_EN</td><td>DPLL2_EN</td><td>APLL2_EN</td><td>DPLL1_EN</td><td>APLL1_EN</td></tr>
<tr><td>0x17</td><td>R23</td><td>RESERVED</td><td>SWRST</td><td>DPLL3_SWRST</td><td>DPLL2_SWRST</td><td>DPLL1_SWRST</td><td>APLL3_SWRST</td><td>APLL2_SWRST</td><td>APLL1_SWRST</td></tr>
<tr><td>0x18</td><td>R24</td><td colspan="2">RESERVED</td><td colspan="2">APLL3_STRT_PRTY</td><td colspan="2">APLL2_STRT_PRTY</td><td colspan="2">APLL1_STRT_PRTY</td></tr>
<tr><td>0x19</td><td>R25</td><td colspan="7">RESERVED</td><td>SYNC_EN</td></tr>
<tr><td>0x1A</td><td>R26</td><td colspan="2">RESERVED</td><td colspan="2">SYSREF_REQ_MODE</td><td colspan="3">SYSREF_REQ_SEL</td><td>SYSREF_REQ_SW</td></tr>
<tr><td>0x1B</td><td>R27</td><td colspan="8">TEC_CNTR_39:32</td></tr>
<tr><td>0x1C</td><td>R28</td><td colspan="8">TEC_CNTR_31:24</td></tr>
<tr><td>0x1D</td><td>R29</td><td colspan="8">TEC_CNTR_23:16</td></tr>
<tr><td>0x1E</td><td>R30</td><td colspan="8">TEC_CNTR_15:8</td></tr>
<tr><td>0x1F</td><td>R31</td><td colspan="8">TEC_CNTR</td></tr>
<tr><td>0x20</td><td>R32</td><td colspan="6">RESERVED</td><td>TEC_CNTR_TRIG_SEL</td><td>TEC_CNTR_EN</td></tr>
<tr><td>0x21</td><td>R33</td><td colspan="4">RESERVED</td><td>LOL_PLL1</td><td>LOL_PLL2</td><td>RESERVED</td><td>LOS_FDET_XO</td></tr>
<tr><td>0x22</td><td>R34</td><td>LOPL_DPLL1</td><td>LOFL_DPLL1</td><td>RESERVED</td><td>HLDOVR1</td><td colspan="4">RESERVED</td></tr>
</table>

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x23	R35	LOPL_DPLL2	LOFL_DPLL2	RESERVED	HLDOVR2	RESERVED			
0x24	R36	LOPL_DPLL3	LOFL_DPLL3	RESERVED	HLDOVR3	RESERVED			
0x25	R37	RESERVED				LOL_PLL1_MASK	LOL_PLL2_MASK	RESERVED	LOS_FDET_XO_MASK
0x26	R38	LOPL_DPLL1_MASK	LOFL_DPLL1_MASK	HIST1_MASK	HLDOVR1_MASK	REFSWITCH1_MASK	LOR_MISSCLK1_MASK	LOR_FREQ1_MASK	LOR_PH1_MASK
0x27	R39	LOPL_DPLL2_MASK	LOFL_DPLL2_MASK	HIST2_MASK	HLDOVR2_MASK	REFSWITCH2_MASK	LOR_MISSCLK2_MASK	LOR_FREQ2_MASK	LOR_PH2_MASK
0x28	R40	LOPL_DPLL3_MASK	LOFL_DPLL3_MASK	HIST3_MASK	HLDOVR3_MASK	REFSWITCH3_MASK	LOR_MISSCLK3_MASK	LOR_FREQ3_MASK	LOR_PH3_MASK
0x29	R41	RESERVED				LOL_PLL1_POL	LOL_PLL2_POL	RESERVED	LOS_FDET_XO_POL
0x2A	R42	LOPL_DPLL1_POL	LOFL_DPLL1_POL	HIST1_POL	HLDOVR1_POL	REFSWITCH1_POL	LOR_MISSCLK1_POL	LOR_FREQ1_POL	LOR_PH1_POL
0x2B	R43	LOPL_DPLL2_POL	LOFL_DPLL2_POL	HIST2_POL	HLDOVR2_POL	REFSWITCH2_POL	LOR_MISSCLK2_POL	LOR_FREQ2_POL	LOR_PH2_POL
0x2C	R44	LOPL_DPLL3_POL	LOFL_DPLL3_POL	HIST3_POL	HLDOVR3_POL	REFSWITCH3_POL	LOR_MISSCLK3_POL	LOR_FREQ3_POL	LOR_PH3_POL
0x2D	R45	RESERVED				LOL_PLL1_INTR	LOL_PLL2_INTR	RESERVED	LOS_FDET_XO_INTR
0x2E	R46	LOPL_DPLL1_INTR	LOFL_DPLL1_INTR	HIST1_INTR	HLDOVR1_INTR	REFSWITCH1_INTR	LOR_MISSCLK1_INTR	LOR_FREQ1_INTR	LOR_PH1_INTR
0x2F	R47	LOPL_DPLL2_INTR	LOFL_DPLL2_INTR	HIST2_INTR	HLDOVR2_INTR	REFSWITCH2_INTR	LOR_MISSCLK2_INTR	LOR_FREQ2_INTR	LOR_PH2_INTR
0x30	R48	LOPL_DPLL3_INTR	LOFL_DPLL3_INTR	HIST3_INTR	HLDOVR3_INTR	REFSWITCH3_INTR	LOR_MISSCLK3_INTR	LOR_FREQ3_INTR	LOR_PH3_INTR
0x31	R49	RESERVED				INT_LATCH_OR_LIVE	INT_AND_OR	INT_EN	INT_CLR
0x32	R50	RESERVED				REF3_VALID_STATUS	REF2_VALID_STATUS	REF1_VALID_STATUS	REF0_VALID_STATUS
0x33	R51	RESERVED		REF3_PH_STATUS	RESERVED	REF3_FDET_STATUS	REF2_PH_STATUS	RESERVED	REF2_FDET_STATUS
0x34	R52	RESERVED		REF1_PH_STATUS	RESERVED	REF1_FDET_STATUS	REF0_PH_STATUS	RESERVED	REF0_FDET_STATUS
0x35	R53	RESERVED			TEC_CNTR_HELD	RESERVED			
0x36	R54	RESERVED	GPIO0_IN_FLT_EN	GPIO0_MODE					
0x37	R55	RESERVED	GPIO1_IN_FLT_EN	GPIO1_MODE					

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x38	R56	RESERVED	GPIO2_IN_FLT_EN	GPIO2_MODE					
0x39	R57	RESERVED	GPIO0_SEL						
0x3A	R58	RESERVED	GPIO1_SEL						
0x3B	R59	RESERVED	GPIO2_SEL						
0x3C	R60	RESERVED		GPIO0_OPEND	GPIO1_OPEND	GPIO2_OPEND	GPIO0_POL	GPIO1_POL	GPIO2_POL
0x3D	R61	RESERVED			GPIO_SYSREF_SEL			MUTE_DPLL3_PHLOCK	MUTE_DPLL3_FRLOCK
0x3E	R62	RESERVED		MUTE_DPLL2_PHLOCK	MUTE_DPLL2_FRLOCK	MUTE_APLL2_LOCK	MUTE_DPLL1_PHLOCK	MUTE_DPLL1_FRLOCK	MUTE_APLL1_LOCK
0x3F	R63	RESERVED			XO_FDET_BYP	XO_ITYPE			
0x40	R64	RESERVED			XO_OUT_BUF_EN				
0x41	R65	RESERVED		REF3_ITYPE					
0x42	R66	RESERVED		REF2_ITYPE					
0x43	R67	RESERVED		REF1_ITYPE					
0x44	R68	RESERVED		REF0_ITYPE					
0x46	R70	RESERVED							STATUS_MUX_DIV2_EN
0x4B	R75	RESERVED	TDC3_ZDM_BYPASS_FB_DIV	TDC3_ZDM_FB_PRE_BYP	TDC3_IN_SEL		TDC3_IN_DRV_SEL		
0x4C	R76	RESERVED	TDC2_ZDM_BYPASS_FB_DIV	TDC2_ZDM_FB_PRE_BYP	TDC2_IN_SEL		TDC2_IN_DRV_SEL		
0x4D	R77	RESERVED	TDC1_ZDM_BYPASS_FB_DIV	TDC1_ZDM_FB_PRE_BYP	TDC1_IN_SEL		TDC1_IN_DRV_SEL		
0x4E	R78	RESERVED		REF_OUT01_EN	REF_OUT01_SEL				
0x4F	R79	RESERVED		REF0_EARLY_DET_EN	REF0_PH_VALID_EN	REF0_VALTMR_EN	REF0_PPM_EN	REF0_MISSCLK_EN	RESERVED
0x50	R80	RESERVED		REF1_EARLY_DET_EN	REF1_PH_VALID_EN	REF1_VALTMR_EN	REF1_PPM_EN	REF1_MISSCLK_EN	RESERVED
0x51	R81	RESERVED		REF2_EARLY_DET_EN	REF2_PH_VALID_EN	REF2_VALTMR_EN	REF2_PPM_EN	REF2_MISSCLK_EN	RESERVED
0x52	R82	RESERVED		REF3_EARLY_DET_EN	REF3_PH_VALID_EN	REF3_VALTMR_EN	REF3_PPM_EN	REF3_MISSCLK_EN	RESERVED
0x53	R83	REF3_DET_CLK_DIV		REF2_DET_CLK_DIV		REF1_DET_CLK_DIV		REF0_DET_CLK_DIV	
0x54	R84	RESERVED		REF0_MISSCLK_DIV_21:16					
0x55	R85	REF0_MISSCLK_DIV_15:8							
0x56	R86	REF0_MISSCLK_DIV							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x57	R87	RESERVED		REF1_MISSCLK_DIV_21:16					
0x58	R88	REF1_MISSCLK_DIV_15:8							
0x59	R89	REF1_MISSCLK_DIV							
0x5A	R90	RESERVED		REF2_MISSCLK_DIV_21:16					
0x5B	R91	REF2_MISSCLK_DIV_15:8							
0x5C	R92	REF2_MISSCLK_DIV							
0x5D	R93	RESERVED		REF3_MISSCLK_DIV_21:16					
0x5E	R94	REF3_MISSCLK_DIV_15:8							
0x5F	R95	REF3_MISSCLK_DIV							
0x60	R96	RESERVED							REF0_MISSCLK_VCOSEL
0x61	R97	RESERVED		REF0_EARLY_CLK_DIV_21:16					
0x62	R98	REF0_EARLY_CLK_DIV_15:8							
0x63	R99	REF0_EARLY_CLK_DIV							
0x64	R100	RESERVED		REF1_EARLY_CLK_DIV_21:16					
0x65	R101	REF1_EARLY_CLK_DIV_15:8							
0x66	R102	REF1_EARLY_CLK_DIV							
0x67	R103	RESERVED		REF2_EARLY_CLK_DIV_21:16					
0x68	R104	REF2_EARLY_CLK_DIV_15:8							
0x69	R105	REF2_EARLY_CLK_DIV							
0x6A	R106	RESERVED		REF3_EARLY_CLK_DIV_21:16					
0x6B	R107	REF3_EARLY_CLK_DIV_15:8							
0x6C	R108	REF3_EARLY_CLK_DIV							
0x6D	R109	RESERVED	REF0_PPM_MIN_14:8						
0x6E	R110	REF0_PPM_MIN							
0x6F	R111	RESERVED	REF0_PPM_MAX_14:8						
0x70	R112	REF0_PPM_MAX							
0x71	R113	RESERVED	REF1_PPM_MIN_14:8						
0x72	R114	REF1_PPM_MIN							
0x73	R115	RESERVED	REF1_PPM_MAX_14:8						
0x74	R116	REF1_PPM_MAX							
0x75	R117	RESERVED	REF2_PPM_MIN_14:8						
0x76	R118	REF2_PPM_MIN							
0x77	R119	RESERVED	REF2_PPM_MAX_14:8						

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x78	R120	REF2_PPM_MAX							
0x79	R121	RESERVED	REF3_PPM_MIN_14:8						
0x7A	R122	REF3_PPM_MIN							
0x7B	R123	RESERVED	REF3_PPM_MAX_14:8						
0x7C	R124	REF3_PPM_MAX							
0x7D	R125	RESERVED				REF0_CNTSTRT_27:24			
0x7E	R126	REF0_CNTSTRT_23:16							
0x7F	R127	REF0_CNTSTRT_15:8							
0x80	R128	REF0_CNTSTRT							
0x81	R129	RESERVED				REF0_HOLD_CNTSTRT_27:24			
0x82	R130	REF0_HOLD_CNTSTRT_23:16							
0x83	R131	REF0_HOLD_CNTSTRT_15:8							
0x84	R132	REF0_HOLD_CNTSTRT							
0x85	R133	RESERVED				REF1_CNTSTRT_27:24			
0x86	R134	REF1_CNTSTRT_23:16							
0x87	R135	REF1_CNTSTRT_15:8							
0x88	R136	REF1_CNTSTRT							
0x89	R137	RESERVED				REF1_HOLD_CNTSTRT_27:24			
0x8A	R138	REF1_HOLD_CNTSTRT_23:16							
0x8B	R139	REF1_HOLD_CNTSTRT_15:8							
0x8C	R140	REF1_HOLD_CNTSTRT							
0x8D	R141	RESERVED	REF2_PH_VALID_CNT_MSB			REF2_CNTSTRT_27:24			
0x8E	R142	REF2_CNTSTRT_23:16							
0x8F	R143	REF2_CNTSTRT_15:8							
0x90	R144	REF2_CNTSTRT							
0x91	R145	RESERVED				REF2_HOLD_CNTSTRT_27:24			
0x92	R146	REF2_HOLD_CNTSTRT_23:16							
0x93	R147	REF2_HOLD_CNTSTRT_15:8							
0x94	R148	REF2_HOLD_CNTSTRT							
0x95	R149	RESERVED	REF3_PH_VALID_CNT_MSB			REF3_CNTSTRT_27:24			
0x96	R150	REF3_CNTSTRT_23:16							
0x97	R151	REF3_CNTSTRT_15:8							
0x98	R152	REF3_CNTSTRT							
0x99	R153	RESERVED				REF3_HOLD_CNTSTRT_27:24			

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x9A	R154	REF3_HOLD_CNTSTRT_23:16							
0x9B	R155	REF3_HOLD_CNTSTRT_15:8							
0x9C	R156	REF3_HOLD_CNTSTRT							
0x9D	R157	RESERVED			REF0VLDTMR				
0x9E	R158	RESERVED			REF1VLDTMR				
0x9F	R159	RESERVED			REF2VLDTMR				
0xA0	R160	RESERVED			REF3VLDTMR				
0xA1	R161	RESERVED		REF0_PH_VALID_THR_13:8					
0xA2	R162	REF0_PH_VALID_THR							
0xA3	R163	RESERVED		REF1_PH_VALID_THR_13:8					
0xA4	R164	REF1_PH_VALID_THR							
0xA5	R165	RESERVED		REF2_PH_VALID_THR_13:8					
0xA6	R166	REF2_PH_VALID_THR							
0xA7	R167	RESERVED		REF3_PH_VALID_THR_13:8					
0xA8	R168	REF3_PH_VALID_THR							
0xAA	R170	NVMSCRC							
0xAB	R171	RESERVED	REGCOMMIT	NVMCRCERR	RESERVED		NVMBUSY	NVMERASE	NVMPROG
0xAC	R172	NVMLCRC							
0xAD	R173	RESERVED			MEMADR_12:8				
0xAE	R174	MEMADR							
0xAF	R175	NVMDAT							
0xB0	R176	RAMDAT							
0xB4	R180	NVMUNLK							
0xDF	R223	RESERVED		DPLL1_REF0_AUTO_PRTY			DPLL1_REF1_AUTO_PRTY		
0xE0	R224	RESERVED		DPLL1_REF2_AUTO_PRTY			DPLL1_REF3_AUTO_PRTY		
0xE1	R225	RESERVED		DPLL1_REF4_AUTO_PRTY			DPLL1_REF5_AUTO_PRTY		
0xE2	R226	RESERVED		DPLL1_MAN_REFSEL			DPLL1_MAN_SWITCH_PIN_MODE	DPLL1_SWITCH_MODE	
0xE3	R227	RESERVED		DPLL1_REFSEL_STAT					
0xE4	R228	DPLL1_LOCKDET_PPM_EN	DPLL1_LOCKDET_PPM_MAX_14:8						
0xE5	R229	DPLL1_LOCKDET_PPM_MAX							
0xE6	R230	RESERVED	DPLL1_UNLOCKDET_PPM_MAX_14:8						
0xE7	R231	DPLL1_UNLOCKDET_PPM_MAX							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xE8	R232	RESERVED		DPLL1_LOCKDET2_PPM_CNTSTRT_29:24					
0xE9	R233	DPLL1_LOCKDET2_PPM_CNTSTRT_23:16							
0xEA	R234	DPLL1_LOCKDET2_PPM_CNTSTRT_15:8							
0xEB	R235	DPLL1_LOCKDET2_PPM_CNTSTRT							
0xEC	R236	RESERVED		DPLL1_LOCKDET_PPM_CNTSTRT_29:24					
0xED	R237	DPLL1_LOCKDET_PPM_CNTSTRT_23:16							
0xEE	R238	DPLL1_LOCKDET_PPM_CNTSTRT_15:8							
0xEF	R239	DPLL1_LOCKDET_PPM_CNTSTRT							
0xF0	R240	RESERVED		DPLL1_LOCKDET_VCO_PPM_CNTSTRT_29:24					
0xF1	R241	DPLL1_LOCKDET_VCO_PPM_CNTSTRT_23:16							
0xF2	R242	DPLL1_LOCKDET_VCO_PPM_CNTSTRT_15:8							
0xF3	R243	DPLL1_LOCKDET_VCO_PPM_CNTSTRT							
0xF4	R244	RESERVED							DPLL1_STATUS_PPM_LOCK
0xF7	R247	DPLL1_LOOP_EN	DPLL1_PHASE_CANCEL_EN	DPLL1_FASTLOCK_ALWAYS	DPLL1_PHS1_EN	DPLL1_ZDM_EN	DPLL1_HIST_EN	DPLL1_PHASE_CANCEL_ALWAYS	RESERVED
0xF8	R248	DPLL1_HOLD_SLEW_LIM_EN	RESERVED				DPLL1_CLK_DIV_SRC_SEL	RESERVED	
0xFA	R250	RESERVED			DPLL1_PH_OFFSET_44:40				
0xFB	R251	DPLL1_PH_OFFSET_39:32							
0xFC	R252	DPLL1_PH_OFFSET_31:24							
0xFD	R253	DPLL1_PH_OFFSET_23:16							
0xFE	R254	DPLL1_PH_OFFSET_15:8							
0xFF	R255	DPLL1_PH_OFFSET							
0x100	R256	DPLL1_FREE_RUN_39:32							
0x101	R257	DPLL1_FREE_RUN_31:24							
0x102	R258	DPLL1_FREE_RUN_23:16							
0x103	R259	DPLL1_FREE_RUN_15:8							
0x104	R260	DPLL1_FREE_RUN							
0x105	R261	RESERVED	DPLL1_1PPS_MODE	DPLL1_1PPS_EN	RESERVED				
0x122	R290	RESERVED						DPLL1_LCK_TIMER_9:8	
0x123	R291	DPLL1_LCK_TIMER							
0x124	R292	RESERVED						DPLL1_HIST_TIMER_9:8	

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x125	R293	DPLL1_HIST_TIMER							
0x126	R294	RESERVED						DPLL1_HOLD_TIMER_9:8	
0x127	R295	DPLL1_HOLD_TIMER							
0x128	R296	RESERVED						DPLL1_PHS1_TIMER_9:8	
0x129	R297	DPLL1_PHS1_TIMER							
0x12E	R302	RESERVED				DPLL1_HIST_GAIN			
0x12F	R303	RESERVED		DPLL1_PL_THRESH					
0x130	R304	RESERVED		DPLL1_PL_UNLK_THRESH					
0x131	R305	RESERVED		DPLL1_PHS1_THRESH					
0x134	R308	RESERVED		DPLL1_HOLD_SLEW_STEP					
0x136	R310	RESERVED		DPLL1_STATUS_PL	RESERVED				
0x137	R311	RESERVED			DPLL1_DCO_SLEW_ACTIVE	RESERVED			
0x13A	R314	RESERVED							DPLL1_FB_DIV_32:32
0x13B	R315	DPLL1_FB_DIV_31:24							
0x13C	R316	DPLL1_FB_DIV_23:16							
0x13D	R317	DPLL1_FB_DIV_15:8							
0x13E	R318	DPLL1_FB_DIV							
0x13F	R319	DPLL1_FB_NUM_39:32							
0x140	R320	DPLL1_FB_NUM_31:24							
0x141	R321	DPLL1_FB_NUM_23:16							
0x142	R322	DPLL1_FB_NUM_15:8							
0x143	R323	DPLL1_FB_NUM							
0x144	R324	DPLL1_FB_DEN_39:32							
0x145	R325	DPLL1_FB_DEN_31:24							
0x146	R326	DPLL1_FB_DEN_23:16							
0x147	R327	DPLL1_FB_DEN_15:8							
0x148	R328	DPLL1_FB_DEN							
0x149	R329	RESERVED							DPLL1_FB2_DIV_32:32
0x14A	R330	DPLL1_FB2_DIV_31:24							
0x14B	R331	DPLL1_FB2_DIV_23:16							
0x14C	R332	DPLL1_FB2_DIV_15:8							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x14D	R333	DPLL1_FB2_DIV							
0x14E	R334	DPLL1_FB2_NUM_39:32							
0x14F	R335	DPLL1_FB2_NUM_31:24							
0x150	R336	DPLL1_FB2_NUM_23:16							
0x151	R337	DPLL1_FB2_NUM_15:8							
0x152	R338	DPLL1_FB2_NUM							
0x153	R339	DPLL1_FB2_DEN_39:32							
0x154	R340	DPLL1_FB2_DEN_31:24							
0x155	R341	DPLL1_FB2_DEN_23:16							
0x156	R342	DPLL1_FB2_DEN_15:8							
0x157	R343	DPLL1_FB2_DEN							
0x158	R344	RESERVED		DPLL1_REF5_FB_SEL	DPLL1_REF4_FB_SEL	DPLL1_REF3_FB_SEL	DPLL1_REF2_FB_SEL	DPLL1_REF1_FB_SEL	DPLL1_REF0_FB_SEL
0x159	R345	RESERVED					DPLL1_FB_MASH_ORDER		
0x15A	R346	RESERVED		DPLL1_FB_FDEV_37:32					
0x15B	R347	DPLL1_FB_FDEV_31:24							
0x15C	R348	DPLL1_FB_FDEV_23:16							
0x15D	R349	DPLL1_FB_FDEV_15:8							
0x15E	R350	DPLL1_FB_FDEV							
0x15F	R351	RESERVED							DPLL1_FB_FDEV_UPDATE
0x160	R352	RESERVED							DPLL1_FB_FDEV_EN
0x161	R353	DPLL1_FB_NUM_STAT_39:32							
0x162	R354	DPLL1_FB_NUM_STAT_31:24							
0x163	R355	DPLL1_FB_NUM_STAT_23:16							
0x164	R356	DPLL1_FB_NUM_STAT_15:8							
0x165	R357	DPLL1_FB_NUM_STAT							
0x166	R358	RESERVED				DPLL1_REF0_DBLR_EN	DPLL1_REF1_DBLR_EN	DPLL1_REF2_DBLR_EN	DPLL1_REF3_DBLR_EN
0x167	R359	DPLL1_REF0_RDIV_15:8							
0x168	R360	DPLL1_REF0_RDIV							
0x169	R361	DPLL1_REF1_RDIV_15:8							
0x16A	R362	DPLL1_REF1_RDIV							
0x16B	R363	DPLL1_REF2_RDIV_15:8							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x16C	R364	DPLL1_REF2_RDIV							
0x16D	R365	DPLL1_REF3_RDIV_15:8							
0x16E	R366	DPLL1_REF3_RDIV							
0x16F	R367	DPLL1_REF4_RDIV_15:8							
0x170	R368	DPLL1_REF4_RDIV							
0x171	R369	DPLL1_REF5_RDIV_15:8							
0x172	R370	DPLL1_REF5_RDIV							
0x175	R373	RESERVED		DPLL2_REF0_AUTO_PRTY			DPLL2_REF1_AUTO_PRTY		
0x176	R374	RESERVED		DPLL2_REF2_AUTO_PRTY			DPLL2_REF3_AUTO_PRTY		
0x177	R375	RESERVED		DPLL2_REF4_AUTO_PRTY			DPLL2_REF5_AUTO_PRTY		
0x178	R376	RESERVED		DPLL2_MAN_REFSEL			DPLL2_MAN_SWITCH_PIN_MODE	DPLL2_SWITCH_MODE	
0x179	R377	RESERVED		DPLL2_REFSEL_STAT					
0x17A	R378	DPLL2_LOCKDET_PPM_EN	DPLL2_LOCKDET_PPM_MAX_14:8						
0x17B	R379	DPLL2_LOCKDET_PPM_MAX							
0x17C	R380	RESERVED	DPLL2_UNLOCKDET_PPM_MAX_14:8						
0x17D	R381	DPLL2_UNLOCKDET_PPM_MAX							
0x17E	R382	RESERVED		DPLL2_LOCKDET2_PPM_CNTSTRT_29:24					
0x17F	R383	DPLL2_LOCKDET2_PPM_CNTSTRT_23:16							
0x180	R384	DPLL2_LOCKDET2_PPM_CNTSTRT_15:8							
0x181	R385	DPLL2_LOCKDET2_PPM_CNTSTRT							
0x182	R386	RESERVED		DPLL2_LOCKDET_PPM_CNTSTRT_29:24					
0x183	R387	DPLL2_LOCKDET_PPM_CNTSTRT_23:16							
0x184	R388	DPLL2_LOCKDET_PPM_CNTSTRT_15:8							
0x185	R389	DPLL2_LOCKDET_PPM_CNTSTRT							
0x186	R390	RESERVED		DPLL2_LOCKDET_VCO_PPM_CNTSTRT_29:24					
0x187	R391	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_23:16							
0x188	R392	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_15:8							
0x189	R393	DPLL2_LOCKDET_VCO_PPM_CNTSTRT							
0x18A	R394	RESERVED							DPLL2_STATUS_PPM_LOCK
0x18D	R397	DPLL2_LOOP_EN	DPLL2_PHASE_CANCEL_EN	DPLL2_FASTLOCK_ALWAYS	DPLL2_PHS1_EN	DPLL2_ZDM_EN	DPLL2_HIST_EN	DPLL2_PHASE_CANCEL_ALWAYS	RESERVED

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x18E	R398	DPLL2_HOLD_SLEW_LIM_EN	RESERVED						
0x190	R400	RESERVED			DPLL2_PH_OFFSET_44:40				
0x191	R401	DPLL2_PH_OFFSET_39:32							
0x192	R402	DPLL2_PH_OFFSET_31:24							
0x193	R403	DPLL2_PH_OFFSET_23:16							
0x194	R404	DPLL2_PH_OFFSET_15:8							
0x195	R405	DPLL2_PH_OFFSET							
0x196	R406	DPLL2_FREE_RUN_39:32							
0x197	R407	DPLL2_FREE_RUN_31:24							
0x198	R408	DPLL2_FREE_RUN_23:16							
0x199	R409	DPLL2_FREE_RUN_15:8							
0x19A	R410	DPLL2_FREE_RUN							
0x19B	R411	RESERVED	DPLL2_1PPS_MODE	DPLL2_1PPS_EN	RESERVED				
0x1B8	R440	RESERVED						DPLL2_LCK_TIMER_9:8	
0x1B9	R441	DPLL2_LCK_TIMER							
0x1BA	R442	RESERVED						DPLL2_HIST_TIMER_9:8	
0x1BB	R443	DPLL2_HIST_TIMER							
0x1BC	R444	RESERVED						DPLL2_HOLD_TIMER_9:8	
0x1BD	R445	DPLL2_HOLD_TIMER							
0x1BE	R446	RESERVED						DPLL2_PHS1_TIMER_9:8	
0x1BF	R447	DPLL2_PHS1_TIMER							
0x1C4	R452	RESERVED			DPLL2_HIST_GAIN				
0x1C5	R453	RESERVED		DPLL2_PL_THRESH					
0x1C6	R454	RESERVED		DPLL2_PL_UNLK_THRESH					
0x1C7	R455	RESERVED		DPLL2_PHS1_THRESH					
0x1CA	R458	RESERVED		DPLL2_HOLD_SLEW_STEP					
0x1CC	R460	RESERVED		DPLL2_STATUS_PL	RESERVED				
0x1CD	R461	RESERVED			DPLL2_DCO_SLEW_ACTIVE	RESERVED			
0x1D0	R464	RESERVED							DPLL2_FB_DIV_32:32
0x1D1	R465	DPLL2_FB_DIV_31:24							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1D2	R466	DPLL2_FB_DIV_23:16							
0x1D3	R467	DPLL2_FB_DIV_15:8							
0x1D4	R468	DPLL2_FB_DIV							
0x1D5	R469	DPLL2_FB_NUM_39:32							
0x1D6	R470	DPLL2_FB_NUM_31:24							
0x1D7	R471	DPLL2_FB_NUM_23:16							
0x1D8	R472	DPLL2_FB_NUM_15:8							
0x1D9	R473	DPLL2_FB_NUM							
0x1DA	R474	DPLL2_FB_DEN_39:32							
0x1DB	R475	DPLL2_FB_DEN_31:24							
0x1DC	R476	DPLL2_FB_DEN_23:16							
0x1DD	R477	DPLL2_FB_DEN_15:8							
0x1DE	R478	DPLL2_FB_DEN							
0x1DF	R479	RESERVED							DPLL2_FB2_DIV_32:32
0x1E0	R480	DPLL2_FB2_DIV_31:24							
0x1E1	R481	DPLL2_FB2_DIV_23:16							
0x1E2	R482	DPLL2_FB2_DIV_15:8							
0x1E3	R483	DPLL2_FB2_DIV							
0x1E4	R484	DPLL2_FB2_NUM_39:32							
0x1E5	R485	DPLL2_FB2_NUM_31:24							
0x1E6	R486	DPLL2_FB2_NUM_23:16							
0x1E7	R487	DPLL2_FB2_NUM_15:8							
0x1E8	R488	DPLL2_FB2_NUM							
0x1E9	R489	DPLL2_FB2_DEN_39:32							
0x1EA	R490	DPLL2_FB2_DEN_31:24							
0x1EB	R491	DPLL2_FB2_DEN_23:16							
0x1EC	R492	DPLL2_FB2_DEN_15:8							
0x1ED	R493	DPLL2_FB2_DEN							
0x1EE	R494	RESERVED		DPLL2_REF5_FB_SEL	DPLL2_REF4_FB_SEL	DPLL2_REF3_FB_SEL	DPLL2_REF2_FB_SEL	DPLL2_REF1_FB_SEL	DPLL2_REF0_FB_SEL
0x1EF	R495	RESERVED					DPLL2_FB_MASH_ORDER		
0x1F0	R496	RESERVED		DPLL2_FB_FDEV_37:32					
0x1F1	R497	DPLL2_FB_FDEV_31:24							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1F2	R498	DPLL2_FB_FDEV_23:16							
0x1F3	R499	DPLL2_FB_FDEV_15:8							
0x1F4	R500	DPLL2_FB_FDEV							
0x1F5	R501	RESERVED							DPLL2_FB_FDEV_UPDATE
0x1F6	R502	RESERVED							DPLL2_FB_FDEV_EN
0x1F7	R503	DPLL2_FB_NUM_STAT_39:32							
0x1F8	R504	DPLL2_FB_NUM_STAT_31:24							
0x1F9	R505	DPLL2_FB_NUM_STAT_23:16							
0x1FA	R506	DPLL2_FB_NUM_STAT_15:8							
0x1FB	R507	DPLL2_FB_NUM_STAT							
0x1FC	R508	RESERVED				DPLL2_REF0_DBLR_EN	DPLL2_REF1_DBLR_EN	DPLL2_REF2_DBLR_EN	DPLL2_REF3_DBLR_EN
0x1FD	R509	DPLL2_REF0_RDIV_15:8							
0x1FE	R510	DPLL2_REF0_RDIV							
0x1FF	R511	DPLL2_REF1_RDIV_15:8							
0x200	R512	DPLL2_REF1_RDIV							
0x201	R513	DPLL2_REF2_RDIV_15:8							
0x202	R514	DPLL2_REF2_RDIV							
0x203	R515	DPLL2_REF3_RDIV_15:8							
0x204	R516	DPLL2_REF3_RDIV							
0x205	R517	DPLL2_REF4_RDIV_15:8							
0x206	R518	DPLL2_REF4_RDIV							
0x207	R519	DPLL2_REF5_RDIV_15:8							
0x208	R520	DPLL2_REF5_RDIV							
0x20B	R523	RESERVED		DPLL3_REF0_AUTO_PRTY			DPLL3_REF1_AUTO_PRTY		
0x20C	R524	RESERVED		DPLL3_REF2_AUTO_PRTY			DPLL3_REF3_AUTO_PRTY		
0x20D	R525	RESERVED		DPLL3_REF4_AUTO_PRTY			DPLL3_REF5_AUTO_PRTY		
0x20E	R526	RESERVED		DPLL3_MAN_REFSEL			DPLL3_MAN_SWITCH_PIN_MODE	DPLL3_SWITCH_MODE	
0x20F	R527	RESERVED		DPLL3_REFSEL_STAT					
0x210	R528	DPLL3_LOCKDET_PPM_EN	DPLL3_LOCKDET_PPM_MAX_14:8						
0x211	R529	DPLL3_LOCKDET_PPM_MAX							

Table 1-1. DEVICE Registers (continued)

<table>
<tr><th>Offset</th><th>Acronym</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td>0x212</td><td>R530</td><td>RESERVED</td><td colspan="7">DPLL3_UNLOCKDET_PPM_MAX_14:8</td></tr>
<tr><td>0x213</td><td>R531</td><td colspan="8">DPLL3_UNLOCKDET_PPM_MAX</td></tr>
<tr><td>0x214</td><td>R532</td><td colspan="2">RESERVED</td><td colspan="6">DPLL3_LOCKDET2_PPM_CNTSTRT_29:24</td></tr>
<tr><td>0x215</td><td>R533</td><td colspan="8">DPLL3_LOCKDET2_PPM_CNTSTRT_23:16</td></tr>
<tr><td>0x216</td><td>R534</td><td colspan="8">DPLL3_LOCKDET2_PPM_CNTSTRT_15:8</td></tr>
<tr><td>0x217</td><td>R535</td><td colspan="8">DPLL3_LOCKDET2_PPM_CNTSTRT</td></tr>
<tr><td>0x218</td><td>R536</td><td colspan="2">RESERVED</td><td colspan="6">DPLL3_LOCKDET_PPM_CNTSTRT_29:24</td></tr>
<tr><td>0x219</td><td>R537</td><td colspan="8">DPLL3_LOCKDET_PPM_CNTSTRT_23:16</td></tr>
<tr><td>0x21A</td><td>R538</td><td colspan="8">DPLL3_LOCKDET_PPM_CNTSTRT_15:8</td></tr>
<tr><td>0x21B</td><td>R539</td><td colspan="8">DPLL3_LOCKDET_PPM_CNTSTRT</td></tr>
<tr><td>0x21C</td><td>R540</td><td colspan="2">RESERVED</td><td colspan="6">DPLL3_LOCKDET_VCO_PPM_CNTSTRT_29:24</td></tr>
<tr><td>0x21D</td><td>R541</td><td colspan="8">DPLL3_LOCKDET_VCO_PPM_CNTSTRT_23:16</td></tr>
<tr><td>0x21E</td><td>R542</td><td colspan="8">DPLL3_LOCKDET_VCO_PPM_CNTSTRT_15:8</td></tr>
<tr><td>0x21F</td><td>R543</td><td colspan="8">DPLL3_LOCKDET_VCO_PPM_CNTSTRT</td></tr>
<tr><td>0x220</td><td>R544</td><td colspan="7">RESERVED</td><td>DPLL3_STATUS_PPM_LOCK</td></tr>
<tr><td>0x223</td><td>R547</td><td>DPLL3_LOOP_EN</td><td>DPLL3_PHASE_CANCEL_EN</td><td>DPLL3_FASTLOCK_ALWAYS</td><td>DPLL3_PHS1_EN</td><td>DPLL3_ZDM_EN</td><td>DPLL3_HIST_EN</td><td>DPLL3_PHASE_CANCEL_ALWAYS</td><td>RESERVED</td></tr>
<tr><td>0x224</td><td>R548</td><td>DPLL3_HOLD_SLEW_LIM_EN</td><td colspan="7">RESERVED</td></tr>
<tr><td>0x226</td><td>R550</td><td colspan="3">RESERVED</td><td colspan="5">DPLL3_PH_OFFSET_44:40</td></tr>
<tr><td>0x227</td><td>R551</td><td colspan="8">DPLL3_PH_OFFSET_39:32</td></tr>
<tr><td>0x228</td><td>R552</td><td colspan="8">DPLL3_PH_OFFSET_31:24</td></tr>
<tr><td>0x229</td><td>R553</td><td colspan="8">DPLL3_PH_OFFSET_23:16</td></tr>
<tr><td>0x22A</td><td>R554</td><td colspan="8">DPLL3_PH_OFFSET_15:8</td></tr>
<tr><td>0x22B</td><td>R555</td><td colspan="8">DPLL3_PH_OFFSET</td></tr>
<tr><td>0x22C</td><td>R556</td><td colspan="8">DPLL3_FREE_RUN_39:32</td></tr>
<tr><td>0x22D</td><td>R557</td><td colspan="8">DPLL3_FREE_RUN_31:24</td></tr>
<tr><td>0x22E</td><td>R558</td><td colspan="8">DPLL3_FREE_RUN_23:16</td></tr>
<tr><td>0x22F</td><td>R559</td><td colspan="8">DPLL3_FREE_RUN_15:8</td></tr>
<tr><td>0x230</td><td>R560</td><td colspan="8">DPLL3_FREE_RUN</td></tr>
<tr><td>0x231</td><td>R561</td><td>DPLL3_PPM_REF_SEL</td><td>DPLL3_1PPS_MODE</td><td>DPLL3_1PPS_EN</td><td colspan="5">RESERVED</td></tr>
<tr><td>0x24E</td><td>R590</td><td colspan="6">RESERVED</td><td colspan="2">DPLL3_LCK_TIMER_9:8</td></tr>
</table>

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x24F	R591	DPLL3_LCK_TIMER							
0x250	R592	RESERVED						DPLL3_HIST_TIMER_9:8	
0x251	R593	DPLL3_HIST_TIMER							
0x252	R594	RESERVED						DPLL3_HOLD_TIMER_9:8	
0x253	R595	DPLL3_HOLD_TIMER							
0x254	R596	RESERVED						DPLL3_PHS1_TIMER_9:8	
0x255	R597	DPLL3_PHS1_TIMER							
0x25A	R602	RESERVED			DPLL3_HIST_GAIN				
0x25B	R603	RESERVED		DPLL3_PL_THRESH					
0x25C	R604	RESERVED		DPLL3_PL_UNLK_THRESH					
0x25D	R605	RESERVED		DPLL3_PHS1_THRESH					
0x262	R610	RESERVED		DPLL3_STATUS_PL	RESERVED				
0x263	R611	RESERVED			DPLL3_DCO_SLEW_ACTIVE	RESERVED			
0x266	R614	RESERVED							DPLL3_FB_DIV_32:32
0x267	R615	DPLL3_FB_DIV_31:24							
0x268	R616	DPLL3_FB_DIV_23:16							
0x269	R617	DPLL3_FB_DIV_15:8							
0x26A	R618	DPLL3_FB_DIV							
0x26B	R619	DPLL3_FB_NUM_39:32							
0x26C	R620	DPLL3_FB_NUM_31:24							
0x26D	R621	DPLL3_FB_NUM_23:16							
0x26E	R622	DPLL3_FB_NUM_15:8							
0x26F	R623	DPLL3_FB_NUM							
0x270	R624	DPLL3_FB_DEN_39:32							
0x271	R625	DPLL3_FB_DEN_31:24							
0x272	R626	DPLL3_FB_DEN_23:16							
0x273	R627	DPLL3_FB_DEN_15:8							
0x274	R628	DPLL3_FB_DEN							
0x275	R629	RESERVED							DPLL3_FB2_DIV_32:32
0x276	R630	DPLL3_FB2_DIV_31:24							
0x277	R631	DPLL3_FB2_DIV_23:16							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x278	R632	DPLL3_FB2_DIV_15:8							
0x279	R633	DPLL3_FB2_DIV							
0x27A	R634	DPLL3_FB2_NUM_39:32							
0x27B	R635	DPLL3_FB2_NUM_31:24							
0x27C	R636	DPLL3_FB2_NUM_23:16							
0x27D	R637	DPLL3_FB2_NUM_15:8							
0x27E	R638	DPLL3_FB2_NUM							
0x27F	R639	DPLL3_FB2_DEN_39:32							
0x280	R640	DPLL3_FB2_DEN_31:24							
0x281	R641	DPLL3_FB2_DEN_23:16							
0x282	R642	DPLL3_FB2_DEN_15:8							
0x283	R643	DPLL3_FB2_DEN							
0x284	R644	RESERVED		DPLL3_REF5_FB_SEL	DPLL3_REF4_FB_SEL	DPLL3_REF3_FB_SEL	DPLL3_REF2_FB_SEL	DPLL3_REF1_FB_SEL	DPLL3_REF0_FB_SEL
0x285	R645	RESERVED					DPLL3_FB_MASH_ORDER		
0x286	R646	RESERVED		DPLL3_FB_FDEV_37:32					
0x287	R647	DPLL3_FB_FDEV_31:24							
0x288	R648	DPLL3_FB_FDEV_23:16							
0x289	R649	DPLL3_FB_FDEV_15:8							
0x28A	R650	DPLL3_FB_FDEV							
0x28B	R651	RESERVED							DPLL3_FB_FDEV_UPDATE
0x28C	R652	RESERVED							DPLL3_FB_FDEV_EN
0x28D	R653	DPLL3_FB_NUM_STAT_39:32							
0x28E	R654	DPLL3_FB_NUM_STAT_31:24							
0x28F	R655	DPLL3_FB_NUM_STAT_23:16							
0x290	R656	DPLL3_FB_NUM_STAT_15:8							
0x291	R657	DPLL3_FB_NUM_STAT							
0x292	R658	RESERVED				DPLL3_REF0_DBLR_EN	DPLL3_REF1_DBLR_EN	DPLL3_REF2_DBLR_EN	DPLL3_REF3_DBLR_EN
0x293	R659	DPLL3_REF0_RDIV_15:8							
0x294	R660	DPLL3_REF0_RDIV							
0x295	R661	DPLL3_REF1_RDIV_15:8							
0x296	R662	DPLL3_REF1_RDIV							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x297	R663	DPLL3_REF2_RDIV_15:8							
0x298	R664	DPLL3_REF2_RDIV							
0x299	R665	DPLL3_REF3_RDIV_15:8							
0x29A	R666	DPLL3_REF3_RDIV							
0x29B	R667	DPLL3_REF4_RDIV_15:8							
0x29C	R668	DPLL3_REF4_RDIV							
0x29D	R669	DPLL3_REF5_RDIV_15:8							
0x29E	R670	DPLL3_REF5_RDIV							
0x2C3	R707	PLL1_CP_PU_R							
0x2C4	R708	RESERVED						PLL1_CPG	
0x2C5	R709	RESERVED		PLL1_LF_R2					
0x2C6	R710	RESERVED		PLL1_LF_R3					
0x2C7	R711	RESERVED		PLL1_LF_R4					
0x2C8	R712	PLL1_DISABLE_3RD4TH		PLL1_LF_C3			PLL1_LF_C4		
0x2C9	R713	RESERVED							PLL1_RDIV_8:8
0x2CA	R714	PLL1_RDIV							
0x2CB	R715	RESERVED			PLL1_RDIV_XO_EN	PLL1_RDIV_XO_DBLR_EN	PLL1_RDIV_BYPASS_EN	PLL1_RDIV_MUX_SEL	
0x2CC	R716	RESERVED							PLL1_NDIV_8:8
0x2CD	R717	PLL1_NDIV							
0x2CE	R718	PLL1_NUM_MSB							
0x2CF	R719	PLL1_NUM_39:32							
0x2D0	R720	PLL1_NUM_31:24							
0x2D1	R721	PLL1_NUM_23:16							
0x2D2	R722	PLL1_NUM_15:8							
0x2D3	R723	PLL1_NUM							
0x2D4	R724	RESERVED		PLL1_DTHRMODE		PLL1_ORDER			PLL1_MODE
0x2D5	R725	APLL1_NUM_STAT_39:32							
0x2D6	R726	APLL1_NUM_STAT_31:24							
0x2D7	R727	APLL1_NUM_STAT_23:16							
0x2D8	R728	APLL1_NUM_STAT_15:8							
0x2D9	R729	APLL1_NUM_STAT							
0x2DB	R731	PLL1_PRI_DIV_SYNC_EN	PLL1_PRI_DIV_EN	PLL1_PRI_DIV			PLL1_P1_DIV_OUT0_1_EN	PLL1_P1_DIV_OUT2_3_EN	PLL1_P1_DIV_OUT14_15_EN

Table 1-1. DEVICE Registers (continued)

<table>
<tr><th>Offset</th><th>Acronym</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td>0x2DC</td><td>R732</td><td>PLL1_SEC_DIV_SYNC_EN</td><td>PLL1_SEC_DIV_EN</td><td colspan="3">PLL1_SEC_DIV</td><td>PLL1_P2_DIV_OUT0_1_EN</td><td colspan="2">RESERVED</td></tr>
<tr><td>0x2DD</td><td>R733</td><td>PLL1_VCO_BUF_EN</td><td colspan="2">PLL1_VCO_BUF_2REF_EN</td><td>PLL1_VCO_BUF_2DPLL_EN</td><td>RESERVED</td><td>PLL1_VCO_BUF_PPM_CHECK_EN</td><td colspan="2">PLL1_VCO_BUF_FB_TDC_EN</td></tr>
<tr><td>0x2E0</td><td>R736</td><td>PLL1_NCLK_TEST_EN</td><td colspan="3">RESERVED</td><td>PLL1_RDIV_OUTPUT_EN</td><td colspan="3">RESERVED</td></tr>
<tr><td>0x2E5</td><td>R741</td><td colspan="2">RESERVED</td><td>PLL1_VM_INSIDE</td><td>PLL1_VM_HI</td><td colspan="4">RESERVED</td></tr>
<tr><td>0x2E9</td><td>R745</td><td colspan="2">RESERVED</td><td>PLL1_NDIV_OUTPUT_EN</td><td colspan="5">RESERVED</td></tr>
<tr><td>0x2EA</td><td>R746</td><td colspan="7">RESERVED</td><td>PLL1_VCO_PREBUF_EN</td></tr>
<tr><td>0x305</td><td>R773</td><td colspan="8">RESERVED</td></tr>
<tr><td>0x309</td><td>R777</td><td colspan="8">PLL2_CP_PU_R</td></tr>
<tr><td>0x30A</td><td>R778</td><td colspan="3">RESERVED</td><td>PLL2_CP_PU_DIS</td><td colspan="4">PLL2_CPG</td></tr>
<tr><td>0x30B</td><td>R779</td><td colspan="8">PLL2_LF_R2</td></tr>
<tr><td>0x30C</td><td>R780</td><td colspan="2">RESERVED</td><td colspan="6">PLL2_LF_R3</td></tr>
<tr><td>0x30D</td><td>R781</td><td colspan="2">RESERVED</td><td colspan="6">PLL2_LF_R4</td></tr>
<tr><td>0x30E</td><td>R782</td><td colspan="2">PLL2_DISABLE_3RD4TH</td><td colspan="3">PLL2_LF_C3</td><td colspan="3">PLL2_LF_C4</td></tr>
<tr><td>0x30F</td><td>R783</td><td colspan="7">RESERVED</td><td>PLL2_RDIV_8:8</td></tr>
<tr><td>0x310</td><td>R784</td><td colspan="8">PLL2_RDIV</td></tr>
<tr><td>0x311</td><td>R785</td><td colspan="3">RESERVED</td><td>PLL2_RDIV_XO_EN</td><td>PLL2_RDIV_XO_DBLR_EN</td><td>PLL2_RDIV_BYPASS_EN</td><td colspan="2">PLL2_RDIV_MUX_SEL</td></tr>
<tr><td>0x312</td><td>R786</td><td colspan="7">RESERVED</td><td>PLL2_NDIV_8:8</td></tr>
<tr><td>0x313</td><td>R787</td><td colspan="8">PLL2_NDIV</td></tr>
<tr><td>0x314</td><td>R788</td><td colspan="8">PLL2_NUM_MSB</td></tr>
<tr><td>0x315</td><td>R789</td><td colspan="8">PLL2_NUM_39:32</td></tr>
<tr><td>0x316</td><td>R790</td><td colspan="8">PLL2_NUM_31:24</td></tr>
<tr><td>0x317</td><td>R791</td><td colspan="8">PLL2_NUM_23:16</td></tr>
<tr><td>0x318</td><td>R792</td><td colspan="8">PLL2_NUM_15:8</td></tr>
<tr><td>0x319</td><td>R793</td><td colspan="8">PLL2_NUM</td></tr>
<tr><td>0x31A</td><td>R794</td><td colspan="2">RESERVED</td><td colspan="2">PLL2_DTHRMODE</td><td colspan="3">PLL2_ORDER</td><td>PLL2_MODE</td></tr>
<tr><td>0x31B</td><td>R795</td><td colspan="8">APLL2_NUM_STAT_39:32</td></tr>
<tr><td>0x31C</td><td>R796</td><td colspan="8">APLL2_NUM_STAT_31:24</td></tr>
</table>

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x31D	R797	APLL2_NUM_STAT_23:16							
0x31E	R798	APLL2_NUM_STAT_15:8							
0x31F	R799	APLL2_NUM_STAT							
0x323	R803	RESERVED			PLL2_VCO_BUF_EN	PLL2_VCO_BUF_2REF_EN		PLL2_VCO_BUF_2DPLL_EN	PLL2_VCO_BUF_2WNDDET_EN
0x324	R804	RESERVED		PLL2_VCO_DIV_SYNC_EN	PLL2_VCO_DIV_EN	PLL2_VCO_DIV			
0x325	R805	RESERVED	PLL2_VCO_BUF_FB_TDC_EN		PLL2_P1_OUT14_15_EN	PLL2_P1_OUT8_13_EN	PLL2_P1_OUT4_7_EN	PLL2_P1_OUT2_3_EN	PLL2_P1_OUT0_1_EN
0x328	R808	RESERVED				PLL2_RDIV_OUTPUT_EN	RESERVED		
0x32D	R813	RESERVED		PLL2_VM_INSIDE	PLL2_VM_HI	RESERVED			
0x332	R818	RESERVED		PLL2_NDIV_OUTPUT_EN	RESERVED				
0x333	R819	RESERVED							PLL2_VCO_PREBUF_EN
0x348	R840	PLL3_CPBAW_BLEED							
0x349	R841	RESERVED			PLL3_CP_PU_DIS	PLL3_CPG			
0x34A	R842	RESERVED		PLL3_LF_R2					
0x34B	R843	RESERVED		PLL3_LF_R3					
0x34C	R844	RESERVED		PLL3_LF_R4					
0x34D	R845	RESERVED		PLL3_LF_C3			PLL3_LF_C4		
0x34E	R846	RESERVED							PLL3_RDIV_8:8
0x34F	R847	PLL3_RDIV							
0x350	R848	RESERVED			PLL3_RDIV_XO_EN	PLL3_RDIV_XO_DBLR_EN	PLL3_RDIV_BYPASS_EN	PLL3_RDIV_MUX_SEL	
0x351	R849	RESERVED							PLL3_NDIV_8:8
0x352	R850	PLL3_NDIV							
0x353	R851	PLL3_NUM_MSB							
0x354	R852	PLL3_NUM_39:32							
0x355	R853	PLL3_NUM_31:24							
0x356	R854	PLL3_NUM_23:16							
0x357	R855	PLL3_NUM_15:8							
0x358	R856	PLL3_NUM							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x359	R857	RESERVED		PLL3_DTHRMODE		PLL3_ORDER			PLL3_MODE
0x35A	R858	APLL3_NUM_STAT_39:32							
0x35B	R859	APLL3_NUM_STAT_31:24							
0x35C	R860	APLL3_NUM_STAT_23:16							
0x35D	R861	APLL3_NUM_STAT_15:8							
0x35E	R862	APLL3_NUM_STAT							
0x360	R864	PLL3_VCO_BUF_OUT_EN				PLL3_VCO_DIV_SYNC_EN	PLL3_PRI_DIV		
0x361	R865	PLL3_VCO_DIV_SEL		PLL3_VCO_CHAN_DRVR_IN_EN	PLL3_P1_OUT14_15_EN	PLL3_P1_OUT8_13_EN	PLL3_P1_OUT4_7_EN	PLL3_P1_OUT2_3_EN	PLL3_P1_OUT0_1_EN
0x362	R866	RESERVED			PLL3_VCO_BUF_2REF_EN		PLL3_WIN_DET_DRVR_EN	PLL3_VCO_BUF_FB_TDC_EN	
0x368	R872	RESERVED				PLL3_RDIV_OUTPUT_EN	RESERVED		
0x372	R882	RESERVED		PLL3_NDIV_OUTPUT_EN	RESERVED				
0x3C1	R961	RESERVED	OUT_0_EN	OUT_0_FMT					
0x3C2	R962	OUT_0_CAP_EN	OUT_0_STATIC_LOW	OUT_0_P_CMOS_EN	OUT_0_N_CMOS_EN	OUT_0_P_INVERT_POLARITY	OUT_0_N_INVERT_POLARITY	OUT_0_P_FORCELOW	OUT_0_N_FORCELOW
0x3C3	R963	OUT_0_CONFIGURATION							
0x3C4	R964	RESERVED	OUT_1_EN	OUT_1_FMT					
0x3C5	R965	OUT_1_CAP_EN	OUT_1_STATIC_LOW	OUT_1_P_CMOS_EN	OUT_1_N_CMOS_EN	OUT_1_P_INVERT_POLARITY	OUT_1_N_INVERT_POLARITY	OUT_1_P_FORCELOW	OUT_1_N_FORCELOW
0x3C6	R966	OUT_1_CONFIGURATION							
0x3C7	R967	RESERVED						OUT_0_1_CMOS_OUT_VOLTAGE_SEL	OUT_0_1_CMOS_OUT_LDO_EN
0x3C8	R968	RESERVED				OUT_0_1_ZDM_TDC_SEL			OUT_0_1_ZDM_EN
0x3C9	R969	RESERVED	OUT_0_1_DIV_MUTE_EN	OUT_0_1_DIV_SYNC_EN	OUT_0_1_SR_DIV_SYNC_EN	OUT_0_1_CH0_CHAN_POL_SEL	OUT_0_1_CH1_CHAN_POL_SEL	OUT_0_1_CH0_DIV_EN	OUT_0_1_CH1_DIV_EN
0x3CB	R971	OUT_0_1_CLK_IN_SEL							
0x3CC	R972	RESERVED						OUT_0_1_CH0_CH_DIV_SR_MUX_CLK_SEL	RESERVED
0x3CD	R973	OUT_0_1_CLK_IN_FANOUT						OUT_0_1_CLK_IN_SEL_9:8	
0x3CE	R974	RESERVED				OUT_0_1_CH0_CH_STATIC_OFFSET_11:8			
0x3CF	R975	OUT_0_1_CH0_CH_STATIC_OFFSET							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x3D0	R976	RESERVED				OUT_0_1_CH1_CH_STATIC_OFFSET_11:8			
0x3D1	R977	OUT_0_1_CH1_CH_STATIC_OFFSET							
0x3D2	R978	RESERVED				OUT_0_1_CH0_CH_DIV_11:8			
0x3D3	R979	OUT_0_1_CH0_CH_DIV							
0x3D4	R980	RESERVED				OUT_0_1_CH1_CH_DIV_11:8			
0x3D5	R981	OUT_0_1_CH1_CH_DIV							
0x3D6	R982	RESERVED			OUT_0_1_SR_ANA_DELAY				
0x3D7	R983	RESERVED		OUT_0_1_SR_ANA_DELAY_DIV2_SEL	OUT_0_1_SR_ANA_DELAY_EN	OUT_0_1_SR_ANA_DELAY_SMALL_STEP_EN	OUT_0_1_SR_ANA_DELAY_RANGE		
0x3D8	R984	RESERVED			OUT_0_1_SR_DDLY				
0x3D9	R985	RESERVED				OUT_0_1_SR_DIV_19:16			
0x3DA	R986	OUT_0_1_SR_DIV_15:8							
0x3DB	R987	OUT_0_1_SR_DIV							
0x3DC	R988	RESERVED	OUT_0_1_SR_DIV_STATIC_OFFSET_14:8						
0x3DD	R989	OUT_0_1_SR_DIV_STATIC_OFFSET							
0x3DE	R990	OUT_0_1_SR_REQ_MODE	OUT_0_1_SR_GPIO_EN	RESERVED	OUT_0_1_PULSE_COUNT			OUT_0_1_SR_MODE	
0x3DF	R991	RESERVED		OUT_0_1_SR_CH0_DIV_BYPASS	RESERVED				
0x400	R1024	RESERVED	OUT_2_EN	OUT_2_FMT					
0x401	R1025	RESERVED				OUT_2_CAP_EN	OUT_2_CONFIGURATION		
0x402	R1026	OUT_2_CHAN_POL_SEL	OUT_2_CLK_MUX		RESERVED	OUT_2_DIV_EN	OUT_2_CH_MUX_SEL		
0x403	R1027	RESERVED			OUT_2_MUTE_EN	OUT_2_SYNC_EN	RESERVED		
0x404	R1028	RESERVED				OUT_2_CH_STATIC_OFFSET_11:8			
0x405	R1029	OUT_2_CH_STATIC_OFFSET							
0x406	R1030	RESERVED				OUT_2_CH_DIV_11:8			
0x407	R1031	OUT_2_CH_DIV							
0x420	R1056	RESERVED	OUT_3_EN	OUT_3_FMT					
0x421	R1057	RESERVED				OUT_3_CAP_EN	OUT_3_CONFIGURATION		
0x422	R1058	OUT_3_CHAN_POL_SEL	OUT_3_CLK_MUX		RESERVED	OUT_3_DIV_EN	OUT_3_CH_MUX_SEL		

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x423	R1059	RESERVED			OUT_3_MUTE_EN	OUT_3_SYNC_EN	RESERVED		
0x424	R1060	RESERVED				OUT_3_CH_STATIC_OFFSET_11:8			
0x425	R1061	OUT_3_CH_STATIC_OFFSET							
0x426	R1062	RESERVED				OUT_3_CH_DIV_11:8			
0x427	R1063	OUT_3_CH_DIV							
0x440	R1088	RESERVED					OUT_4_5_SR_ANA_DLY_BIASTRIM		
0x441	R1089	RESERVED	OUT_4_EN	OUT_4_FMT					
0x442	R1090	RESERVED	OUT_4_CAP_EN	RESERVED	OUT_4_CONFIGURATION				
0x443	R1091	RESERVED	OUT_5_EN	OUT_5_FMT					
0x444	R1092	RESERVED	OUT_5_CAP_EN	RESERVED	OUT_5_CONFIGURATION				
0x445	R1093	RESERVED		OUT_4_5_DIV_SYNC_EN	OUT_4_5_SR_DIV_SYNC_EN	RESERVED		OUT_4_5_CHAN_POL_SEL	OUT_4_5_DIV_EN
0x446	R1094	OUT_4_5_MUTE_EN	OUT_4_5_ZDM_EN	OUT_4_5_CLK_IN_SEL	OUT_4_5_CH_DIV_SR_MUX_CLK_SEL	OUT_4_5_CH_MUX_SEL			
0x447	R1095	RESERVED				OUT_4_5_CH_STATIC_OFFSET_11:8			
0x448	R1096	OUT_4_5_CH_STATIC_OFFSET							
0x449	R1097	RESERVED				OUT_4_5_CH_DIV_11:8			
0x44A	R1098	OUT_4_5_CH_DIV							
0x44B	R1099	RESERVED			OUT_4_5_SR_ANA_DELAY				
0x44C	R1100	RESERVED		OUT_4_5_SR_ANA_DELAY_DIV2_SEL	OUT_4_5_SR_ANA_DELAY_EN	OUT_4_5_SR_ANA_DELAY_SMALL_STEP_EN	OUT_4_5_SR_ANA_DELAY_RANGE		
0x44D	R1101	RESERVED			OUT_4_5_SR_DDLY				
0x44E	R1102	RESERVED				OUT_4_5_SR_DIV_19:16			
0x44F	R1103	OUT_4_5_SR_DIV_15:8							
0x450	R1104	OUT_4_5_SR_DIV							
0x451	R1105	RESERVED	OUT_4_5_SR_DIV_STATIC_OFFSET_14:8						
0x452	R1106	OUT_4_5_SR_DIV_STATIC_OFFSET							
0x453	R1107	RESERVED	OUT_4_5_SR_REQ_MODE	OUT_4_5_PULSE_COUNT			OUT_4_5_SR_GPIO_EN	OUT_4_5_SR_MODE	
0x454	R1108	RESERVED			OUT_4_5_SR_CH_DIV_BYPASS	RESERVED			
0x461	R1121	RESERVED	OUT_6_EN	OUT_6_FMT					
0x462	R1122	RESERVED	OUT_6_CAP_EN	RESERVED	OUT_6_CONFIGURATION				

Table 1-1. DEVICE Registers (continued)

<table>
<tr><th>Offset</th><th>Acronym</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td>0x463</td><td>R1123</td><td>RESERVED</td><td>OUT_7_EN</td><td colspan="6">OUT_7_FMT</td></tr>
<tr><td>0x464</td><td>R1124</td><td>RESERVED</td><td>OUT_7_CAP_EN</td><td>RESERVED</td><td colspan="5">OUT_7_CONFIGURATION</td></tr>
<tr><td>0x465</td><td>R1125</td><td colspan="2">RESERVED</td><td>OUT_6_7_DIV_SYNC_EN</td><td>OUT_6_7_SR_DIV_SYNC_EN</td><td colspan="2">RESERVED</td><td>OUT_6_7_CHAN_POL_SEL</td><td>OUT_6_7_DIV_EN</td></tr>
<tr><td>0x466</td><td>R1126</td><td>OUT_6_7_MUTE_EN</td><td>RESERVED</td><td>OUT_6_7_CLK_IN_SEL</td><td>OUT_6_7_CH_DIV_SR_MUX_CLK_SEL</td><td colspan="4">OUT_6_7_CH_MUX_SEL</td></tr>
<tr><td>0x467</td><td>R1127</td><td colspan="4">RESERVED</td><td colspan="4">OUT_6_7_CH_STATIC_OFFSET_11:8</td></tr>
<tr><td>0x468</td><td>R1128</td><td colspan="8">OUT_6_7_CH_STATIC_OFFSET</td></tr>
<tr><td>0x469</td><td>R1129</td><td colspan="4">RESERVED</td><td colspan="4">OUT_6_7_CH_DIV_11:8</td></tr>
<tr><td>0x46A</td><td>R1130</td><td colspan="8">OUT_6_7_CH_DIV</td></tr>
<tr><td>0x46B</td><td>R1131</td><td colspan="3">RESERVED</td><td colspan="5">OUT_6_7_SR_ANA_DELAY</td></tr>
<tr><td>0x46C</td><td>R1132</td><td colspan="2">RESERVED</td><td>OUT_6_7_SR_ANA_DELAY_DIV2_SEL</td><td>OUT_6_7_SR_ANA_DELAY_EN</td><td>OUT_6_7_SR_ANA_DELAY_SMALL_STEP_EN</td><td colspan="3">OUT_6_7_SR_ANA_DELAY_RANGE</td></tr>
<tr><td>0x46D</td><td>R1133</td><td colspan="3">RESERVED</td><td colspan="5">OUT_6_7_SR_DDLY</td></tr>
<tr><td>0x46E</td><td>R1134</td><td colspan="4">RESERVED</td><td colspan="4">OUT_6_7_SR_DIV_19:16</td></tr>
<tr><td>0x46F</td><td>R1135</td><td colspan="8">OUT_6_7_SR_DIV_15:8</td></tr>
<tr><td>0x470</td><td>R1136</td><td colspan="8">OUT_6_7_SR_DIV</td></tr>
<tr><td>0x471</td><td>R1137</td><td>RESERVED</td><td colspan="7">OUT_6_7_SR_DIV_STATIC_OFFSET_14:8</td></tr>
<tr><td>0x472</td><td>R1138</td><td colspan="8">OUT_6_7_SR_DIV_STATIC_OFFSET</td></tr>
<tr><td>0x473</td><td>R1139</td><td>RESERVED</td><td>OUT_6_7_SR_REQ_MODE</td><td colspan="3">OUT_6_7_PULSE_COUNT</td><td>OUT_6_7_SR_GPIO_EN</td><td colspan="2">OUT_6_7_SR_MODE</td></tr>
<tr><td>0x474</td><td>R1140</td><td colspan="3">RESERVED</td><td>OUT_6_7_SR_CH_DIV_BYPASS</td><td colspan="4">RESERVED</td></tr>
<tr><td>0x481</td><td>R1153</td><td>RESERVED</td><td>OUT_8_EN</td><td colspan="6">OUT_8_FMT</td></tr>
<tr><td>0x482</td><td>R1154</td><td>RESERVED</td><td>OUT_8_CAP_EN</td><td>RESERVED</td><td colspan="5">OUT_8_CONFIGURATION</td></tr>
<tr><td>0x483</td><td>R1155</td><td>RESERVED</td><td>OUT_9_EN</td><td colspan="6">OUT_9_FMT</td></tr>
<tr><td>0x484</td><td>R1156</td><td>RESERVED</td><td>OUT_9_CAP_EN</td><td>RESERVED</td><td colspan="5">OUT_9_CONFIGURATION</td></tr>
<tr><td>0x485</td><td>R1157</td><td colspan="2">RESERVED</td><td>OUT_8_9_DIV_SYNC_EN</td><td>OUT_8_9_SR_DIV_SYNC_EN</td><td colspan="2">RESERVED</td><td>OUT_8_9_CHAN_POL_SEL</td><td>OUT_8_9_DIV_EN</td></tr>
<tr><td>0x486</td><td>R1158</td><td>OUT_8_9_MUTE_EN</td><td>RESERVED</td><td>OUT_8_9_CLK_IN_SEL</td><td>OUT_8_9_CH_DIV_SR_MUX_CLK_SEL</td><td colspan="4">OUT_8_9_CH_MUX_SEL</td></tr>
<tr><td>0x487</td><td>R1159</td><td colspan="4">RESERVED</td><td colspan="4">OUT_8_9_CH_STATIC_OFFSET_11:8</td></tr>
<tr><td>0x488</td><td>R1160</td><td colspan="8">OUT_8_9_CH_STATIC_OFFSET</td></tr>
<tr><td>0x489</td><td>R1161</td><td colspan="4">RESERVED</td><td colspan="4">OUT_8_9_CH_DIV_11:8</td></tr>
</table>

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x48A	R1162	OUT_8_9_CH_DIV							
0x48B	R1163	RESERVED			OUT_8_9_SR_ANA_DELAY				
0x48C	R1164	RESERVED		OUT_8_9_SR_ANA_DELAY_DIV2_SEL	OUT_8_9_SR_ANA_DELAY_EN	OUT_8_9_SR_ANA_DELAY_SMALL_STEP_EN	OUT_8_9_SR_ANA_DELAY_RANGE		
0x48D	R1165	RESERVED			OUT_8_9_SR_DDLY				
0x48E	R1166	RESERVED				OUT_8_9_SR_DIV_19:16			
0x48F	R1167	OUT_8_9_SR_DIV_15:8							
0x490	R1168	OUT_8_9_SR_DIV							
0x491	R1169	RESERVED	OUT_8_9_SR_DIV_STATIC_OFFSET_14:8						
0x492	R1170	OUT_8_9_SR_DIV_STATIC_OFFSET							
0x493	R1171	RESERVED	OUT_8_9_SR_REQ_MODE	OUT_8_9_PULSE_COUNT			OUT_8_9_SR_GPIO_EN	OUT_8_9_SR_MODE	
0x4A1	R1185	RESERVED	OUT_10_EN	OUT_10_FMT					
0x4A2	R1186	RESERVED	OUT_10_CAP_EN	RESERVED	OUT_10_CONFIGURATION				
0x4A3	R1187	RESERVED	OUT_11_EN	OUT_11_FMT					
0x4A4	R1188	RESERVED	OUT_11_CAP_EN	RESERVED	OUT_11_CONFIGURATION				
0x4A5	R1189	RESERVED		OUT_10_11_DIV_SYNC_EN	OUT_10_11_SR_DIV_SYNC_EN	RESERVED		OUT_10_11_CHAN_POL_SEL	OUT_10_11_DIV_EN
0x4A6	R1190	OUT_10_11_MUTE_EN	OUT_10_11_ZDM_EN	OUT_10_11_CLK_IN_SEL	OUT_10_11_CH_DIV_SR_MUX_CLK_SEL	OUT_10_11_CH_MUX_SEL			
0x4A7	R1191	RESERVED				OUT_10_11_CH_STATIC_OFFSET_11:8			
0x4A8	R1192	OUT_10_11_CH_STATIC_OFFSET							
0x4A9	R1193	RESERVED				OUT_10_11_CH_DIV_11:8			
0x4AA	R1194	OUT_10_11_CH_DIV							
0x4AB	R1195	RESERVED			OUT_10_11_SR_ANA_DELAY				
0x4AC	R1196	RESERVED		OUT_10_11_SR_ANA_DELAY_DIV2_SEL	OUT_10_11_SR_ANA_DELAY_EN	OUT_10_11_SR_ANA_DELAY_SMALL_STEP_EN	OUT_10_11_SR_ANA_DELAY_RANGE		
0x4AD	R1197	RESERVED			OUT_10_11_SR_DDLY				
0x4AE	R1198	RESERVED				OUT_10_11_SR_DIV_19:16			
0x4AF	R1199	OUT_10_11_SR_DIV_15:8							
0x4B0	R1200	OUT_10_11_SR_DIV							
0x4B1	R1201	RESERVED	OUT_10_11_SR_DIV_STATIC_OFFSET_14:8						

Table 1-1. DEVICE Registers (continued)

<table>
<tr><th>Offset</th><th>Acronym</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td>0x4B2</td><td>R1202</td><td colspan="8">OUT_10_11_SR_DIV_STATIC_OFFSET</td></tr>
<tr><td>0x4B3</td><td>R1203</td><td>RESERVED</td><td>OUT_10_11_SR_REQ_MODE</td><td colspan="3">OUT_10_11_PULSE_COUNT</td><td>OUT_10_11_SR_GPIO_EN</td><td colspan="2">OUT_10_11_SR_MODE</td></tr>
<tr><td>0x4B4</td><td>R1204</td><td colspan="3">RESERVED</td><td>OUT_10_11_SR_CH_DIV_BYPASS</td><td colspan="4">RESERVED</td></tr>
<tr><td>0x4C1</td><td>R1217</td><td>RESERVED</td><td>OUT_12_EN</td><td colspan="6">OUT_12_FMT</td></tr>
<tr><td>0x4C2</td><td>R1218</td><td>RESERVED</td><td>OUT_12_CAP_EN</td><td>RESERVED</td><td colspan="5">OUT_12_CONFIGURATION</td></tr>
<tr><td>0x4C3</td><td>R1219</td><td>RESERVED</td><td>OUT_13_EN</td><td colspan="6">OUT_13_FMT</td></tr>
<tr><td>0x4C4</td><td>R1220</td><td>RESERVED</td><td>OUT_13_CAP_EN</td><td>RESERVED</td><td colspan="5">OUT_13_CONFIGURATION</td></tr>
<tr><td>0x4C5</td><td>R1221</td><td colspan="2">RESERVED</td><td>OUT_12_13_DIV_SYNC_EN</td><td>OUT_12_13_SR_DIV_SYNC_EN</td><td colspan="2">RESERVED</td><td>OUT_12_13_CHAN_POL_SEL</td><td>OUT_12_13_DIV_EN</td></tr>
<tr><td>0x4C6</td><td>R1222</td><td>OUT_12_13_MUTE_EN</td><td>RESERVED</td><td>OUT_12_13_CLK_IN_SEL</td><td>OUT_12_13_CH_DIV_SR_MUX_CLK_SEL</td><td colspan="4">OUT_12_13_CH_MUX_SEL</td></tr>
<tr><td>0x4C7</td><td>R1223</td><td colspan="4">RESERVED</td><td colspan="4">OUT_12_13_CH_STATIC_OFFSET_11:8</td></tr>
<tr><td>0x4C8</td><td>R1224</td><td colspan="8">OUT_12_13_CH_STATIC_OFFSET</td></tr>
<tr><td>0x4C9</td><td>R1225</td><td colspan="4">RESERVED</td><td colspan="4">OUT_12_13_CH_DIV_11:8</td></tr>
<tr><td>0x4CA</td><td>R1226</td><td colspan="8">OUT_12_13_CH_DIV</td></tr>
<tr><td>0x4CB</td><td>R1227</td><td colspan="3">RESERVED</td><td colspan="5">OUT_12_13_SR_ANA_DELAY</td></tr>
<tr><td>0x4CC</td><td>R1228</td><td colspan="2">RESERVED</td><td>OUT_12_13_SR_ANA_DELAY_DIV2_SEL</td><td>OUT_12_13_SR_ANA_DELAY_EN</td><td>OUT_12_13_SR_ANA_DELAY_SMALL_STEP_EN</td><td colspan="3">OUT_12_13_SR_ANA_DELAY_RANGE</td></tr>
<tr><td>0x4CD</td><td>R1229</td><td colspan="3">RESERVED</td><td colspan="5">OUT_12_13_SR_DDLY</td></tr>
<tr><td>0x4CE</td><td>R1230</td><td colspan="4">RESERVED</td><td colspan="4">OUT_12_13_SR_DIV_19:16</td></tr>
<tr><td>0x4CF</td><td>R1231</td><td colspan="8">OUT_12_13_SR_DIV_15:8</td></tr>
<tr><td>0x4D0</td><td>R1232</td><td colspan="8">OUT_12_13_SR_DIV</td></tr>
<tr><td>0x4D1</td><td>R1233</td><td>RESERVED</td><td colspan="7">OUT_12_13_SR_DIV_STATIC_OFFSET_14:8</td></tr>
<tr><td>0x4D2</td><td>R1234</td><td colspan="8">OUT_12_13_SR_DIV_STATIC_OFFSET</td></tr>
<tr><td>0x4D3</td><td>R1235</td><td>RESERVED</td><td>OUT_12_13_SR_REQ_MODE</td><td colspan="3">OUT_12_13_PULSE_COUNT</td><td>OUT_12_13_SR_GPIO_EN</td><td colspan="2">OUT_12_13_SR_MODE</td></tr>
<tr><td>0x4D4</td><td>R1236</td><td colspan="3">RESERVED</td><td>OUT_12_13_SR_CH_DIV_BYPASS</td><td colspan="4">RESERVED</td></tr>
<tr><td>0x4E0</td><td>R1248</td><td colspan="2">RESERVED</td><td colspan="6">OUT_14_FMT</td></tr>
</table>

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x500	R1280	RESERVED		OUT_15_FMT					

Complex bit access types are encoded to fit into small table cells. Table 1-2 shows the codes that are used for access types in this section.

Table 1-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WSC	W	Write
Reset or Default Value		
-n		Value after reset or the default value

1.1 R0 (Offset = 0x0)

Return to the Summary Table.

Table 1-3. R0 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VNDRID_15:8	R	0x10	See Register 1

1.2 R1 (Offset = 0x1)

Return to the Summary Table.

Table 1-4. R1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VNDRID	R	0xB	Vendor Identification Number. The Vendor Identification Number is a unique 16-bit identification number assigned to I2C/SMBus vendors. ROM=N, EEPROM=N

1.3 R2 (Offset = 0x2)

Return to the Summary Table.

Table 1-5. R2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRODID	R	0x42	Product ID. ROM=N, EEPROM=N

1.4 R3 (Offset = 0x3)

Return to the Summary Table.

Table 1-6. R3 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REVID	R	0x4	Revision ID. ROM=N, EEPROM=N

1.5 R4 (Offset = 0x4)

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Table 1-7. R4 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_47:40	R	0x0	Part ID. Used for manufacturing ROM=N, EEPROM=Y

1.6 R5 (Offset = 0x5)

Return to the Summary Table.

Table 1-8. R5 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_39:32	R	0x0	Part ID. Used for manufacturing ROM=N, EEPROM=Y

1.7 R6 (Offset = 0x6)

Return to the Summary Table.

Table 1-9. R6 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_31:24	R	0x0	Part ID. Used for manufacturing ROM=N, EEPROM=Y

1.8 R7 (Offset = 0x7)

Return to the Summary Table.

Table 1-10. R7 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_23:16	R	0x0	Part ID. Used for manufacturing ROM=N, EEPROM=Y

1.9 R8 (Offset = 0x8)

Return to the Summary Table.

Table 1-11. R8 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_15:8	R	0x0	Part ID. Used for manufacturing ROM=N, EEPROM=Y

1.10 R9 (Offset = 0x9)

Return to the Summary Table.

Table 1-12. R9 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID	R	0x0	Part ID. Used for manufacturing ROM=N, EEPROM=Y

1.11 R16 (Offset = 0x10)

Return to the Summary Table.

Table 1-13. R16 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMCNT	R	0x12	NVM Program Count. The NVMCNT increments automatically after every EEPROM Erase/ Program Cycle. The NVMCNT value is retrieved automatically after reset, after a NVM Commit operation, or after a Erase/Program cycle. The NVMCNT register will increment until it reaches it's maximum value of 255 after which no further increments will take place. ROM=N, EEPROM=Y

1.12 R18 (Offset = 0x12)

Return to the Summary Table.

Table 1-14. R18 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	TARGET_ADR_MSB	R	0x19	I2C/SMBus Target Address. This field holds the 5 MSB bits of the Target Address used to identify this device during I2C/SMBus transactions. The two least significant bits of the Target Address are defined by CSC/ADD/TEC pin upon power-up. This is user-writable to EEPROM only through SRAM register at address 12. ROM=N, EEPROM=Y

1.13 R19 (Offset = 0x13)

Return to the Summary Table.

Table 1-15. R19 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	EEREV	R/W	0x0	EEPROM Image Revision ID. EEPROM Image Revision is automatically retrieved from EEPROM and stored in the EEREV register after a reset or after a NVM commit operation. This is user-writable to EEPROM only through SRAM register address 13. ROM=N, EEPROM=Y

1.14 R20 (Offset = 0x14)

Return to the Summary Table.

Table 1-16. R20 Field Descriptions

Bit	Field	Type	Reset	Description
7	ROM_PLUS_EE	R/W	0x0	When set, the thin EEPROM settings are loaded. This is user-writable to EEPROM only through SRAM register address 14. ROM=N, EEPROM=Y
6:3	EE_ROM_PAGE_SEL	R/W	0x0	EE_ROM_PAGE_SEL value is added to the GPIO pin value for selecting the start-up ROM. ROM=N, EEPROM=Y

Table 1-16. R20 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	R	0x0	Reserved

1.15 R21 (Offset = 0x15)

Return to the Summary Table.

Table 1-17. R21 Field Descriptions

Bit	Field	Type	Reset	Description
7	SPI_3WIRE_DIS	R/W	0x1	Disable SPI 3 wire readback. The SDIO pin will remain input at all times. ROM=Y, EEPROM=N 0x0 = 3-wire SPI readback enabled 0x1 = 3-wire SPI readback disabled
6	SYNC_SW	R/W	0x0	Software SYNC Assertion. Writing a '1' to this bit is equivalent to asserting the SYNC pin. SYNC_EN must also be set to 1. ROM=Y, EEPROM=Y
5:0	RESERVED	R	0x0	Reserved

1.16 R22 (Offset = 0x16)

Return to the Summary Table.

Table 1-18. R22 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL3_EN	R/W	0x1	Enable DPLL3. ROM=Y, EEPROM=N
4	APLL3_EN	R/W	0x1	Enable APLL3. ROM=Y, EEPROM=Y
3	DPLL2_EN	R/W	0x0	Enable DPLL2. ROM=Y, EEPROM=N
2	APLL2_EN	R/W	0x1	Enable APLL2. ROM=Y, EEPROM=Y
1	DPLL1_EN	R/W	0x0	Enable DPLL1. ROM=Y, EEPROM=N
0	APLL1_EN	R/W	0x1	Enable APLL1. ROM=Y, EEPROM=Y

1.17 R23 (Offset = 0x17)

Return to the Summary Table.

Table 1-19. R23 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	SWRST	R/W	0x0	Software Reset ALL functions (active low). Writing a '0' will cause the device to return to its power-up state apart from the programmed registers and the configuration controller. The configuration controller is excluded to prevent an re-transfer of EEPROM data to on-chip registers. Not a self clearing field. ROM=N, EEPROM=N
5	DPLL3_SWRST	R-0/W1S	0x0	Software Reset DPLL3.. Setting to '1' resets the DPLL loop filter.This bit is automatically cleared to '0'. ROM=N, EEPROM=N
4	DPLL2_SWRST	R-0/W1S	0x0	Software Reset DPLL2. Setting to '1' resets the DPLL loop filter. This bit is automatically cleared to '0'. ROM=N, EEPROM=N
3	DPLL1_SWRST	R-0/W1S	0x0	Software Reset DPLL1. Setting to '1' resets the DPLL loop filter. This bit is automatically cleared to '0'. ROM=N, EEPROM=N
2	APLL3_SWRST	R-0/W1S	0x0	Software Reset PLL3. Setting to '1' resets the PLL Calibrator, the PLL N Divider, R Divider and VCO Divider. The PLL Calibrator then takes control of the N Divider reset. This bit is automatically cleared to '0'. It does not reset the divider driving the CMOS Outputs. ROM=N, EEPROM=N
1	APLL2_SWRST	R-0/W1S	0x0	Software Reset PLL2. Setting to '1' resets the PLL Calibrator, the PLL N Divider, R Divider and VCO Divider. The PLL Calibrator then takes control of the N Divider reset. This bit is automatically cleared to '0'. It does not reset the divider driving the CMOS Outputs. ROM=N, EEPROM=N
0	APLL1_SWRST	R-0/W1S	0x0	Software Reset PLL1. Setting to '1' resets the PLL Calibrator, the PLL N Divider, R Divider and VCO Divider. The PLL Calibrator then takes control of the N Divider reset. This bit is automatically cleared to '0'. It does not reset the divider driving the CMOS Outputs. ROM=N, EEPROM=N

1.18 R24 (Offset = 0x18)

Return to the Summary Table.

Table 1-20. R24 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	APLL3_STRT_PRTY	R/W	0x0	APLL3 Start-up Priority. 0 is highest priority. APLLs with the same priority will start simultaneously. ROM=Y, EEPROM=Y

Table 1-20. R24 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	APLL2_STRT_PRTY	R/W	0x2	APLL2 Start-up Priority. 0 is highest priority. APLLs with the same priority will start simultaneously. ROM=Y, EEPROM=Y
1:0	APLL1_STRT_PRTY	R/W	0x1	APLL1 Start-up Priority. 0 is highest priority. APLLs with the same priority will start simultaneously. ROM=Y, EEPROM=Y

1.19 R25 (Offset = 0x19)

Return to the Summary Table.

Table 1-21. R25 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:1	RESERVED	R	0x0	Reserved
0	SYNC_EN	R/W	0x1	Allows SYNC from SYNC_SW and GPIO pin. For GPIO sync, must be set together with SYNC input for GPIOx_MODE. ROM=Y, EEPROM=Y

1.20 R26 (Offset = 0x1A)

Return to the Summary Table.

Table 1-22. R26 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	SYSREF_REQ_MODE	R/W	0x3	SYSREF Request Mode. Determines how a GPIO input is syncronized to generate a SYSREF request. ROM=Y, EEPROM=N 0x0 = Direct SYSREF request 0x1 = Reserved 0x2 = Reserved 0x3 = Resampled SYSREF request
3:1	SYSREF_REQ_SEL	R/W	0x3	SYSREF Request Select. Choses which output drives the SYSREF feedback clock. ROM=Y, EEPROM=N 0x0 = SYSREF0_1_CLK 0x1 = SYSREF4_5_CLK 0x2 = SYSREF6_7_CLK 0x3 = SYSREF8_9_CLK 0x4 = SYSREF10_11_CLK 0x5 = SYSREF12_13_CLK 0x6 = Reserved

Table 1-22. R26 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SYSREF_REQ_SW	R/WSC	0x0	Software SYSREF request trigger ROM=N, EEPROM=N

1.21 R27 (Offset = 0x1B)

Return to the Summary Table.

Table 1-23. R27 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR_39:32	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.22 R28 (Offset = 0x1C)

Return to the Summary Table.

Table 1-24. R28 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR_31:24	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.23 R29 (Offset = 0x1D)

Return to the Summary Table.

Table 1-25. R29 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR_23:16	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.24 R30 (Offset = 0x1E)

Return to the Summary Table.

Table 1-26. R30 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR_15:8	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.25 R31 (Offset = 0x1F)

Return to the Summary Table.

Table 1-27. R31 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.26 R32 (Offset = 0x20)

Return to the Summary Table.

Table 1-28. R32 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	TEC_CNTR_TRIG_SEL	R/W	0x0	Time Elapsed Counter trigger select. If using GPIO, must also set GPIOx_MODE to provide TEC trigger. ROM=Y, EEPROM=N 0x0 = SPI 0x1 = GPIO
0	TEC_CNTR_EN	R/W	0x0	Time Elapsed Counter counter enable. When transitioning from 0 --> 1, the TEC counter will start from 0. ROM=Y, EEPROM=N

1.27 R33 (Offset = 0x21)

Return to the Summary Table.

Table 1-29. R33 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	LOL_PLL1	R	0x0	Loss of Lock - APLL1 ROM=N, EEPROM=N
2	LOL_PLL2	R	0x0	Loss of Lock - APLL2 ROM=N, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	LOS_FDET_XO	R	0x0	Loss of Source Freq Detection - XO ROM=N, EEPROM=N

1.28 R34 (Offset = 0x22)

Return to the Summary Table.

Table 1-30. R34 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1	R	0x1	Loss of Phase Lock - DPLL1 ROM=N, EEPROM=N
6	LOFL_DPLL1	R	0x1	Loss of Frequency Lock - DPLL1 ROM=N, EEPROM=N
5	RESERVED	R	0x0	Reserved
4	HLDOVR1	R	0x1	Holdover event - DPLL1 ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.29 R35 (Offset = 0x23)

Return to the Summary Table.

Table 1-31. R35 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2	R	0x0	Loss of Phase Lock - DPLL2 ROM=N, EEPROM=N
6	LOFL_DPLL2	R	0x0	Loss of Frequency Lock - DPLL2 ROM=N, EEPROM=N
5	RESERVED	R	0x0	Reserved
4	HLDOVR2	R	0x0	Holdover event - DPLL2 ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.30 R36 (Offset = 0x24)

Return to the Summary Table.

Table 1-32. R36 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL3	R	0x0	Loss of Phase Lock - DPLL3 ROM=N, EEPROM=N
6	LOFL_DPLL3	R	0x0	Loss of Frequency Lock - DPLL3 ROM=N, EEPROM=N
5	RESERVED	R	0x0	Reserved

Table 1-32. R36 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	HLDOVR3	R	0x0	Holdover event - DPLL3 ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.31 R37 (Offset = 0x25)

Return to the Summary Table.

Table 1-33. R37 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	LOL_PLL1_MASK	R/W	0x0	Masks Loss of Lock - APLL1. When LOL_PLL1_MASK is 1 then the LOL_PLL1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
2	LOL_PLL2_MASK	R/W	0x0	Masks Loss of Lock - APLL2. When LOL_PLL2_MASK is 1 then the LOL_PLL2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	LOS_FDET_XO_MASK	R/W	0x0	Masks Loss of Source Freq Detection - XO. When LOS_FDET_XO_MASK is 1 then the LOS_FDET_XO interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.32 R38 (Offset = 0x26)

Return to the Summary Table.

Table 1-34. R38 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_MASK	R/W	0x1	Masks Loss of Phase Lock - DPLL1. When LOPL_DPLL1_MASK is 1 then the LOPL_DPLL1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
6	LOFL_DPLL1_MASK	R/W	0x1	Masks Loss of Freq Lock - DPLL1. When LOFL_DPLL1_MASK is 1 then the LOFL_DPLL1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
5	HIST1_MASK	R/W	0x1	Masks Tuning word history update - DPLL1. When HIST1_MASK is 1 then the HIST1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

Table 1-34. R38 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	HLDOVR1_MASK	R/W	0x1	Masks Holdover event - DPLL1. When HLDOVR1_MASK is 1 then the HLDOVR1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
3	REFSWITCH1_MASK	R/W	0x1	Masks Reference Switchover - DPLL1. When REFSWITCH1_MASK is 1 then the REFSWITCH1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
2	LOR_MISSCLK1_MASK	R/W	0x1	Masks Loss of Active Reference - Missing Clock - DPLL1. When LOR_MISSCLK1_MASK is 1 then the LOR_MISSCLK1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	LOR_FREQ1_MASK	R/W	0x1	Masks Loss of Active Reference - Frequency - DPLL1. When LOR_FREQ1_MASK is 1 then the LOR_FREQ1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
0	LOR_PH1_MASK	R/W	0x1	Masks Loss of Active Reference - Phase - DPLL1. When LOR_PH1_MASK is 1 then the LOR_PH1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.33 R39 (Offset = 0x27)

Return to the Summary Table.

Table 1-35. R39 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_MASK	R/W	0x1	Masks Loss of Phase Lock - DPLL2. When LOPL_DPLL2_MASK is 1 then the LOPL_DPLL2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
6	LOFL_DPLL2_MASK	R/W	0x1	Masks Loss of Freq Lock - DPLL2. When LOFL_DPLL2_MASK is 1 then the LOFL_DPLL2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
5	HIST2_MASK	R/W	0x1	Masks Tuning word history update - DPLL2. When HIST2_MASK is 1 then the HIST2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
4	HLDOVR2_MASK	R/W	0x1	Masks Holdover event - DPLL2. When HLDOVR2_MASK is 1 then the HLDOVR2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
3	REFSWITCH2_MASK	R/W	0x1	Masks Reference Switchover - DPLL2. When REFSWITCH2_MASK is 1 then the REFSWITCH2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

Table 1-35. R39 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LOR_MISSCLK2_MASK	R/W	0x1	Masks Loss of Active Reference - Missing Clock - DPLL2. When LOR_MISSCLK2_MASK is 1 then the LOR_MISSCLK2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	LOR_FREQ2_MASK	R/W	0x1	Masks Loss of Active Reference - Frequency - DPLL2. When LOR_FREQ2_MASK is 1 then the LOR_FREQ2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
0	LOR_PH2_MASK	R/W	0x1	Masks Loss of Active Reference - Phase - DPLL2. When LOR_PH2_MASK is 1 then the LOR_PH2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.34 R40 (Offset = 0x28)

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Table 1-36. R40 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL3_MASK	R/W	0x0	Masks Loss of Phase Lock - DPLL3. When LOPL_DPLL3_MASK is 1 then the LOPL_DPLL3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
6	LOFL_DPLL3_MASK	R/W	0x0	Masks Loss of Freq Lock - DPLL3. When LOFL_DPLL3_MASK is 1 then the LOFL_DPLL3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
5	HIST3_MASK	R/W	0x1	Masks Tuning word history update - DPLL3. When HIST3_MASK is 1 then the HIST3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
4	HLDOVR3_MASK	R/W	0x0	Masks Holdover event - DPLL3. When HLDOVR3_MASK is 1 then the HLDOVR3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
3	REFSWITCH3_MASK	R/W	0x0	Masks Reference Switchover - DPLL3. When REFSWITCH3_MASK is 1 then the REFSWITCH3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
2	LOR_MISSCLK3_MASK	R/W	0x0	Masks Loss of Active Reference - Missing Clock - DPLL3. When LOR_MISSCLK3_MASK is 1 then the LOR_MISSCLK3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	LOR_FREQ3_MASK	R/W	0x0	Masks Loss of Active Reference - Frequency - DPLL3. When LOR_FREQ3_MASK is 1 then the LOR_FREQ3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

Table 1-36. R40 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LOR_PH3_MASK	R/W	0x0	Masks Loss of Active Reference - Phase - DPLL3. When LOR_PH3_MASK is 1 then the LOR_PH3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.35 R41 (Offset = 0x29)

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Table 1-37. R41 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	LOL_PLL1_POL	R/W	0x0	LOL_PLL1 Flag Polarity. When LOL_PLL1_POL = 1,LOL_PLL1 = 0 results in LOL_PLL1_INTR = 1. When LOL_PLL1_POL = 0, LOL_PLL1 = 1 results in LOL_PLL1_INTR = 1. ROM=Y, EEPROM=N
2	LOL_PLL2_POL	R/W	0x0	LOL_PLL2 Flag Polarity. When LOL_PLL2_POL = 1,LOL_PLL2 = 0 results in LOL_PLL2_INTR = 1. When LOL_PLL2_POL = 0, LOL_PLL2 = 1 results in LOL_PLL2_INTR = 1. ROM=Y, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	LOS_FDET_XO_POL	R/W	0x0	LOS_FDET_XO Flag Polarity. When LOS_FDET_XO_POL = 1, LOS_FDET_XO = 0 results in LOS_FDET_XO_INTR = 1. When LOS_FDET_XO_POL = 0, LOS_FDET_XO = 1 results in LOS_FDET_XO_INTR = 1. ROM=Y, EEPROM=N

1.36 R42 (Offset = 0x2A)

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Table 1-38. R42 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_POL	R/W	0x0	LOPL_DPLL1 Flag Polarity. When LOPL_DPLL1_POL = 1, LOPL_DPLL1 = 0 results in LOPL_DPLL1_INTR = 1. When LOPL_DPLL1_POL = 0, LOPL_DPLL1 = 1 results in LOPL_DPLL1_INTR = 1. ROM=Y, EEPROM=N
6	LOFL_DPLL1_POL	R/W	0x0	LOFL_DPLL1 Flag Polarity. When LOFL_DPLL1_POL = 1, LOFL_DPLL1 = 0 results in LOFL_DPLL1_INTR = 1. When LOFL_DPLL1_POL = 0, LOFL_DPLL1 = 1 results in LOFL_DPLL1_INTR = 1. ROM=Y, EEPROM=N

Table 1-38. R42 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	HIST1_POL	R/W	0x0	HIST1 Flag Polarity. When HIST1_POL = 1, HIST1 = 0 results in HIST1_INTR = 1. When HIST1_POL = 0, HIST1 = 1 results in HIST1_INTR = 1. ROM=Y, EEPROM=N
4	HLDOVR1_POL	R/W	0x0	HLDOVR1 Flag Polarity. When HLDOVR1_POL = 1, HLDOVR1 = 0 results in HLDOVR1_INTR = 1. When HLDOVR1_POL = 0, HLDOVR1 = 1 results in HLDOVR1_INTR = 1. ROM=Y, EEPROM=N
3	REFSWITCH1_POL	R/W	0x0	REFSWITCH1 Flag Polarity. When REFSWITCH1_POL = 1, REFSWITCH1 = 0 results in REFSWITCH1_INTR = 1. When REFSWITCH1_POL = 0, REFSWITCH1 = 1 results in REFSWITCH1_INTR = 1. ROM=Y, EEPROM=N
2	LOR_MISSCLK1_POL	R/W	0x0	LOR_MISSCLK1 Flag Polarity. When LOR_MISSCLK1_POL = 1, LOR_MISSCLK1 = 0 results in LOR_MISSCLK1_INTR = 1. When LOR_MISSCLK1_POL = 0, LOR_MISSCLK1 = 1 results in LOR_MISSCLK1_INTR = 1. ROM=Y, EEPROM=N
1	LOR_FREQ1_POL	R/W	0x0	LOR_FREQ1 Flag Polarity. When LOR_FREQ1_POL = 1, LOR_FREQ1 = 0 results in LOR_FREQ1_INTR = 1. When LOR_FREQ1_POL = 0, LOR_FREQ1 = 1 results in LOR_FREQ1_INTR = 1. ROM=Y, EEPROM=N
0	LOR_PH1_POL	R/W	0x0	LOR_PH1 Flag Polarity. When LOR_PH1_POL = 1, LOR_PH1 = 0 results in LOR_PH1_INTR = 1. When LOR_PH1_POL = 0, LOR_PH1 = 1 results in LOR_PH1_INTR = 1. ROM=Y, EEPROM=N

1.37 R43 (Offset = 0x2B)

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Table 1-39. R43 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_POL	R/W	0x0	LOPL_DPLL2 Flag Polarity. When LOPL_DPLL2_POL = 1, LOPL_DPLL2 = 0 results in LOPL_DPLL2_INTR = 1. When LOPL_DPLL2_POL = 0, LOPL_DPLL2 = 1 results in LOPL_DPLL2_INTR = 1. ROM=Y, EEPROM=N
6	LOFL_DPLL2_POL	R/W	0x0	LOFL_DPLL2 Flag Polarity. When LOFL_DPLL2_POL = 1, LOFL_DPLL2 = 0 results in LOFL_DPLL2_INTR = 1. When LOFL_DPLL2_POL = 0, LOFL_DPLL2 = 1 results in LOFL_DPLL2_INTR = 1. ROM=Y, EEPROM=N
5	HIST2_POL	R/W	0x0	HIST2 Flag Polarity. When HIST2_POL = 1, HIST2 = 0 results in HIST2_INTR = 1. When HIST2_POL = 0, HIST2 = 1 results in HIST2_INTR = 1. ROM=Y, EEPROM=N

Table 1-39. R43 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	HLDOVR2_POL	R/W	0x0	HLDOVR2 Flag Polarity. When HLDOVR2_POL = 1, HLDOVR2 = 0 results in HLDOVR2_INTR = 1. When HLDOVR2_POL = 0, HLDOVR2 = 1 results in HLDOVR2_INTR = 1. ROM=Y, EEPROM=N
3	REFSWITCH2_POL	R/W	0x0	REFSWITCH2 Flag Polarity. When REFSWITCH2_POL = 1, REFSWITCH2 = 0 results in REFSWITCH2_INTR = 1. When REFSWITCH2_POL = 0, REFSWITCH2 = 1 results in REFSWITCH2_INTR = 1. ROM=Y, EEPROM=N
2	LOR_MISSCLK2_POL	R/W	0x0	LOR_MISSCLK2 Flag Polarity. When LOR_MISSCLK2_POL = 1, LOR_MISSCLK2 = 0 results in LOR_MISSCLK2_INTR = 1. When LOR_MISSCLK2_POL = 0, LOR_MISSCLK2 = 1 results in LOR_MISSCLK2_INTR = 1. ROM=Y, EEPROM=N
1	LOR_FREQ2_POL	R/W	0x0	LOR_FREQ2 Flag Polarity. When LOR_FREQ2_POL = 1, LOR_FREQ2 = 0 results in LOR_FREQ2_INTR = 1. When LOR_FREQ2_POL = 0, LOR_FREQ2 = 1 results in LOR_FREQ2_INTR = 1. ROM=Y, EEPROM=N
0	LOR_PH2_POL	R/W	0x0	LOR_PH2 Flag Polarity. When LOR_PH2_POL = 1, LOR_PH2 = 0 results in LOR_PH2_INTR = 1. When LOR_PH2_POL = 0, LOR_PH2 = 1 results in LOR_PH2_INTR = 1. ROM=Y, EEPROM=N

1.38 R44 (Offset = 0x2C)

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Table 1-40. R44 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL3_POL	R/W	0x0	LOPL_DPLL3 Flag Polarity. When LOPL_DPLL3_POL = 1, LOPL_DPLL3 = 0 results in LOPL_DPLL3_INTR = 1. When LOPL_DPLL3_POL = 0, LOPL_DPLL3 = 1 results in LOPL_DPLL3_INTR = 1. ROM=Y, EEPROM=N
6	LOFL_DPLL3_POL	R/W	0x0	LOFL_DPLL3 Flag Polarity. When LOFL_DPLL3_POL = 1, LOFL_DPLL3 = 0 results in LOFL_DPLL3_INTR = 1. When LOFL_DPLL3_POL = 0, LOFL_DPLL3 = 1 results in LOFL_DPLL3_INTR = 1. ROM=Y, EEPROM=N
5	HIST3_POL	R/W	0x0	HIST3 Flag Polarity. When HIST3_POL = 1, HIST3 = 0 results in HIST3_INTR = 1. When HIST3_POL = 0, HIST3 = 1 results in HIST3_INTR = 1 ROM=Y, EEPROM=N
4	HLDOVR3_POL	R/W	0x0	HLDOVR3 Flag Polarity. When HLDOVR3_POL = 1, HLDOVR3 = 0 results in HLDOVR3_INTR = 1. When HLDOVR3_POL = 0, HLDOVR3 = 1 results in HLDOVR3_INTR = 1. ROM=Y, EEPROM=N

Table 1-40. R44 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	REFSWITCH3_POL	R/W	0x0	REFSWITCH3 Flag Polarity. When REFSWITCH3_POL = 1, REFSWITCH3 = 0 results in REFSWITCH3_INTR = 1. When REFSWITCH3_POL = 0, REFSWITCH3 = 1 results in REFSWITCH3_INTR = 1. ROM=Y, EEPROM=N
2	LOR_MISSCLK3_POL	R/W	0x0	LOR_MISSCLK3 Flag Polarity. When LOR_MISSCLK3_POL = 1, LOR_MISSCLK3 = 0 results in LOR_MISSCLK3_INTR = 1. When LOR_MISSCLK3_POL = 0, LOR_MISSCLK3 = 1 results in LOR_MISSCLK3_INTR = 1. ROM=Y, EEPROM=N
1	LOR_FREQ3_POL	R/W	0x0	LOR_FREQ3 Flag Polarity. When LOR_FREQ3_POL = 1, LOR_FREQ3 = 0 results in LOR_FREQ3_INTR = 1. When LOR_FREQ3_POL = 0, LOR_FREQ3 = 1 results in LOR_FREQ3_INTR = 1. ROM=Y, EEPROM=N
0	LOR_PH3_POL	R/W	0x0	LOR_PH3 Flag Polarity. When LOR_PH3_POL = 1, LOR_PH3 = 0 results in LOR_PH3_INTR = 1. When LOR_PH3_POL = 0, LOR_PH3 = 1 results in LOR_PH3_INTR = 1. ROM=Y, EEPROM=N

1.39 R45 (Offset = 0x2D)

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Table 1-41. R45 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	LOL_PLL1_INTR	R	0x1	LOL_PLL1 Interrupt. The LOL_PLL1_INTR bit is set when a level of the correct polarity is detected on the LOL_PLL1 interrupt source. The LOL_PLL1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
2	LOL_PLL2_INTR	R	0x1	LOL_PLL2 Interrupt. The LOL_PLL2_INTR bit is set when a level of the correct polarity is detected on the LOL_PLL2 interrupt source. The LOL_PLL2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	LOS_FDET_XO_INTR	R	0x1	LOL_FDET_XO Interrupt. The LOL_FDET_XO_INTR bit is set when a level of the correct polarity is detected on the LOL_FDET_XO interrupt source. The LOL_FDET_XO_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.40 R46 (Offset = 0x2E)

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Table 1-42. R46 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_INTR	R	0x1	LOPL_DPLL1 Interrupt. The LOPL_DPLL1_INTR bit is set when a level of the correct polarity is detected on the LOPL_DPLL1 interrupt source. The LOPL_DPLL1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
6	LOFL_DPLL1_INTR	R	0x1	LOFL_DPLL1 Interrupt. The LOFL_DPLL1_INTR bit is set when a level of the correct polarity is detected on the LOFL_DPLL1 interrupt source. The LOFL_DPLL1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
5	HIST1_INTR	R	0x0	HIST1 Interrupt. The HIST1_INTR bit is set when a level of the correct polarity is detected on the HIST1 interrupt source. The HIST1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
4	HLDOVR1_INTR	R	0x1	HLDOVR1 Interrupt. The HLDOVR1_INTR bit is set when a level of the correct polarity is detected on the HLDOVR1 interrupt source. The HLDOVR1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
3	REFSWITCH1_INTR	R	0x0	REFSWITCH1 Interrupt. The REFSWITCH1_INTR bit is set when a level of the correct polarity is detected on the REFSWITCH1 interrupt source. The REFSWITCH1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
2	LOR_MISSCLK1_INTR	R	0x0	LOR_MISSCLK1 Interrupt. The LOR_MISSCLK1_INTR bit is set when a level of the correct polarity is detected on the LOR_MISSCLK1 interrupt source. The LOR_MISSCLK1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	LOR_FREQ1_INTR	R	0x0	LOR_FREQ1 Interrupt. The LOR_FREQ1_INTR bit is set when a level of the correct polarity is detected on the LOR_FREQ1 interrupt source. The LOR_FREQ1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
0	LOR_PH1_INTR	R	0x0	LOR_PH1 Interrupt. The LOR_PH1_INTR bit is set when a level of the correct polarity is detected on the LOR_PH1 interrupt source. The LOR_PH1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.41 R47 (Offset = 0x2F)

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Table 1-43. R47 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_INTR	R	0x1	LOPL_DPLL2 Interrupt. The LOPL_DPLL2_INTR bit is set when a level of the correct polarity is detected on the LOPL_DPLL2 interrupt source. The LOPL_DPLL2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

Table 1-43. R47 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	LOFL_DPLL2_INTR	R	0x1	LOFL_DPLL2 Interrupt. The LOFL_DPLL2_INTR bit is set when a level of the correct polarity is detected on the LOFL_DPLL2 interrupt source. The LOFL_DPLL2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
5	HIST2_INTR	R	0x1	HIST2 Interrupt. The HIST2_INTR bit is set when a level of the correct polarity is detected on the HIST2 interrupt source. The HIST2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
4	HLDOVR2_INTR	R	0x1	HLDOVR2 Interrupt. The HLDOVR2_INTR bit is set when a level of the correct polarity is detected on the HLDOVR2 interrupt source. The HLDOVR2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
3	REFSWITCH2_INTR	R	0x1	REFSWITCH2 Interrupt. The REFSWITCH2_INTR bit is set when a level of the correct polarity is detected on the REFSWITCH2 interrupt source. The REFSWITCH2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
2	LOR_MISSCLK2_INTR	R	0x0	LOR_MISSCLK2 Interrupt. The LOR_MISSCLK2_INTR bit is set when a level of the correct polarity is detected on the LOR_MISSCLK2 interrupt source. The LOR_MISSCLK2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	LOR_FREQ2_INTR	R	0x0	LOR_FREQ2 Interrupt. The LOR_FREQ2_INTR bit is set when a level of the correct polarity is detected on the LOR_FREQ2 interrupt source. The LOR_FREQ2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
0	LOR_PH2_INTR	R	0x0	LOR_PH2 Interrupt. The LOR_PH2_INTR bit is set when a level of the correct polarity is detected on the LOR_PH2 interrupt source. The LOR_PH2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.42 R48 (Offset = 0x30)

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Table 1-44. R48 Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL3_INTR	R	0x1	LOPL_DPLL3 Interrupt. The LOPL_DPLL3_INTR bit is set when a level of the correct polarity is detected on the LOPL_DPLL3 interrupt source. The LOPL_DPLL3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
6	LOFL_DPLL3_INTR	R	0x1	LOFL_DPLL3 Interrupt. The LOFL_DPLL3_INTR bit is set when a level of the correct polarity is detected on the LOFL_DPLL3 interrupt source. The LOFL_DPLL3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

Table 1-44. R48 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	HIST3_INTR	R	0x0	HIST3 Interrupt. The HIST3_INTR bit is set when a level of the correct polarity is detected on the HIST3 interrupt source. The HIST3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
4	HLDOVR3_INTR	R	0x1	HLDOVR3 Interrupt. The HLDOVR3_INTR bit is set when a level of the correct polarity is detected on the HLDOVR3 interrupt source. The HLDOVR3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
3	REFSWITCH3_INTR	R	0x1	REFSWITCH3 Interrupt. The REFSWITCH3_INTR bit is set when a level of the correct polarity is detected on the REFSWITCH3 interrupt source. The REFSWITCH3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
2	LOR_MISSCLK3_INTR	R	0x0	LOR_MISSCLK3 Interrupt. The LOR_MISSCLK3_INTR bit is set when a level of the correct polarity is detected on the LOR_MISSCLK3 interrupt source. The LOR_MISSCLK3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	LOR_FREQ3_INTR	R	0x0	LOR_FREQ3 Interrupt. The LOR_FREQ3_INTR bit is set when a level of the correct polarity is detected on the LOR_FREQ3 interrupt source. The LOR_FREQ3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
0	LOR_PH3_INTR	R	0x0	LOR_PH3 Interrupt. The LOR_PH3_INTR bit is set when a level of the correct polarity is detected on the LOR_PH3 interrupt source. The LOR_PH3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.43 R49 (Offset = 0x31)

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Table 1-45. R49 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	INT_LATCH_OR_LIVE	R/W	0x0	ROM=Y, EEPROM=N 0x0 = Latch Mode 0x1 = Live Mode
2	INT_AND_OR	R/W	0x0	Interrupt AND/OR Combination. If INT_AND_OR is 1, then the interrupts are combined in an AND structure, in which case ALL un-masked interrupt flags must be active in order to generate the interrupt. If INT_AND_OR is 0, then the interrupts are combined in an OR structure, in which case ANY un-masked interrupt flags can generate the interrupt. ROM=Y, EEPROM=N 0x0 = OR 0x1 = AND

Table 1-45. R49 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_EN	R/W	0x1	Interrupt Enable. If INT_EN is 1 then the interrupt circuit is enabled. If INT_EN is 0 the interrupt circuit is disabled. When INT_EN is 0, interrupts cannot be signaled on the GPIOx pins, and the flag registers (*_INTR) will not be updated; however, the live status registers will still reflect the current state of the internal interrupt source signals. To provide an interrupt on a pin, a GPIOx pin must also be configured as interrupt output. Interrupts may be enabled without providing a GPIOx output to allow sticky bits to be set. ROM=Y, EEPROM=N
0	INT_CLR	R/WSC	0x0	Clears all interrupt flag (*_INTR) registers ROM=N, EEPROM=N

1.44 R50 (Offset = 0x32)

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Table 1-46. R50 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	REF3_VALID_STATUS	R	0x0	Status of Reference Input Validation for IN3 ROM=N, EEPROM=N
2	REF2_VALID_STATUS	R	0x0	Status of Reference Input Validation for IN2 ROM=N, EEPROM=N
1	REF1_VALID_STATUS	R	0x0	Status of Reference Input Validation for IN1 ROM=N, EEPROM=N
0	REF0_VALID_STATUS	R	0x0	Status of Reference Input Validation for IN0 ROM=N, EEPROM=N

1.45 R51 (Offset = 0x33)

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Table 1-47. R51 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF3_PH_STATUS	R	0x0	Status of Reference 3 Phase Validation ROM=N, EEPROM=N
4	RESERVED	R	0x0	Reserved
3	REF3_FDET_STATUS	R	0x0	Status of Reference 3 Frequency Validation ROM=N, EEPROM=N
2	REF2_PH_STATUS	R	0x0	Status of Reference 2 Phase Validation ROM=N, EEPROM=N

Table 1-47. R51 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RESERVED	R	0x0	Reserved
0	REF2_FDET_STATUS	R	0x0	Status of Reference 2 Frequency Validation ROM=N, EEPROM=N

1.46 R52 (Offset = 0x34)

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Table 1-48. R52 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF1_PH_STATUS	R	0x0	Status of Reference 1 Phase Validation ROM=N, EEPROM=N
4	RESERVED	R	0x0	Reserved
3	REF1_FDET_STATUS	R	0x0	Status of Reference 1 Frequency Validation ROM=N, EEPROM=N
2	REF0_PH_STATUS	R	0x0	Status of Reference 0 Phase Validation ROM=N, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	REF0_FDET_STATUS	R	0x0	Status of Reference 0 Frequency Validation ROM=N, EEPROM=N

1.47 R53 (Offset = 0x35)

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Table 1-49. R53 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	TEC_CNTR_HELD	R	0x0	TEC Held. Reading back a 1 indicates GPIO or SPI event has latched a holdover value. Will clear to 0 after TEC CNTR LSB is read. ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.48 R54 (Offset = 0x36)

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Table 1-50. R54 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO0_IN_FLT_EN	R/W	0x0	Enable GPIO0 Input Pin Deglitch Filter ROM=Y, EEPROM=N

Table 1-50. R54 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	GPIO0_MODE	R/W	0x0	Select GPIO0 Pin Operating Mode. ROM=Y, EEPROM=N 0x0 = STATUS or INT, Acts as status or interrupt outputs (See section on STATUS/INTERRUPT) 0x1 = INSEL01_DPLL1, Selects input 0 or input 1 for DPLL1 0x2 = INSEL01_DPLL2, Selects input 0 or input 1 for DPLL2 0x3 = INSEL01_DPLL3, Selects input 0 or input 1 for DPLL3 0x4 = INSEL23_DPLL1, Selects input 2 or input 3 for DPLL1 0x5 = INSEL23_DPLL2, Selects input 2 or input 3 for DPLL2 0x6 = INSEL23_DPLL3, Selects input 2 or input 3 for DPLL3 0x7 = Reserved 0x8 = Reserved 0x9 = Reserved 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = INSEL12_DPLL1, Selects input 1 or input 2 for DPLL1 0xE = INSEL12_DPLL2, Selects input 1 or input 2 for DPLL2 0xF = INSEL12_DPLL3, Selects input 1 or input 2 for DPLL3 0x10 = INSEL03_DPLL1, Selects input 0 or input 3 for DPLL1 0x11 = INSEL03_DPLL2, Selects input 0 or input 3 for DPLL2 0x12 = INSEL03_DPLL3, Selects input 0 or input 3 for DPLL3 0x13 = INSEL02_DPLL1, Selects input 0 or input 2 for DPLL1 0x14 = INSEL02_DPLL2, Selects input 0 or input 2 for DPLL2 0x15 = INSEL02_DPLL3, Selects input 0 or input 2 for DPLL3 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = INSEL13_DPLL1, Selects input 1 or input 3 for DPLL1 0x1A = INSEL13_DPLL2, Selects input 1 or input 3 for DPLL2 0x1B = INSEL13_DPLL3, Selects input 1 or input 3 for DPLL3 0x1C = Reserved 0x1D = Reserved 0x1E = Reserved 0x1F = SYNC, Synchronizes selected outputs on a low-to-high pulse. "1" is normal state for outputs. "0" sets outputs in SYNC. 0x20 = SYSREF_REQ, Can request SYSREF pulses on appropriate output channels via low-to-high pulse. 0x21 = FDEV_TRIG_DPLL1, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL1 0x22 = FDEV_TRIG_DPLL2, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL2 0x23 = FDEV_TRIG_DPLL3, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL3 0x24 = FDEV_DIR_DPLL1, FDEV_DIR_DPLL1 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive 0x25 = FDEV_DIR_DPLL2, FDEV_DIR_DPLL2 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive

Table 1-50. R54 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x26 = FDEV_DIR_DPLL3, FDEV_DIR_DPLL3 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive 0x27 = TEC_TRIG_SEL

1.49 R55 (Offset = 0x37)

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Table 1-51. R55 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO1_IN_FLT_EN	R/W	0x0	Enable GPIO1 Input Pin Deglitch Filter ROM=Y, EEPROM=N

Table 1-51. R55 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	GPIO1_MODE	R/W	0x0	Select GPIO1 Pin Operating Mode. ROM=Y, EEPROM=N 0x0 = STATUS or INT, Acts as status or interrupt outputs (See section on STATUS/ INTERRUPT) 0x1 = INSEL01_DPLL1, Selects input 0 or input 1 for DPLL1 0x2 = INSEL01_DPLL2, Selects input 0 or input 1 for DPLL2 0x3 = INSEL01_DPLL3, Selects input 0 or input 1 for DPLL3 0x4 = INSEL23_DPLL1, Selects input 2 or input 3 for DPLL1 0x5 = INSEL23_DPLL2, Selects input 2 or input 3 for DPLL2 0x6 = INSEL23_DPLL3, Selects input 2 or input 3 for DPLL3 0x7 = Reserved 0x8 = Reserved 0x9 = Reserved 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = INSEL12_DPLL1, Selects input 1 or input 2 for DPLL1 0xE = INSEL12_DPLL2, Selects input 1 or input 2 for DPLL2 0xF = INSEL12_DPLL3, Selects input 1 or input 2 for DPLL3 0x10 = INSEL03_DPLL1, Selects input 0 or input 3 for DPLL1 0x11 = INSEL03_DPLL2, Selects input 0 or input 3 for DPLL2 0x12 = INSEL03_DPLL3, Selects input 0 or input 3 for DPLL3 0x13 = INSEL02_DPLL1, Selects input 0 or input 2 for DPLL1 0x14 = INSEL02_DPLL2, Selects input 0 or input 2 for DPLL2 0x15 = INSEL02_DPLL3, Selects input 0 or input 2 for DPLL3 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = INSEL13_DPLL1, Selects input 1 or input 3 for DPLL1 0x1A = INSEL13_DPLL2, Selects input 1 or input 3 for DPLL2 0x1B = INSEL13_DPLL3, Selects input 1 or input 3 for DPLL3 0x1C = Reserved 0x1D = Reserved 0x1E = Reserved 0x1F = SYNC, Synchronizes selected outputs on a low-to-high pulse. "1" is normal state for outputs. "0" sets outputs in SYNC. 0x20 = SYSREF_REQ, Can request SYSREF pulses on appropriate output channels via low-to-high pulse. 0x21 = FDEV_TRIG_DPLL1, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL1 0x22 = FDEV_TRIG_DPLL2, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL2 0x23 = FDEV_TRIG_DPLL3, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL3 0x24 = FDEV_DIR_DPLL1, FDEV_DIR_DPLL1 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive 0x25 = FDEV_DIR_DPLL2, FDEV_DIR_DPLL2 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive

Table 1-51. R55 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x26 = FDEV_DIR_DPLL3, FDEV_DIR_DPLL3 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive 0x27 = TEC_TRIG_SEL

1.50 R56 (Offset = 0x38)

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Table 1-52. R56 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO2_IN_FLT_EN	R/W	0x0	Enable GPIO2 Input Pin Deglitch Filter ROM=Y, EEPROM=N

Table 1-52. R56 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	GPIO2_MODE	R/W	0x0	Select GPIO2 Pin Operating Mode. ROM=Y, EEPROM=N 0x0 = STATUS or INT, Acts as status or interrupt outputs (See section on STATUS/ INTERRUPT) 0x1 = INSEL01_DPLL1, Selects input 0 or input 1 for DPLL1 0x2 = INSEL01_DPLL2, Selects input 0 or input 1 for DPLL2 0x3 = INSEL01_DPLL3, Selects input 0 or input 1 for DPLL3 0x4 = INSEL23_DPLL1, Selects input 2 or input 3 for DPLL1 0x5 = INSEL23_DPLL2, Selects input 2 or input 3 for DPLL2 0x6 = INSEL23_DPLL3, Selects input 2 or input 3 for DPLL3 0x7 = Reserved 0x8 = Reserved 0x9 = Reserved 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = INSEL12_DPLL1, Selects input 1 or input 2 for DPLL1 0xE = INSEL12_DPLL2, Selects input 1 or input 2 for DPLL2 0xF = INSEL12_DPLL3, Selects input 1 or input 2 for DPLL3 0x10 = INSEL03_DPLL1, Selects input 0 or input 3 for DPLL1 0x11 = INSEL03_DPLL2, Selects input 0 or input 3 for DPLL2 0x12 = INSEL03_DPLL3, Selects input 0 or input 3 for DPLL3 0x13 = INSEL02_DPLL1, Selects input 0 or input 2 for DPLL1 0x14 = INSEL02_DPLL2, Selects input 0 or input 2 for DPLL2 0x15 = INSEL02_DPLL3, Selects input 0 or input 2 for DPLL3 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = INSEL13_DPLL1, Selects input 1 or input 3 for DPLL1 0x1A = INSEL13_DPLL2, Selects input 1 or input 3 for DPLL2 0x1B = INSEL13_DPLL3, Selects input 1 or input 3 for DPLL3 0x1C = Reserved 0x1D = Reserved 0x1E = Reserved 0x1F = SYNC, Synchronizes selected outputs on a low-to-high pulse. "1" is normal state for outputs. "0" sets outputs in SYNC. 0x20 = SYSREF_REQ, Can request SYSREF pulses on appropriate output channels via low-to-high pulse. 0x21 = FDEV_TRIG_DPLL1, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL1 0x22 = FDEV_TRIG_DPLL2, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL2 0x23 = FDEV_TRIG_DPLL3, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL3 0x24 = FDEV_DIR_DPLL1, FDEV_DIR_DPLL1 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive 0x25 = FDEV_DIR_DPLL2, FDEV_DIR_DPLL2 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive

Table 1-52. R56 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x26 = FDEV_DIR_DPLL3, FDEV_DIR_DPLL3 will determine the direction of the FDEV trigger. 0 = Negative and 1 = Positive 0x27 = TEC_TRIG_SEL

1.51 R57 (Offset = 0x39)

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Table 1-53. R57 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-53. R57 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	GPIO0_SEL	R/W	0x2	GPIO0 Status Signal Select. ROM=Y, EEPROM=N 0x0 = XO Loss of Signal (LOS) 0x1 = APLL1 Loss of Lock (LOL) 0x2 = APLL2 Loss of Lock (LOL) 0x3 = APLL3 Loss of Lock (LOL) 0x4 = DPLL1 Loss of Phase Lock (LOPL) 0x5 = DPLL1 Loss of Frequency Lock (LOFL) 0x6 = PLL1 LOL | DPLL1 LOPL | DPLL1 LOFL 0x7 = DPLL2 Loss of Phase Lock (LOPL) 0x8 = DPLL2 Loss of Frequency Lock (LOFL) 0x9 = PLL2 LOL | DPLL2 LOPL | DPLL2 LOFL 0xA = DPLL3 Loss of Phase Lock (LOPL) 0xB = DPLL3 Loss of Frequency Lock (LOFL) 0xC = PLL3 LOL | DPLL3 LOPL | DPLL3 LOFL 0xD = DPLL1 | DPLL2 | DPLL3 LOL 0xE = Interrupt (INTR). Derived from INT_FLAG register bits. 0xF = SPI Readback Data (SDO) 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = DPLL1 REF0 Selected 0x16 = DPLL1 REF1 Selected 0x17 = DPLL1 REF2 Selected 0x18 = DPLL1 REF3 Selected 0x19 = Reserved 0x1A = DPLL1 Holdover Active 0x1B = DPLL2 REF0 Selected 0x1C = DPLL2 REF1 Selected 0x1D = DPLL2 REF2 Selected 0x1E = DPLL2 REF3 Selected 0x1F = Reserved 0x20 = DPLL2 Holdover Active 0x21 = DPLL3 REF0 Selected 0x22 = DPLL3 REF1 Selected 0x23 = DPLL3 REF2 Selected 0x24 = DPLL3 REF3 Selected 0x25 = Reserved 0x26 = DPLL3 Holdover Active 0x27 = REF0 Frequency Monitor 0x28 = REF1 Frequency Monitor 0x29 = REF2 Frequency Monitor 0x2A = REF3 Frequency Monitor 0x2B = Reserved 0x2C = REF0 Missing Clock Monitor 0x2D = REF1 Missing Clock Monitor 0x2E = REF2 Missing Clock Monitor

Table 1-53. R57 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = REF3 Missing Clock Monitor 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = REF0 Phase Validation Monitor 0x3C = REF1 Phase Validation Monitor 0x3D = REF2 Phase Validation Monitor 0x3E = REF3 Phase Validation Monitor 0x3F = Reserved 0x40 = Reserved 0x41 = Reserved 0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = Reserved 0x47 = Reserved 0x48 = Reserved 0x49 = Reserved 0x4A = Reserved 0x4B = Reserved 0x4C = Reserved 0x4D = Reserved 0x4E = Reserved 0x4F = Reserved 0x50 = PLL1 N-Divider Divided By 2 0x51 = PLL2 N-Divider Divided By 2 0x52 = PLL3 N-Divider Divided By 2 0x53 = PLL1 R-Divider Divided By 2 0x54 = PLL2 R-Divider Divided By 2 0x55 = PLL3 R-Divider Divided By 2 0x56 = Reserved 0x57 = Reserved 0x58 = Reserved 0x59 = REF0 Monitor Divider Output Divided By 2 / REFx_DET_CLK_DIV 0x5A = REF1 Monitor Divider Output Divided By 2 / REFx_DET_CLK_DIV 0x5B = REF2 Monitor Divider Output Divided By 2 / REFx_DET_CLK_DIV 0x5C = REF3 Monitor Divider Output Divided By 2 / REFx_DET_CLK_DIV 0x5D = Reserved 0x5E = TDC1 R-Divider Divided By 2 0x5F = Reserved

Table 1-53. R57 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = TDC1 FB-Divider Divided By 2 0x61 = TDC2 R-Divider Divided By 2 0x62 = Reserved 0x63 = TDC2 FB-Divider Divided By 2 0x64 = TDC3 R-Divider Divided By 2 0x65 = Reserved 0x66 = TDC3 FB-Divider Divided By 2 0x67 = Reserved 0x68 = Reserved 0x69 = Reserved 0x6A = Reserved 0x6B = Reserved 0x6C = Reserved 0x6D = Reserved 0x6E = Reserved 0x6F = Reserved 0x70 = Reserved 0x71 = Reserved 0x72 = Reserved

1.52 R58 (Offset = 0x3A)

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Table 1-54. R58 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-54. R58 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	GPIO1_SEL	R/W	0xF	GPIO1 Status Signal Select. ROM=Y, EEPROM=N 0x0 = XO Loss of Signal (LOS) 0x1 = APLL1 Loss of Lock (LOL) 0x2 = APLL2 Loss of Lock (LOL) 0x3 = APLL3 Loss of Lock (LOL) 0x4 = DPLL1 Loss of Phase Lock (LOPL) 0x5 = DPLL1 Loss of Frequency Lock (LOFL) 0x6 = PLL1 LOL | DPLL1 LOPL | DPLL1 LOFL 0x7 = DPLL2 Loss of Phase Lock (LOPL) 0x8 = DPLL2 Loss of Frequency Lock (LOFL) 0x9 = PLL2 LOL | DPLL2 LOPL | DPLL2 LOFL 0xA = DPLL3 Loss of Phase Lock (LOPL) 0xB = DPLL3 Loss of Frequency Lock (LOFL) 0xC = PLL3 LOL | DPLL3 LOPL | DPLL3 LOFL 0xD = DPLL1 | DPLL2 | DPLL3 LOL 0xE = Interrupt (INTR). Derived from INT_FLAG register bits. 0xF = SPI Readback Data (SDO) 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = DPLL1 REF0 Selected 0x16 = DPLL1 REF1 Selected 0x17 = DPLL1 REF2 Selected 0x18 = DPLL1 REF3 Selected 0x19 = Reserved 0x1A = DPLL1 Holdover Active 0x1B = DPLL2 REF0 Selected 0x1C = DPLL2 REF1 Selected 0x1D = DPLL2 REF2 Selected 0x1E = DPLL2 REF3 Selected 0x1F = Reserved 0x20 = DPLL2 Holdover Active 0x21 = DPLL3 REF0 Selected 0x22 = DPLL3 REF1 Selected 0x23 = DPLL3 REF2 Selected 0x24 = DPLL3 REF3 Selected 0x25 = Reserved 0x26 = DPLL3 Holdover Active 0x27 = REF0 Frequency Monitor 0x28 = REF1 Frequency Monitor 0x29 = REF2 Frequency Monitor 0x2A = REF3 Frequency Monitor 0x2B = Reserved 0x2C = REF0 Missing Clock Monitor 0x2D = REF1 Missing Clock Monitor 0x2E = REF2 Missing Clock Monitor

Table 1-54. R58 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = REF3 Missing Clock Monitor 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = REF0 Phase Validation Monitor 0x3C = REF1 Phase Validation Monitor 0x3D = REF2 Phase Validation Monitor 0x3E = REF3 Phase Validation Monitor 0x3F = Reserved 0x40 = Reserved 0x41 = Reserved 0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = Reserved 0x47 = Reserved 0x48 = Reserved 0x49 = Reserved 0x4A = Reserved 0x4B = Reserved 0x4C = Reserved 0x4D = Reserved 0x4E = Reserved 0x4F = Reserved 0x50 = PLL1 N-Divider Divided By 2 0x51 = PLL2 N-Divider Divided By 2 0x52 = PLL3 N-Divider Divided By 2 0x53 = PLL1 R-Divider Divided By 2 0x54 = PLL2 R-Divider Divided By 2 0x55 = PLL3 R-Divider Divided By 2 0x56 = Reserved 0x57 = Reserved 0x58 = Reserved 0x59 = REF0 Monitor Divider Output Divided By 2 / REFx_DET_CLK_DIV 0x5A = REF1 Monitor Divider Output Divided By 2 / REFx_DET_CLK_DIV 0x5B = REF2 Monitor Divider Output Divided By 2 / REFx_DET_CLK_DIV 0x5C = REF3 Monitor Divider Output Divided By 2 / REFx_DET_CLK_DIV 0x5D = Reserved 0x5E = TDC1 R-Divider Divided By 2 0x5F = Reserved

Table 1-54. R58 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = TDC1 FB-Divider Divided By 2 0x61 = TDC2 R-Divider Divided By 2 0x62 = Reserved 0x63 = TDC2 FB-Divider Divided By 2 0x64 = TDC3 R-Divider Divided By 2 0x65 = Reserved 0x66 = TDC3 FB-Divider Divided By 2 0x67 = Reserved 0x68 = Reserved 0x69 = Reserved 0x6A = Reserved 0x6B = Reserved 0x6C = Reserved 0x6D = Reserved 0x6E = Reserved 0x6F = Reserved 0x70 = Reserved 0x71 = Reserved 0x72 = Reserved 0x73 = Continuous SYSREF / 1-PPS from selected SYSREF DIV

1.53 R59 (Offset = 0x3B)

Return to the Summary Table.

Table 1-55. R59 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-55. R59 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	GPIO2_SEL	R/W	0xE	GPIO2 Status Signal Select. ROM=Y, EEPROM=N 0x0 = XO Loss of Signal (LOS) 0x1 = APLL1 Loss of Lock (LOL) 0x2 = APLL2 Loss of Lock (LOL) 0x3 = APLL3 Loss of Lock (LOL) 0x4 = DPLL1 Loss of Phase Lock (LOPL) 0x5 = DPLL1 Loss of Frequency Lock (LOFL) 0x6 = PLL1 LOL | DPLL1 LOPL | DPLL1 LOFL 0x7 = DPLL2 Loss of Phase Lock (LOPL) 0x8 = DPLL2 Loss of Frequency Lock (LOFL) 0x9 = PLL2 LOL | DPLL2 LOPL | DPLL2 LOFL 0xA = DPLL3 Loss of Phase Lock (LOPL) 0xB = DPLL3 Loss of Frequency Lock (LOFL) 0xC = PLL3 LOL | DPLL3 LOPL | DPLL3 LOFL 0xD = DPLL1 | DPLL2 | DPLL3 LOL 0xE = Interrupt (INTR). Derived from INT_FLAG register bits. 0xF = SPI Readback Data (SDO) 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = DPLL1 REF0 Selected 0x16 = DPLL1 REF1 Selected 0x17 = DPLL1 REF2 Selected 0x18 = DPLL1 REF3 Selected 0x19 = Reserved 0x1A = DPLL1 Holdover Active 0x1B = DPLL2 REF0 Selected 0x1C = DPLL2 REF1 Selected 0x1D = DPLL2 REF2 Selected 0x1E = DPLL2 REF3 Selected 0x1F = Reserved 0x20 = DPLL2 Holdover Active 0x21 = DPLL3 REF0 Selected 0x22 = DPLL3 REF1 Selected 0x23 = DPLL3 REF2 Selected 0x24 = DPLL3 REF3 Selected 0x25 = Reserved 0x26 = DPLL3 Holdover Active 0x27 = REF0 Frequency Monitor 0x28 = REF1 Frequency Monitor 0x29 = REF2 Frequency Monitor 0x2A = REF3 Frequency Monitor 0x2B = Reserved 0x2C = REF0 Missing Clock Monitor 0x2D = REF1 Missing Clock Monitor 0x2E = REF2 Missing Clock Monitor

Table 1-55. R59 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = REF3 Missing Clock Monitor 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = REF0 Phase Validation Monitor 0x3C = REF1 Phase Validation Monitor 0x3D = REF2 Phase Validation Monitor 0x3E = REF3 Phase Validation Monitor 0x3F = Reserved 0x40 = Reserved 0x41 = Reserved 0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = Reserved 0x47 = Reserved 0x48 = Reserved 0x49 = Reserved 0x4A = Reserved 0x4B = Reserved 0x4C = Reserved 0x4D = Reserved 0x4E = Reserved 0x4F = Reserved 0x50 = PLL1 N-Divider Divided By 2 0x51 = PLL2 N-Divider Divided By 2 0x52 = PLL3 N-Divider Divided By 2 0x53 = PLL1 R-Divider Divided By 2 0x54 = PLL2 R-Divider Divided By 2 0x55 = PLL3 R-Divider Divided By 2 0x56 = Reserved 0x57 = Reserved 0x58 = Reserved 0x59 = REF0 Monitor Divider Output Divided By 2 / REFx_DET_CLK_DIV 0x5A = REF1 Monitor Divider Output Divided By 2 / REFx_DET_CLK_DIV 0x5B = REF2 Monitor Divider Output Divided By 2 / REFx_DET_CLK_DIV 0x5C = REF3 Monitor Divider Output Divided By 2 / REFx_DET_CLK_DIV 0x5D = Reserved 0x5E = TDC1 R-Divider Divided By 2 0x5F = Reserved

Table 1-55. R59 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = TDC1 FB-Divider Divided By 2 0x61 = TDC2 R-Divider Divided By 2 0x62 = Reserved 0x63 = TDC2 FB-Divider Divided By 2 0x64 = TDC3 R-Divider Divided By 2 0x65 = Reserved 0x66 = TDC3 FB-Divider Divided By 2 0x67 = Reserved 0x68 = Reserved 0x69 = Reserved 0x6A = Reserved 0x6B = Reserved 0x6C = Reserved 0x6D = Reserved 0x6E = Reserved 0x6F = Reserved 0x70 = Reserved 0x71 = Reserved 0x72 = Reserved 0x73 = Continuous SYSREF / 1-PPS from selected SYSREF DIV

1.54 R60 (Offset = 0x3C)

Return to the Summary Table.

Table 1-56. R60 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	GPIO0_OPEND	R/W	0x0	GPIO0 Open Drain Enable ROM=Y, EEPROM=N 0x0 = CMOS 0x1 = NMOS open drain. External pull-up from 1.8 V to 5.5 V supply rail required.
4	GPIO1_OPEND	R/W	0x1	GPIO1 Open Drain Enable ROM=Y, EEPROM=N 0x0 = CMOS 0x1 = NMOS open drain. External pull-up from 1.8 V to 5.5 V supply rail required.
3	GPIO2_OPEND	R/W	0x0	GPIO2 Open Drain Enable ROM=Y, EEPROM=N 0x0 = CMOS 0x1 = NMOS open drain. External pull-up from 1.8 V to 5.5 V supply rail required.

Table 1-56. R60 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	GPIO0_POL	R/W	0x1	GPIO0 Status Output Polarity. The GPIO0_STAT_POL bit defines the polarity of information presented on the GPIO0 output. If GPIO0_STAT_POL is set to 1, then GPIO0 is active high. If GPIO0_STAT_POL is 0, then GPIO0 is active low. ROM=Y, EEPROM=N 0x0 = Active High 0x1 = Active Low
1	GPIO1_POL	R/W	0x0	GPIO1 Status Output Polarity. The GPIO1_STAT_POL bit defines the polarity of information presented on the GPIO1 output. If GPIO1_STAT_POL is set to 1, then GPIO1 is active high. If GPIO1_STAT_POL is 0, then GPIO1 is active low. ROM=Y, EEPROM=N 0x0 = Active High 0x1 = Active Low
0	GPIO2_POL	R/W	0x0	GPIO2 Status Output Polarity. The GPIO2_STAT_POL bit defines the polarity of information presented on the GPIO2 output. If GPIO2_STAT_POL is set to 1, then GPIO2 is active high. If GPIO2_STAT_POL is 0, then GPIO2 is active low. ROM=Y, EEPROM=N 0x0 = Active High 0x1 = Active Low

1.55 R61 (Offset = 0x3D)

Return to the Summary Table.

Table 1-57. R61 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	GPIO_SYSREF_SEL	R/W	0x0	Select SYSREF divider output for GPIO output. When GPIOx_SEL chooses SYSREF divider, this is the SYSREF divider output on the GPIO. This signal is continuous. This could be used for low frequency outputs such as 1-PPS or 8 kHz as a 3.3-V LVCMOS signal. Select SYSREF divider output after static digital delay but before the analog and digital delay and pulser. ROM=Y, EEPROM=N 0x0 = OUT_0_1 0x1 = OUT_4_5 0x2 = OUT_6_7 0x3 = OUT_8_9 0x4 = OUT_10_11 0x5 = OUT_12_13 0x6 = NA 0x7 = NA
1	MUTE_DPLL3_PHLOCK	R/W	0x0	DPLL3 mute enabled during phase lock. Muted outputs will start clocking glitch free once achieving lock status. PLL3 outputs will be muted even if DPLL3_EN = 0. ROM=Y, EEPROM=Y

Table 1-57. R61 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MUTE_DPLL3_FRLOCK	R/W	0x0	DPLL3 mute enabled during dpll lock. Muted outputs will start clocking glitch free once achieving lock status. PLL3 outputs will be muted even if DPLL3_EN = 0. ROM=Y, EEPROM=Y

1.56 R62 (Offset = 0x3E)

Return to the Summary Table.

Table 1-58. R62 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	MUTE_DPLL2_PHLOCK	R/W	0x0	DPLL2 mute enabled during phase lock. Muted outputs will start clocking glitch free once achieving lock status. PLL2 outputs will be muted even if DPLL2_EN = 0. ROM=Y, EEPROM=Y
4	MUTE_DPLL2_FRLOCK	R/W	0x0	DPLL2 mute enabled during dpll lock. Muted outputs will start clocking glitch free once achieving lock status. PLL2 outputs will be muted even if DPLL2_EN = 0. ROM=Y, EEPROM=Y
3	MUTE_APLL2_LOCK	R/W	0x0	APLL2 mute enabled during PLL lock. Muted outputs will start clocking glitch free once achieving lock status. ROM=Y, EEPROM=Y
2	MUTE_DPLL1_PHLOCK	R/W	0x0	DPLL1 mute enabled during phase lock. Muted outputs will start clocking glitch free once achieving lock status. ROM=Y, EEPROM=Y
1	MUTE_DPLL1_FRLOCK	R/W	0x0	DPLL1 mute enabled during dpll lock. Muted outputs will start clocking glitch free once achieving lock status. ROM=Y, EEPROM=Y
0	MUTE_APLL1_LOCK	R/W	0x0	APLL1 mute enabled during PLL lock. Muted outputs will start clocking glitch free once achieving lock status. ROM=Y, EEPROM=Y

1.57 R63 (Offset = 0x3F)

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Table 1-59. R63 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-59. R63 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XO_FDET_BYP	R/W	0x0	Frequency Detector Bypass. When XO_FDET_BYP is set to 1, the output of the XO frequency detector is ignored. ROM=Y, EEPROM=N
3:0	XO_ITYPE	R/W	0x0	XO interface type control. ROM=Y, EEPROM=Y 0x0 = DC (ext term) 0x1 = AC (ext term) 0x3 = AC (int 100 Ω to GND) 0x4 = DC (int 50 Ω to GND) 0x5 = AC (int 50 Ω to GND) 0x8 = LVCMOS 0xC = LVCMOS (int 50 Ω)

1.58 R64 (Offset = 0x40)

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Table 1-60. R64 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	XO_OUT_BUF_EN	R/W	0x9	Bit position enables XO Output Buffer path to: [0] The XO Freq Detector [1] APLL1 REF [2] APLL2 REF [3] APLL3 REF, and [4] OUT0_1 ROM=Y, EEPROM=Y

1.59 R65 (Offset = 0x41)

Return to the Summary Table.

Table 1-61. R65 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-61. R65 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF3_ITYPE	R/W	0x0	To be updated. REF3 interface type control. ROM=Y, EEPROM=N 0x0 = DIFFin, ext DC, ext term 0x1 = DIFFin, ext AC, ext term 0x2 = DIFFin, ext DC, int 100 Ω diff 0x3 = DIFFin, ext AC, int 100 Ω diff 0x4 = DIFFin, ext DC, int 50 Ω to GND 0x5 = DIFFin, ext AC, int 50 Ω to GND 0x8 = CMOS, ext DC, int AC couple, 70 mV margin 0xC = S-E, ext DC, int AC couple, 70 mV margin, int 50 Ω to GND 0x18 = CMOS, ext DC, int DC couple, 150 mV hysteresis 0x23 = DIFFin, ext AC/DC, int 100 Ω diff, 210 mV margin 0x28 = CMOS, ext DC, int AC couple, 210 mV margin 0x38 = CMOS, ext DC, int DC couple, 0 mV hysteresis

1.60 R66 (Offset = 0x42)

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Table 1-62. R66 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF2_ITYPE	R/W	0x0	To be updated. REF2 interface type control. ROM=Y, EEPROM=N 0x0 = DIFFin, ext DC, ext term 0x1 = DIFFin, ext AC, ext term 0x2 = DIFFin, ext DC, int 100 Ω diff 0x3 = DIFFin, ext AC, int 100 Ω diff 0x4 = DIFFin, ext DC, int 50 Ω to GND 0x5 = DIFFin, ext AC, int 50 Ω to GND 0x8 = CMOS, ext DC, int AC couple, 70 mV margin 0xC = S-E, ext DC, int AC couple, 70 mV margin, int 50 Ω to GND 0x18 = CMOS, ext DC, int DC couple, 150 mV hysteresis 0x23 = DIFFin, ext AC/DC, int 100 Ω diff, 210 mV margin 0x28 = CMOS, ext DC, int AC couple, 210 mV margin 0x38 = CMOS, ext DC, int DC couple, 0 mV hysteresis

1.61 R67 (Offset = 0x43)

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Table 1-63. R67 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_ITYPE	R/W	0x0	REF1 interface type control. ROM=Y, EEPROM=N 0x0 = DIFFin, ext DC, ext term 0x1 = DIFFin, ext AC, ext term 0x2 = DIFFin, ext DC, int 100 Ω diff 0x3 = DIFFin, ext AC, int 100 Ω diff 0x4 = DIFFin, ext DC, int 50 Ω to GND 0x5 = DIFFin, ext AC, int 50 Ω to GND 0x8 = CMOS, ext DC, int AC couple, 70 mV margin 0xC = S-E, ext DC, int AC couple, 70 mV margin, int 50 Ω to GND 0x18 = CMOS, ext DC, int DC couple, 150 mV hysteresis 0x23 = DIFFin, ext AC/DC, int 100 Ω diff, 210 mV margin 0x28 = CMOS, ext DC, int AC couple, 210 mV margin 0x38 = CMOS, ext DC, int DC couple, 0 mV hysteresis

1.62 R68 (Offset = 0x44)

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Table 1-64. R68 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF0_ITYPE	R/W	0x0	REF0 interface type control. ROM=Y, EEPROM=N 0x0 = DIFFin, ext DC, ext term 0x1 = DIFFin, ext AC, ext term 0x2 = DIFFin, ext DC, int 100 Ω diff 0x3 = DIFFin, ext AC, int 100 Ω diff 0x4 = DIFFin, ext DC, int 50 Ω to GND 0x5 = DIFFin, ext AC, int 50 Ω to GND 0x8 = CMOS, ext DC, int AC couple, 70 mV margin 0xC = S-E, ext DC, int AC couple, 70 mV margin, int 50 Ω to GND 0x18 = CMOS, ext DC, int DC couple, 150 mV hysteresis 0x23 = DIFFin, ext AC/DC, int 100 Ω diff, 210 mV margin 0x28 = CMOS, ext DC, int AC couple, 210 mV margin 0x38 = CMOS, ext DC, int DC couple, 0 mV hysteresis

1.63 R70 (Offset = 0x46)

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Table 1-65. R70 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	STATUS_MUX_DIV2_EN	R/W	0x0	Enable all DivideBy2 clocks for Status MUX debug signals ROM=N, EEPROM=N

1.64 R75 (Offset = 0x4B)

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Table 1-66. R75 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	TDC3_ZDM_BYPASS_FB_DIV	R/W	0x0	Selects TDC3 feedback input source. 0 = FB_DIV (Normal or ZDM) 1 = bypass FBDIV (ZDM) ROM=Y, EEPROM=N 0x0 = Select FB Divider 0x1 = Bypass FB Divider
5	TDC3_ZDM_FB_PRE_BYP	R/W	0x0	Bypasses TDC3 feedback divider when using ZDM with DPLL3. ROM=Y, EEPROM=N 0x0 = Select FB Prescaler 0x1 = Bypass FB Prescaler
4:3	TDC3_IN_SEL	R/W	0x3	Selects TDC3 zero delay input ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = OUT_10_11_ZD_FB 0x2 = OUT_0_1_ZD_FB 0x3 = VCO3 direct (ZDM disabled)
2:0	TDC3_IN_DRV_SEL	R/W	0x2	Enables zero delay input mux output ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = ZDM disabled 0x3 = Reserved 0x4 = Reserved 0x5 = ZDM enabled 0x6 = Reserved 0x7 = Reserved

1.65 R76 (Offset = 0x4C)

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Table 1-67. R76 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	TDC2_ZDM_BYPASS_FB_DIV	R/W	0x0	Selects TDC2 feedback input source. 0 = FB_DIV (Normal or ZDM) 1 = bypass FBDIV (ZDM) ROM=Y, EEPROM=N 0x0 = Select FB Divider 0x1 = Bypass FB Divider
5	TDC2_ZDM_FB_PRE_BYP	R/W	0x0	Bypasses TDC2 feedback divider when using ZDM with DPLL2. ROM=Y, EEPROM=N 0x0 = Select FB Prescaler 0x1 = Bypass FB Prescaler
4:3	TDC2_IN_SEL	R/W	0x3	Selects zero delay input ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = OUT_4_5_ZD_FB 0x2 = OUT_0_1_ZD_FB 0x3 = VCO2 direct (ZDM disabled)
2:0	TDC2_IN_DRV_SEL	R/W	0x2	Enables zero delay input mux output ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = ZDM disabled 0x3 = Reserved 0x4 = Reserved 0x5 = ZDM enabled 0x6 = Reserved 0x7 = Reserved

1.66 R77 (Offset = 0x4D)

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Table 1-68. R77 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	TDC1_ZDM_BYPASS_FB_DIV	R/W	0x0	Selects TDC1 feedback input source. 0 = FB_DIV (Normal or ZDM) 1 = bypass FBDIV (ZDM) ROM=Y, EEPROM=N 0x0 = Select FB Divider 0x1 = Bypass FB Divider

Table 1-68. R77 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TDC1_ZDM_FB_PRE_BYP	R/W	0x0	Bypasses TDC1 feedback divider when using ZDM with DPLL1. ROM=Y, EEPROM=N 0x0 = Select FB Prescaler 0x1 = Bypass FB Prescaler
4:3	TDC1_IN_SEL	R/W	0x3	Selects which output group to feedback for zero delay mode. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = OUT_0_1_ZD_FB 0x3 = VCO1 direct (ZDM disabled)
2:0	TDC1_IN_DRV_SEL	R/W	0x2	Enables zero delay input mux output ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = ZDM disabled 0x3 = Reserved 0x4 = Reserved 0x5 = ZDM enabled 0x6 = Reserved 0x7 = Reserved

1.67 R78 (Offset = 0x4E)

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Table 1-69. R78 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF_OUT01_EN	R/W	0x0	Ref to OUT0_1 Enable. Enables the path for a reference clock (selected by REF_2OUT01_SEL) to be available for selection at OUT0_1. ROM=Y, EEPROM=N
4:0	REF_OUT01_SEL	R/W	0x0	Ref to OUT0_1 Select. Selects one reference clock which will be fed to the input of OUT0_1 (if path enabled by REF_2OUT01_EN). ROM=Y, EEPROM=N 0x0 = OFF 0x1 = REF0 0x2 = REF1 0x4 = REF2 0x8 = REF3

1.68 R79 (Offset = 0x4F)

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Table 1-70. R79 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF0_EARLY_DET_EN	R/W	0x0	REF0 Early Clock Detect Enable ROM=Y, EEPROM=N
4	REF0_PH_VALID_EN	R/W	0x0	REF0 Phase Validation Enable ROM=Y, EEPROM=N
3	REF0_VALTMR_EN	R/W	0x1	REF0 Validation Timer Enable ROM=Y, EEPROM=N
2	REF0_PPM_EN	R/W	0x1	REF0 Freq ppm Enable ROM=Y, EEPROM=N
1	REF0_MISSCLK_EN	R/W	0x1	REF0 Missing Clock Detect Enable ROM=Y, EEPROM=N
0	RESERVED	R	0x0	Reserved

1.69 R80 (Offset = 0x50)

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Table 1-71. R80 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF1_EARLY_DET_EN	R/W	0x0	REF1 Early Clock Detect Enable ROM=Y, EEPROM=N
4	REF1_PH_VALID_EN	R/W	0x0	REF1 Phase Validation Enable ROM=Y, EEPROM=N
3	REF1_VALTMR_EN	R/W	0x1	REF1 Validation Timer Enable ROM=Y, EEPROM=N
2	REF1_PPM_EN	R/W	0x1	REF1 Freq ppm Enable ROM=Y, EEPROM=N
1	REF1_MISSCLK_EN	R/W	0x1	REF1 Missing Clock Detect Enable ROM=Y, EEPROM=N
0	RESERVED	R	0x0	Reserved

1.70 R81 (Offset = 0x51)

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Table 1-72. R81 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF2_EARLY_DET_EN	R/W	0x0	REF2 Early Clock Detect Enable ROM=Y, EEPROM=N
4	REF2_PH_VALID_EN	R/W	0x0	REF2 Phase Validation Enable ROM=Y, EEPROM=N
3	REF2_VALTMR_EN	R/W	0x0	REF2 Validation Timer Enable ROM=Y, EEPROM=N
2	REF2_PPM_EN	R/W	0x0	REF2 Freq ppm Enable ROM=Y, EEPROM=N
1	REF2_MISSCLK_EN	R/W	0x0	REF2 Missing Clock Detect Enable ROM=Y, EEPROM=N
0	RESERVED	R	0x0	Reserved

1.71 R82 (Offset = 0x52)

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Table 1-73. R82 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF3_EARLY_DET_EN	R/W	0x0	REF3 Early Clock Detect Enable ROM=Y, EEPROM=N
4	REF3_PH_VALID_EN	R/W	0x0	REF3 Phase Validation Enable ROM=Y, EEPROM=N
3	REF3_VALTMR_EN	R/W	0x0	REF3 Validation Timer Enable ROM=Y, EEPROM=N
2	REF3_PPM_EN	R/W	0x0	REF3 Freq ppm Enable ROM=Y, EEPROM=N
1	REF3_MISSCLK_EN	R/W	0x0	REF3 Missing Clock Detect Enable ROM=Y, EEPROM=N
0	RESERVED	R	0x0	Reserved

1.72 R83 (Offset = 0x53)

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Table 1-74. R83 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	REF3_DET_CLK_DIV	R/W	0x2	REF3 Clock Detector Divider. Bit 0 controls the divide value (0=Div4, 1=Div16). Bit 1, if set, causes the divider to be bypassed. ROM=Y, EEPROM=N 0x0 = Div By 4 0x1 = Div By 16 0x2 = Bypass 0x3 = Bypass (Reserved)
5:4	REF2_DET_CLK_DIV	R/W	0x2	REF2 Clock Detector Divider. Bit 0 controls the divide value (0=Div4, 1=Div16). Bit 1, if set, causes the divider to be bypassed. ROM=Y, EEPROM=N 0x0 = Div By 4 0x1 = Div By 16 0x2 = Bypass 0x3 = Bypass (Reserved)
3:2	REF1_DET_CLK_DIV	R/W	0x2	REF1 Clock Detector Divider. Bit 0 controls the divide value (0=Div4, 1=Div16). Bit 1, if set, causes the divider to be bypassed. ROM=Y, EEPROM=N 0x0 = Div By 4 0x1 = Div By 16 0x2 = Bypass 0x3 = Bypass (Reserved)
1:0	REF0_DET_CLK_DIV	R/W	0x0	REF0 Clock Detector Divider. Bit 0 controls the divide value (0=Div4, 1=Div16). Bit 1, if set, causes the divider to be bypassed. ROM=Y, EEPROM=N 0x0 = Div By 4 0x1 = Div By 16 0x2 = Bypass 0x3 = Bypass (Reserved)

1.73 R84 (Offset = 0x54)

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Table 1-75. R84 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF0_MISSCLK_DIV_21:16	R/W	0x0	See Register 86

1.74 R85 (Offset = 0x55)

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Table 1-76. R85 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_MISSCLK_DIV_15:8	R/W	0x0	See Register 86

1.75 R86 (Offset = 0x56)

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Table 1-77. R86 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_MISSCLK_DIV	R/W	0xB	REF0 Missing Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF0 or VCO2/5 to REF0 (determined by REF0_MISSCLK_VCOSEL selection) with some offset added for upper bound. ROM=Y, EEPROM=N

1.76 R87 (Offset = 0x57)

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Table 1-78. R87 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_MISSCLK_DIV_21:16	R/W	0x0	See Register 89

1.77 R88 (Offset = 0x58)

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Table 1-79. R88 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_MISSCLK_DIV_15:8	R/W	0x0	See Register 89

1.78 R89 (Offset = 0x59)

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Table 1-80. R89 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_MISSCLK_DIV	R/W	0x7E	REF1 Missing Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF1 or VCO2/5 to REF0 (determined by REF1_MISSCLK_VCOSEL selection) with some offset added for upper bound. ROM=Y, EEPROM=N

1.79 R90 (Offset = 0x5A)

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Table 1-81. R90 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF2_MISSCLK_DIV_21:16	R/W	0x0	See Register 92

1.80 R91 (Offset = 0x5B)

Return to the Summary Table.

Table 1-82. R91 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_MISSCLK_DIV_15:8	R/W	0x0	See Register 92

1.81 R92 (Offset = 0x5C)

Return to the Summary Table.

Table 1-83. R92 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_MISSCLK_DIV	R/W	0x35	REF2 Missing Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF2 or VCO2/5 to REF2 (determined by REF0_MISSCLK_VCOSEL selection) with some offset added for upper bound. ROM=Y, EEPROM=N

1.82 R93 (Offset = 0x5D)

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Table 1-84. R93 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF3_MISSCLK_DIV_21:16	R/W	0x0	See Register 95

1.83 R94 (Offset = 0x5E)

Return to the Summary Table.

Table 1-85. R94 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_MISSCLK_DIV_15:8	R/W	0x0	See Register 95

1.84 R95 (Offset = 0x5F)

Return to the Summary Table.

Table 1-86. R95 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_MISSCLK_DIV	R/W	0x4	REF3 Missing Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF3 or VCO2/5 to REF3 (determined by REF0_MISSCLK_VCOSEL selection) with some offset added for upper bound. ROM=Y, EEPROM=N

1.85 R96 (Offset = 0x60)

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Table 1-87. R96 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:1	RESERVED	R	0x0	Reserved
0	REF0_MISSCLK_VCOSEL	R/W	0x0	Missing/Early Clock Detector VCO selection for all references. Also selects TEC clock source. ROM=Y, EEPROM=N 0x0 = VCO3 0x1 = VCO2

1.86 R97 (Offset = 0x61)

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Table 1-88. R97 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF0_EARLY_CLK_DIV_21:16	R/W	0x0	See Register 99

1.87 R98 (Offset = 0x62)

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Table 1-89. R98 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_EARLY_CLK_DIV_15:8	R/W	0x0	See Register 99

1.88 R99 (Offset = 0x63)

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Table 1-90. R99 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_EARLY_CLK_DIV	R/W	0x3	REF0 Early Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF0 or VCO2/5 to REF0 (determined by REF0_MISSCLK_VCOSEL selection) with some offset subtracted for lower bound. ROM=Y, EEPROM=N

1.89 R100 (Offset = 0x64)

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Table 1-91. R100 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_EARLY_CLK_DIV_21:16	R/W	0x0	See Register 102

1.90 R101 (Offset = 0x65)

Return to the Summary Table.

Table 1-92. R101 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_EARLY_CLK_DIV_15:8	R/W	0x0	See Register 102

1.91 R102 (Offset = 0x66)

Return to the Summary Table.

Table 1-93. R102 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_EARLY_CLK_DIV	R/W	0x76	REF1 Early Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF1 or VCO2/5 to REF1 (determined by REF0_MISSCLK_VCOSEL selection) with some offset subtracted for lower bound. ROM=Y, EEPROM=N

1.92 R103 (Offset = 0x67)

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Table 1-94. R103 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF2_EARLY_CLK_DIV_21:16	R/W	0x0	See Register 105

1.93 R104 (Offset = 0x68)

Return to the Summary Table.

Table 1-95. R104 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_EARLY_CLK_DIV_15:8	R/W	0x0	See Register 105

1.94 R105 (Offset = 0x69)

Return to the Summary Table.

Table 1-96. R105 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_EARLY_CLK_DIV	R/W	0x2D	REF2 Early Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF2 or VCO2/5 to REF2 (determined by REF0_MISSCLK_VCOSEL selection) with some offset subtracted for lower bound. ROM=Y, EEPROM=N

1.95 R106 (Offset = 0x6A)

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Table 1-97. R106 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF3_EARLY_CLK_DIV_21:16	R/W	0x1F	See Register 108

1.96 R107 (Offset = 0x6B)

Return to the Summary Table.

Table 1-98. R107 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_EARLY_CLK_DIV_15:8	R/W	0xFF	See Register 108

1.97 R108 (Offset = 0x6C)

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Table 1-99. R108 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_EARLY_CLK_DIV	R/W	0xFF	REF3 Early Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF3 or VCO2/5 to REF3 (determined by REF0_MISSCLK_VCOSEL selection) with some offset subtracted for lower bound. ROM=Y, EEPROM=N

1.98 R109 (Offset = 0x6D)

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Table 1-100. R109 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF0_PPM_MIN_14:8	R/W	0x0	See Register 110

1.99 R110 (Offset = 0x6E)

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Table 1-101. R110 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_PPM_MIN	R/W	0xE	REF0 Frequency PPM Lower Limit ROM=Y, EEPROM=N

1.100 R111 (Offset = 0x6F)

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Table 1-102. R111 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF0_PPM_MAX_14:8	R/W	0x0	See Register 112

1.101 R112 (Offset = 0x70)

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Table 1-103. R112 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_PPM_MAX	R/W	0x14	REF0 Frequency PPM Upper Limit ROM=Y, EEPROM=N

1.102 R113 (Offset = 0x71)

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Table 1-104. R113 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-104. R113 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	REF1_PPM_MIN_14:8	R/W	0x0	See Register 114

1.103 R114 (Offset = 0x72)

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Table 1-105. R114 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_PPM_MIN	R/W	0xE	REF1 Frequency PPM Lower Limit ROM=Y, EEPROM=N

1.104 R115 (Offset = 0x73)

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Table 1-106. R115 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF1_PPM_MAX_14:8	R/W	0x0	See Register 116

1.105 R116 (Offset = 0x74)

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Table 1-107. R116 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_PPM_MAX	R/W	0x14	REF1 Frequency PPM Upper Limit ROM=Y, EEPROM=N

1.106 R117 (Offset = 0x75)

Return to the Summary Table.

Table 1-108. R117 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF2_PPM_MIN_14:8	R/W	0x0	See Register 118

1.107 R118 (Offset = 0x76)

Return to the Summary Table.

Table 1-109. R118 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_PPM_MIN	R/W	0xE	REF2 Frequency PPM Lower Limit ROM=Y, EEPROM=N

1.108 R119 (Offset = 0x77)

Return to the Summary Table.

Table 1-110. R119 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF2_PPM_MAX_14:8	R/W	0x0	See Register 120

1.109 R120 (Offset = 0x78)

Return to the Summary Table.

Table 1-111. R120 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_PPM_MAX	R/W	0x14	REF2 Frequency PPM Upper Limit ROM=Y, EEPROM=N

1.110 R121 (Offset = 0x79)

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Table 1-112. R121 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF3_PPM_MIN_14:8	R/W	0x0	See Register 122

1.111 R122 (Offset = 0x7A)

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Table 1-113. R122 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_PPM_MIN	R/W	0xE	REF3 Frequency PPM Lower Limit ROM=Y, EEPROM=N

1.112 R123 (Offset = 0x7B)

Return to the Summary Table.

Table 1-114. R123 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF3_PPM_MAX_14:8	R/W	0x0	See Register 124

1.113 R124 (Offset = 0x7C)

Return to the Summary Table.

Table 1-115. R124 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_PPM_MAX	R/W	0x14	REF3 Frequency PPM Upper Limit ROM=Y, EEPROM=N

1.114 R125 (Offset = 0x7D)

Return to the Summary Table.

Table 1-116. R125 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R	0x0	Reserved
3:0	REF0_CNTSTRT_27:24	R/W	0x0	See Register 128

1.115 R126 (Offset = 0x7E)

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Table 1-117. R126 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_CNTSTRT_23:16	R/W	0x2	See Register 128

1.116 R127 (Offset = 0x7F)

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Table 1-118. R127 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_CNTSTRT_15:8	R/W	0x7B	See Register 128

1.117 R128 (Offset = 0x80)

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Table 1-119. R128 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_CNTSTRT	R/W	0xC9	28-bit REF0 PPM detect counter. REF0 decreases a counter reset by REF0_CNTSTRT value. When this becomes 0, then counter reset by REF0_HOLD_CNTSTRT is the error and used to know frequency accuracy. ROM=Y, EEPROM=N

1.118 R129 (Offset = 0x81)

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Table 1-120. R129 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	REF0_HOLD_CNTSTRT_27:24	R/W	0x0	See Register 132

1.119 R130 (Offset = 0x82)

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Table 1-121. R130 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_HOLD_CNTSTRT_23:16	R/W	0x3	See Register 132

1.120 R131 (Offset = 0x83)

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Table 1-122. R131 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_HOLD_CNTSTRT_15:8	R/W	0xD	See Register 132

1.121 R132 (Offset = 0x84)

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Table 1-123. R132 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_HOLD_CNTSTRT	R/W	0x41	28-bit REF0 PPM detect counter. XO decreases a counter reset by REF0_HOLD_CNTSTRT. When counter reset by REF0_CNTSTRT becomes 0, this counter reset by REF0_HOLD_CNTSTRT contains the time error from which PPM error may be determined. ROM=Y, EEPROM=N

1.122 R133 (Offset = 0x85)

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Table 1-124. R133 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R	0x0	Reserved
3:0	REF1_CNTSTRT_27:24	R/W	0x0	See Register 136

1.123 R134 (Offset = 0x86)

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Table 1-125. R134 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_CNTSTRT_23:16	R/W	0x0	See Register 136

1.124 R135 (Offset = 0x87)

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Table 1-126. R135 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_CNTSTRT_15:8	R/W	0xA2	See Register 136

1.125 R136 (Offset = 0x88)

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Table 1-127. R136 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_CNTSTRT	R/W	0xC3	28-bit REF1 PPM detect counter. REF1 decreases a counter reset by REF1_CNTSTRT value. When this becomes 0, then counter reset by REF1_HOLD_CNTSTRT is the error and used to know frequency accuracy. ROM=Y, EEPROM=N

1.126 R137 (Offset = 0x89)

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Table 1-128. R137 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	REF1_HOLD_CNTSTRT_27:24	R/W	0x0	See Register 140

1.127 R138 (Offset = 0x8A)

Return to the Summary Table.

Table 1-129. R138 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_HOLD_CNTSTRT_23:16	R/W	0x3	See Register 140

1.128 R139 (Offset = 0x8B)

Return to the Summary Table.

Table 1-130. R139 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_HOLD_CNTSTRT_15:8	R/W	0xD	See Register 140

1.129 R140 (Offset = 0x8C)

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Table 1-131. R140 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_HOLD_CNTSTRT	R/W	0x42	28-bit REF1 PPM detect counter. XO decreases a counter reset by REF1_HOLD_CNTSTRT. When counter reset by REF1_CNTSTRT becomes 0, this counter reset by REF1_HOLD_CNTSTRT contains the time error from which PPM error may be determined. ROM=Y, EEPROM=N

1.130 R141 (Offset = 0x8D)

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Table 1-132. R141 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	REF2_PH_VALID_CNT_MSB	R/W	0x0	REF2 phase detector validation. Extra 3 bits for REF2 phase detector validation counter. Lower 28-bits are in REF2_CNTSTRT. REF2 frequency PPM detect validation and phase detect validation are mutually exclusive. Only one of REF2_PPM_EN or REF2_PH_VALID_EN may be enabled at same time. ROM=Y, EEPROM=N
3:0	REF2_CNTSTRT_27:24	R/W	0x0	See Register 144

1.131 R142 (Offset = 0x8E)

Return to the Summary Table.

Table 1-133. R142 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_CNTSTRT_23:16	R/W	0x1	See Register 144

1.132 R143 (Offset = 0x8F)

Return to the Summary Table.

Table 1-134. R143 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_CNTSTRT_15:8	R/W	0x96	See Register 144

1.133 R144 (Offset = 0x90)

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Table 1-135. R144 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_CNTSTRT	R/W	0xE7	28-bit REF2 PPM detect counter. REF2 decreases a counter reset by REF2_CNTSTRT value. When this becomes 0, then counter reset by REF2_HOLD_CNTSTRT is the error and used to know frequency accuracy. ROM=Y, EEPROM=N

1.134 R145 (Offset = 0x91)

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Table 1-136. R145 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	REF2_HOLD_CNTSTRT_27:24	R/W	0x0	See Register 148

1.135 R146 (Offset = 0x92)

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Table 1-137. R146 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_HOLD_CNTSTRT_23:16	R/W	0x3	See Register 148

1.136 R147 (Offset = 0x93)

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Table 1-138. R147 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_HOLD_CNTSTRT_15:8	R/W	0xD	See Register 148

1.137 R148 (Offset = 0x94)

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Table 1-139. R148 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_HOLD_CNTSTRT	R/W	0x41	28-bit REF2 PPM detect counter. XO decreases a counter reset by REF2_HOLD_CNTSTRT. When counter reset by REF2_CNTSTRT becomes 0, this counter reset by REF2_HOLD_CNTSTRT contains the time error from which PPM error may be determined. ROM=Y, EEPROM=N

1.138 R149 (Offset = 0x95)

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Table 1-140. R149 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	REF3_PH_VALID_CNT_MSB	R/W	0x0	REF3 phase detector validation. Extra 3 bits for REF3 phase detector validation counter. Lower 28-bits are in REF3_CNTSTRT. REF3 frequency PPM detect validation and phase detect validation are mutually exclusive. Only one of REF3_PPM_EN or REF3_PH_VALID_EN may be enabled at same time. ROM=Y, EEPROM=N
3:0	REF3_CNTSTRT_27:24	R/W	0x0	See Register 152

1.139 R150 (Offset = 0x96)

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Table 1-141. R150 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_CNTSTRT_23:16	R/W	0x1	See Register 152

1.140 R151 (Offset = 0x97)

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Table 1-142. R151 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_CNTSTRT_15:8	R/W	0x96	See Register 152

1.141 R152 (Offset = 0x98)

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Table 1-143. R152 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_CNTSTRT	R/W	0xE7	28-bit REF3 PPM detect counter. REF3 decreases a counter reset by REF3_CNTSTRT value. When this becomes 0, then counter reset by REF3_HOLD_CNTSTRT is the error and used to know frequency accuracy. ROM=Y, EEPROM=N

1.142 R153 (Offset = 0x99)

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Table 1-144. R153 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	REF3_HOLD_CNTSTRT_27:24	R/W	0x0	See Register 156

1.143 R154 (Offset = 0x9A)

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Table 1-145. R154 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_HOLD_CNTSTRT_23:16	R/W	0x3	See Register 156

1.144 R155 (Offset = 0x9B)

Return to the Summary Table.

Table 1-146. R155 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_HOLD_CNTSTRT_15:8	R/W	0xD	See Register 156

1.145 R156 (Offset = 0x9C)

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Table 1-147. R156 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_HOLD_CNTSTRT	R/W	0x41	28-bit REF3 PPM detect counter. XO decreases a counter reset by REF3_HOLD_CNTSTRT. When counter reset by REF3_CNTSTRT becomes 0, this counter reset by REF3_HOLD_CNTSTRT contains the time error from which PPM error may be determined. ROM=Y, EEPROM=N

1.146 R157 (Offset = 0x9D)

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Table 1-148. R157 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-148. R157 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	REF0VLDTMR	R/W	0xA	REF0 Validation Timer. All selected validations must be valid for selected amount of time before the IN0/REF0 is considered valid. ROM=Y, EEPROM=N 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6 s 0xF = 3.3 s 0x10 = 6.6 s 0x11 = 13.1 s 0x12 = 26.2 s 0x13 = 52.4 s 0x14 = 1.7 min 0x15 = 3.5 min 0x16 = 7.0 min 0x17 = 14.0 min 0x18 = 28.0 min 0x19 = 55.9 min 0x1A = 1.9 hr 0x1B = 3.7 hr 0x1C = 7.5 hr 0x1D = 14.9 hr 0x1E = 29.8 hr 0x1F = 59.7 hr

1.147 R158 (Offset = 0x9E)

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Table 1-149. R158 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-149. R158 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	REF1VLDTMR	R/W	0xA	REF1 Validation Timer. All selected validations must be valid for selected amount of time before the IN1/REF1 is considered valid. ROM=Y, EEPROM=N 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6 s 0xF = 3.3 s 0x10 = 6.6 s 0x11 = 13.1 s 0x12 = 26.2 s 0x13 = 52.4 s 0x14 = 1.7 min 0x15 = 3.5 min 0x16 = 7.0 min 0x17 = 14.0 min 0x18 = 28.0 min 0x19 = 55.9 min 0x1A = 1.9 hr 0x1B = 3.7 hr 0x1C = 7.5 hr 0x1D = 14.9 hr 0x1E = 29.8 hr 0x1F = 59.7 hr

1.148 R159 (Offset = 0x9F)

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Table 1-150. R159 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-150. R159 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	REF2VLDTMR	R/W	0xA	REF2 Validation Timer. All selected validations must be valid for selected amount of time before the IN2/REF2 is considered valid. ROM=Y, EEPROM=N 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6 s 0xF = 3.3 s 0x10 = 6.6 s 0x11 = 13.1 s 0x12 = 26.2 s 0x13 = 52.4 s 0x14 = 1.7 min 0x15 = 3.5 min 0x16 = 7.0 min 0x17 = 14.0 min 0x18 = 28.0 min 0x19 = 55.9 min 0x1A = 1.9 hr 0x1B = 3.7 hr 0x1C = 7.5 hr 0x1D = 14.9 hr 0x1E = 29.8 hr 0x1F = 59.7 hr

1.149 R160 (Offset = 0xA0)

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Table 1-151. R160 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-151. R160 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	REF3VLDTMR	R/W	0xA	REF3 Validation Timer. All selected validations must be valid for selected amount of time before the IN3/REF3 is considered valid. ROM=Y, EEPROM=N 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6 s 0xF = 3.3 s 0x10 = 6.6 s 0x11 = 13.1 s 0x12 = 26.2 s 0x13 = 52.4 s 0x14 = 1.7 min 0x15 = 3.5 min 0x16 = 7.0 min 0x17 = 14.0 min 0x18 = 28.0 min 0x19 = 55.9 min 0x1A = 1.9 hr 0x1B = 3.7 hr 0x1C = 7.5 hr 0x1D = 14.9 hr 0x1E = 29.8 hr 0x1F = 59.7 hr

1.150 R161 (Offset = 0xA1)

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Table 1-152. R161 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF0_PH_VALID_THR_13:8	R/W	0x0	REF0 Phase Validation Threshold ROM=Y, EEPROM=N

1.151 R162 (Offset = 0xA2)

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Table 1-153. R162 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_PH_VALID_THR	R/W	0x0	REF0 Phase Validation Threshold ROM=Y, EEPROM=N

1.152 R163 (Offset = 0xA3)

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Table 1-154. R163 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_PH_VALID_THR_13:8	R/W	0x0	REF1 Phase Validation Threshold ROM=Y, EEPROM=N

1.153 R164 (Offset = 0xA4)

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Table 1-155. R164 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_PH_VALID_THR	R/W	0x0	REF1 Phase Validation Threshold ROM=Y, EEPROM=N

1.154 R165 (Offset = 0xA5)

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Table 1-156. R165 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF2_PH_VALID_THR_13:8	R/W	0x0	REF2 Phase Validation Threshold ROM=Y, EEPROM=N

1.155 R166 (Offset = 0xA6)

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Table 1-157. R166 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_PH_VALID_THR	R/W	0x0	REF2 Phase Validation Threshold ROM=Y, EEPROM=N

1.156 R167 (Offset = 0xA7)

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Table 1-158. R167 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF3_PH_VALID_THR_13:8	R/W	0x0	REF3 Phase Validation Threshold ROM=Y, EEPROM=N

1.157 R168 (Offset = 0xA8)

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Table 1-159. R168 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_PH_VALID_THR	R/W	0x0	REF3 Phase Validation Threshold ROM=Y, EEPROM=N

1.158 R170 (Offset = 0xAA)

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Table 1-160. R170 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMSCRC	R	0x0	NVM Stored CRC ROM=N, EEPROM=N

1.159 R171 (Offset = 0xAB)

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Table 1-161. R171 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-161. R171 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	REGCOMMIT	R/WSC	0x0	Copy fields which also exist in SRAM to SRAM memory. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete. Next an EEPROM programming operation may be performed to update NVM EEPROM. When programming to alter an NVM profile, it is suggested to toggle PD# to assure default conditions, change the desired fields, then assert the REGCOMMIT bit. ROM=N, EEPROM=N
5	NVMCRCERR	R	0x0	NVM CRC Error Indication. The NVMCRCERR bit is set to 1 if a CRC Error has been detected when reading back from on-chip EEPROM during device configuration. ROM=N, EEPROM=N
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	NVMBUSY	R	0x0	NVM Program Busy Indication. The NVMBUSY bit is 1 during an on-chip EEPROM Erase/Program cycle. While NVMBUSY is 1 the on-chip EEPROM cannot be accessed. Toggling PD# or removing power while NVMBUSY is asserted will corrupt the EEPROM. ROM=N, EEPROM=N
1	NVMERASE	R/WSC	0x0	NVM Erase Start. The NVMERASE bit is used to begin an on-chip EEPROM Erase cycle. The Erase cycle is only initiated if the immediately preceding I2C/SMBus transaction was a write to the NVMUNLK register with the appropriate code. The NVMERASE bit is automatically cleared to 0.
0	NVMPROG	R/WSC	0x0	NVM Program Start. The NVMPROG bit is used to begin an on-chip EEPROM Program cycle. The Program cycle is only initiated if the immediately preceding I2C/SMBus transaction was a write to the NVMUNLK register with the appropriate code. The NVMPROG bit is automatically cleared to 0.

1.160 R172 (Offset = 0xAC)

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Table 1-162. R172 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMLCRC	R	0x0	NVM Live CRC ROM=N, EEPROM=N

1.161 R173 (Offset = 0xAD)

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Table 1-163. R173 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-163. R173 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	MEMADR_12:8	R/W	0x0	See Register 174

1.162 R174 (Offset = 0xAE)

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Table 1-164. R174 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	MEMADR	R/W	0x0	Memory Address. The MEMADR value determines the starting address for access to the on-chip memories. This same MEMADR value is used for EEPROM and SRAM access which share the same memory map and also ROM access. The NVMDAT field is used to read and write from EEPROM. The RAMDAT field is used to read and write from SRAM. The ROMDAT field is used to read and write from ROM.

1.163 R175 (Offset = 0xAF)

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Table 1-165. R175 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMDAT	R/W	0x0	EEPROM Read Data. The first time an I2C/SMBus read transaction accesses the NVMDAT register address, either because it was explicitly targeted or because the address was auto-incremented, the read transaction will returnthe EEPROM data located at the address specified by the MEMADR register. Any additional read's which are part ofthe same transaction will cause the EEPROM address to be incremented and the next EEPROM data byte will bereturned. The I2C/SMBus address will no longer be auto-incremented, i.e the I2C/SMBus address will be locked tothe NVMDAT register after the first access. Access to the NVMDAT register will terminate at the end of the currentI2C/SMBus transaction. ROM=N, EEPROM=N

1.164 R176 (Offset = 0xB0)

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Table 1-166. R176 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RAMDAT	R/W	0x0	RAM Read/Write Data. The first time an I2C/SMBus read or write transaction accesses the RAMDAT register address, either because it was explicitly targeted or because the address was auto-incremented, a read transaction will return the RAM data located at the address specified by the MEMADR register and a write transaction will cause the current I2C/SMBus data to be written to the address specified by the MEMADR register. Any additional accesses which are part of the same transaction will cause the RAM address to be incremented and a read or write access will take place to the next SRAM address. The I2C/SMBus address will no longer be auto-incremented (that is, the I2C/SMBus address will be locked to the RAMDAT register after the first access). Access to the RAMDAT register will terminate at the end of the current I2C/SMBus transaction. ROM=N, EEPROM=N

1.165 R180 (Offset = 0xB4)

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Table 1-167. R180 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMUNLK	R/W	0x0	NVM Prog Unlock. The NVMUNLK register must be written immediately prior to setting the NVMERASE and NVMPROG bit, otherwise the Erase/Program cycle will not be triggered. NVMUNLK must be written with a value of 0xEA. ROM=N, EEPROM=N

1.166 R223 (Offset = 0xDF)

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Table 1-168. R223 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL1_REF0_AUTO_PRTY	R/W	0x0	REF0 Priority for Automatic Switchover. Sets the priority for REF0 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

Table 1-168. R223 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DPLL1_REF1_AUTO_PRTY	R/W	0x0	REF1 Priority for Automatic Switchover. Sets the priority for REF1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.167 R224 (Offset = 0xE0)

Return to the Summary Table.

Table 1-169. R224 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL1_REF2_AUTO_PRTY	R/W	0x0	REF2 Priority for Automatic Switchover. Sets the priority for REF2 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL1_REF3_AUTO_PRTY	R/W	0x0	REF3 Priority for Automatic Switchover. Sets the priority for REF3 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.168 R225 (Offset = 0xE1)

Return to the Summary Table.

Table 1-170. R225 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL1_REF4_AUTO_PRTY	R/W	0x0	REF4 Priority for Automatic Switchover. Sets the priority for REF4 feedback from APLL2 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL1_REF5_AUTO_PRTY	R/W	0x0	REF5 Priority for Automatic Switchover. Sets the priority for REF5 feedback from APLL3 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.169 R226 (Offset = 0xE2)

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Table 1-171. R226 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved

Table 1-171. R226 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	DPLL1_MAN_REFSEL	R/W	0x0	DPLL1 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from ROM=Y, EEPROM=N 0x0 = REF0 0x1 = REF1 0x2 = REF2 0x3 = REF3 0x4 = PLL2 0x5 = PLL3
2	DPLL1_MAN_SWITCH_PIN_MODE	R/W	0x0	DPLL1 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = Register 0x1 = Pin
1:0	DPLL1_SWITCH_MODE	R/W	0x1	DPLL1 Reference Switchover Mode. Selects between Automatic Non-revertive, Automatic Revertive, Manual Selection with Automatic Fallback, and Manual Selection with Automatic Holdover. ROM=Y, EEPROM=N 0x0 = Auto non-revertive 0x1 = Auto revertive 0x2 = Manual with fallback 0x3 = Manual with holdover

1.170 R227 (Offset = 0xE3)

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Table 1-172. R227 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_REFSEL_STAT	R	0x0	Reports the DPLL1 selected reference ROM=N, EEPROM=N 0x0 = Holdover 0x1 = REF0 0x2 = REF1 0x4 = REF2 0x8 = REF3 0x10 = APLL2 0x20 = APLL3

1.171 R228 (Offset = 0xE4)

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Table 1-173. R228 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_LOCKDET_PPM_EN	R/W	0x0	DPLL frequency lock detect enable ROM=Y, EEPROM=N
6:0	DPLL1_LOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 229

1.172 R229 (Offset = 0xE5)

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Table 1-174. R229 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_MAX	R/W	0x9	DPLL frequency lock detect in-lock threshold ROM=Y, EEPROM=N

1.173 R230 (Offset = 0xE6)

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Table 1-175. R230 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL1_UNLOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 231

1.174 R231 (Offset = 0xE7)

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Table 1-176. R231 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_UNLOCKDET_PPM_MAX	R/W	0xC	DPLL frequency lock detect out-of-lock threshold ROM=Y, EEPROM=N

1.175 R232 (Offset = 0xE8)

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Table 1-177. R232 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_LOCKDET2_PPM_CNTSTRT_29:24	R/W	0x0	See Register 235

1.176 R233 (Offset = 0xE9)

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Table 1-178. R233 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET2_PPM_CNTSTRT_23:16	R/W	0x9	See Register 235

1.177 R234 (Offset = 0xEA)

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Table 1-179. R234 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET2_PPM_CNTSTRT_15:8	R/W	0x27	See Register 235

1.178 R235 (Offset = 0xEB)

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Table 1-180. R235 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET2_PPM_CNTSTRT	R/W	0xC0	DPLL frequency lock detect reference count value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.179 R236 (Offset = 0xEC)

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Table 1-181. R236 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-181. R236 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DPLL1_LOCKDET_PPM_CNTSTRT_29:24	R/W	0x0	See Register 239

1.180 R237 (Offset = 0xED)

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Table 1-182. R237 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_CNTSTRT_23:16	R/W	0x0	See Register 239

1.181 R238 (Offset = 0xEE)

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Table 1-183. R238 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_CNTSTRT_15:8	R/W	0x4	DPLL frequency lock detect reference count value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.182 R239 (Offset = 0xEF)

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Table 1-184. R239 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_CNTSTRT	R/W	0xB1	DPLL frequency lock detect reference count value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.183 R240 (Offset = 0xF0)

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Table 1-185. R240 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-185. R240 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DPLL1_LOCKDET_VCO_PPM_CNT STRT_29:24	R/W	0x0	See Register 243

1.184 R241 (Offset = 0xF1)

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Table 1-186. R241 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_VCO_PPM_CNT STRT_23:16	R/W	0x1	See Register 243

1.185 R242 (Offset = 0xF2)

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Table 1-187. R242 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_VCO_PPM_CNT STRT_15:8	R/W	0x86	See Register 243

1.186 R243 (Offset = 0xF3)

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Table 1-188. R243 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_VCO_PPM_CNT STRT	R/W	0xF3	DPLL frequency lock detect VCO count value ROM=Y, EEPROM=N

1.187 R244 (Offset = 0xF4)

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Table 1-189. R244 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R	0x0	Reserved

Table 1-189. R244 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DPLL1_STATUS_PPM_LOCK	R	0x0	Readback lock indicator from DPLL PPM Checker ROM=N, EEPROM=N

1.188 R247 (Offset = 0xF7)

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Table 1-190. R247 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_LOOP_EN	R/W	0x0	Enable DPLL1 loop filter and R-Div mash engine ROM=Y, EEPROM=N
6	DPLL1_PHASE_CANCEL_EN	R/W	0x1	Enable Phase Cancellation ROM=Y, EEPROM=N
5	DPLL1_FASTLOCK_ALWAYS	R/W	0x0	Always perform fastlock. No phase cancellation is done. ROM=Y, EEPROM=N
4	DPLL1_PHS1_EN	R/W	0x1	Enable holdover exit phase slew control . ROM=Y, EEPROM=N
3	DPLL1_ZDM_EN	R/W	0x0	Enable Zero Delay ROM=Y, EEPROM=N
2	DPLL1_HIST_EN	R/W	0x1	Enable History word to be used during holdover ROM=Y, EEPROM=N
1	DPLL1_PHASE_CANCEL_ALWAYS	R/W	0x0	Force phase cancellation to always occur when DPLL is acquiring lock ROM=Y, EEPROM=N
0	RESERVED	R	0x0	Reserved

1.189 R248 (Offset = 0xF8)

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Table 1-191. R248 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_HOLD_SLEW_LIM_EN	R/W	0x0	Enable slew limiter when entering holdover. Allows slew rate control between current DPLL value before entering holdover and history value. Requires DPLL1_LOOP_EN=1. ROM=Y, EEPROM=N
6	RESERVED	R	0x0	Reserved
5:3	RESERVED	R	0x0	Reserved
2	DPLL1_CLK_DIV_SRC_SEL	R/W	0x0	DPLL1 cannot be used without DPLL2 or DPLL3 operating. DPLL1 clock select 0x0 = DPLL3 0x1 = DPLL2

Table 1-191. R248 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	RESERVED	R	0x0	Reserved

1.190 R250 (Offset = 0xFA)

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Table 1-192. R250 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL1_PH_OFFSET_44:40	R/W	0x0	See Register 255

1.191 R251 (Offset = 0xFB)

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Table 1-193. R251 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET_39:32	R/W	0x0	See Register 255

1.192 R252 (Offset = 0xFC)

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Table 1-194. R252 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET_31:24	R/W	0x0	See Register 255

1.193 R253 (Offset = 0xFD)

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Table 1-195. R253 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET_23:16	R/W	0x0	See Register 255

1.194 R254 (Offset = 0xFE)

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Table 1-196. R254 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET_15:8	R/W	0x0	See Register 255

1.195 R255 (Offset = 0xFF)

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Table 1-197. R255 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET	R/W	0x0	Phase offset to adjust and calibrate input to output phase in ZDM. This is a 2s complement number. ROM=Y, EEPROM=N

1.196 R256 (Offset = 0x100)

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Table 1-198. R256 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_39:32	R/W	0x0	See Register 260

1.197 R257 (Offset = 0x101)

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Table 1-199. R257 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_31:24	R/W	0x0	See Register 260

1.198 R258 (Offset = 0x102)

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Table 1-200. R258 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_23:16	R/W	0x0	See Register 260

1.199 R259 (Offset = 0x103)

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Table 1-201. R259 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_15:8	R/W	0x0	See Register 260

1.200 R260 (Offset = 0x104)

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Table 1-202. R260 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN	R/W	0x0	DPLL1 starting word. Also non-history holdover word. Used for APLL DCO. ROM=Y, EEPROM=N

1.201 R261 (Offset = 0x105)

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Table 1-203. R261 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	DPLL1_1PPS_MODE	R/W	0x0	Set when using 1-PPS input ROM=Y, EEPROM=N
5	DPLL1_1PPS_EN	R/W	0x0	Set when using 1-PPS input ROM=Y, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.202 R290 (Offset = 0x122)

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Table 1-204. R290 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_LCK_TIMER_9:8	R/W	0x3	See Register 291

1.203 R291 (Offset = 0x123)

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Table 1-205. R291 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LCK_TIMER	R/W	0x9	Minimum amount of time until DPLL1_LOPL will be deasserted after starting to lock. Timer begins once device is within valid phase lock window. ROM=Y, EEPROM=N

1.204 R292 (Offset = 0x124)

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Table 1-206. R292 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_HIST_TIMER_9:8	R/W	0x1	See Register 293

1.205 R293 (Offset = 0x125)

Return to the Summary Table.

Table 1-207. R293 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_HIST_TIMER	R/W	0x92	Time interval between history update events. ROM=Y, EEPROM=N

1.206 R294 (Offset = 0x126)

Return to the Summary Table.

Table 1-208. R294 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-208. R294 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_HOLD_TIMER_9:8	R/W	0x1	See Register 295

1.207 R295 (Offset = 0x127)

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Table 1-209. R295 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_HOLD_TIMER	R/W	0x42	Rate of change to DPLL or APLL numerator during phase slew control. See DPLLx_HOLD_SLEW_STEP. ROM=Y, EEPROM=N

1.208 R296 (Offset = 0x128)

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Table 1-210. R296 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_PHS1_TIMER_9:8	R/W	0x1	See Register 297

1.209 R297 (Offset = 0x129)

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Table 1-211. R297 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PHS1_TIMER	R/W	0x40	Holdover exit phase slew control. Timer controlling update period. ROM=Y, EEPROM=N

1.210 R302 (Offset = 0x12E)

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Table 1-212. R302 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-212. R302 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	DPLL1_HIST_GAIN	R/W	0x8	History filter gain ROM=Y, EEPROM=N

1.211 R303 (Offset = 0x12F)

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Table 1-213. R303 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_PL_THRESH	R/W	0x1E	Phase lock in-lock threshold ROM=Y, EEPROM=N

1.212 R304 (Offset = 0x130)

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Table 1-214. R304 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_PL_UNLK_THRESH	R/W	0x20	Phase lock out-of-lock threshold ROM=Y, EEPROM=N

1.213 R305 (Offset = 0x131)

Return to the Summary Table.

Table 1-215. R305 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_PHS1_THRESH	R/W	0x7	Holdover exit phase slew control. Change per timer event. ROM=Y, EEPROM=N

1.214 R308 (Offset = 0x134)

Return to the Summary Table.

Table 1-216. R308 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_HOLD_SLEW_STEP	R/W	0x3F	When DPLL exits holdover, rate of phase change relates to the ratio of DPLLx_HOLD_SLEW_STEP divided by DPLLx_HOLD_TIMER. DPLLx_HOLD_SLEW_STEP is applied to DPLL numerator when exiting holdover or APLL numerator when using APLL relative DCO. ROM=Y, EEPROM=N

1.215 R310 (Offset = 0x136)

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Table 1-217. R310 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	DPLL1_STATUS_PL	R	0x0	Readback the phase lock status ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.216 R311 (Offset = 0x137)

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Table 1-218. R311 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	DPLL1_DCO_SLEW_ACTIVE	R	0x0	Readback DCO slew status ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.217 R314 (Offset = 0x13A)

Return to the Summary Table.

Table 1-219. R314 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved

Table 1-219. R314 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DPLL1_FB_DIV_32:32	R/W	0x0	See Register 318

1.218 R315 (Offset = 0x13B)

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Table 1-220. R315 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV_31:24	R/W	0x0	See Register 318

1.219 R316 (Offset = 0x13C)

Return to the Summary Table.

Table 1-221. R316 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV_23:16	R/W	0x0	See Register 318

1.220 R317 (Offset = 0x13D)

Return to the Summary Table.

Table 1-222. R317 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV_15:8	R/W	0xF	See Register 318

1.221 R318 (Offset = 0x13E)

Return to the Summary Table.

Table 1-223. R318 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV	R/W	0xA0	DPLL Feedback Divider N Value used with DPLL1 feedback configuration 1. Divide value is programmed value except when using ZDM mode with FB div, actual divide value is +1. ROM=Y, EEPROM=N

1.222 R319 (Offset = 0x13F)

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Table 1-224. R319 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_39:32	R/W	0x0	See Register 323

1.223 R320 (Offset = 0x140)

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Table 1-225. R320 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_31:24	R/W	0x0	See Register 323

1.224 R321 (Offset = 0x141)

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Table 1-226. R321 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_23:16	R/W	0x0	See Register 323

1.225 R322 (Offset = 0x142)

Return to the Summary Table.

Table 1-227. R322 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_15:8	R/W	0x0	See Register 323

1.226 R323 (Offset = 0x143)

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Table 1-228. R323 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM	R/W	0x0	DPLL Feedback Divider Numerator Value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.227 R324 (Offset = 0x144)

Return to the Summary Table.

Table 1-229. R324 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_39:32	R/W	0x0	See Register 328

1.228 R325 (Offset = 0x145)

Return to the Summary Table.

Table 1-230. R325 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_31:24	R/W	0x0	See Register 328

1.229 R326 (Offset = 0x146)

Return to the Summary Table.

Table 1-231. R326 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_23:16	R/W	0x0	See Register 328

1.230 R327 (Offset = 0x147)

Return to the Summary Table.

Table 1-232. R327 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_15:8	R/W	0x0	See Register 328

1.231 R328 (Offset = 0x148)

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Table 1-233. R328 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.232 R329 (Offset = 0x149)

Return to the Summary Table.

Table 1-234. R329 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL1_FB2_DIV_32:32	R/W	0x0	See Register 333

1.233 R330 (Offset = 0x14A)

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Table 1-235. R330 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV_31:24	R/W	0x0	See Register 333

1.234 R331 (Offset = 0x14B)

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Table 1-236. R331 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV_23:16	R/W	0x0	See Register 333

1.235 R332 (Offset = 0x14C)

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Table 1-237. R332 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV_15:8	R/W	0xF	See Register 333

1.236 R333 (Offset = 0x14D)

Return to the Summary Table.

Table 1-238. R333 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV	R/W	0xA0	DPLL Feedback Divider N Value used with DPLL1 feedback configuration 2. Divide value is programmed value except when using ZDM mode with FB div, actual divide value is +1. ROM=Y, EEPROM=N

1.237 R334 (Offset = 0x14E)

Return to the Summary Table.

Table 1-239. R334 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_39:32	R/W	0x0	See Register 338

1.238 R335 (Offset = 0x14F)

Return to the Summary Table.

Table 1-240. R335 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_31:24	R/W	0x0	See Register 338

1.239 R336 (Offset = 0x150)

Return to the Summary Table.

Table 1-241. R336 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_23:16	R/W	0x0	See Register 338

1.240 R337 (Offset = 0x151)

Return to the Summary Table.

Table 1-242. R337 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_15:8	R/W	0x0	See Register 338

1.241 R338 (Offset = 0x152)

Return to the Summary Table.

Table 1-243. R338 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM	R/W	0x0	DPLL Feedback Divider Numerator Value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.242 R339 (Offset = 0x153)

Return to the Summary Table.

Table 1-244. R339 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_39:32	R/W	0x0	See Register 343

1.243 R340 (Offset = 0x154)

Return to the Summary Table.

Table 1-245. R340 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_31:24	R/W	0x0	See Register 343

1.244 R341 (Offset = 0x155)

Return to the Summary Table.

Table 1-246. R341 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_23:16	R/W	0x0	See Register 343

1.245 R342 (Offset = 0x156)

Return to the Summary Table.

Table 1-247. R342 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_15:8	R/W	0x0	See Register 343

1.246 R343 (Offset = 0x157)

Return to the Summary Table.

Table 1-248. R343 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.247 R344 (Offset = 0x158)

Return to the Summary Table.

Table 1-249. R344 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL1_REF5_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF3. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
4	DPLL1_REF4_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF4. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
3	DPLL1_REF3_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF3. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
2	DPLL1_REF2_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF2. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
1	DPLL1_REF1_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF1. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

Table 1-249. R344 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DPLL1_REF0_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF0. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

1.248 R345 (Offset = 0x159)

Return to the Summary Table.

Table 1-250. R345 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:3	RESERVED	R	0x0	Reserved
2:0	DPLL1_FB_MASH_ORDER	R/W	0x2	DPLL Feedback Divider MASH Order. ROM=Y, EEPROM=N 0x0 = Integer 0x1 = 1st order 0x2 = 2nd order 0x3 = 3rd order 0x4 = 4th order

1.249 R346 (Offset = 0x15A)

Return to the Summary Table.

Table 1-251. R346 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_FB_FDEV_37:32	R/W	0x0	See Register 350

1.250 R347 (Offset = 0x15B)

Return to the Summary Table.

Table 1-252. R347 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV_31:24	R/W	0x0	See Register 350

1.251 R348 (Offset = 0x15C)

Return to the Summary Table.

Table 1-253. R348 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV_23:16	R/W	0x0	See Register 350

1.252 R349 (Offset = 0x15D)

Return to the Summary Table.

Table 1-254. R349 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV_15:8	R/W	0x0	See Register 350

1.253 R350 (Offset = 0x15E)

Return to the Summary Table.

Table 1-255. R350 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV	R/W	0x0	DPLL Feedback Divider DCO Frequency Deviation Value ROM=Y, EEPROM=N

1.254 R351 (Offset = 0x15F)

Return to the Summary Table.

Table 1-256. R351 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL1_FB_FDEV_UPDATE	R/W	0x0	Increment/Decrement DPLL Feedback Numerator value with DPLL_FB_FDEV value ROM=Y, EEPROM=N

1.255 R352 (Offset = 0x160)

Return to the Summary Table.

Table 1-257. R352 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL1_FB_FDEV_EN	R/W	0x0	Enable DPLL DCO mode ROM=Y, EEPROM=N

1.256 R353 (Offset = 0x161)

Return to the Summary Table.

Table 1-258. R353 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT_39:32	R	0x0	See Register 357

1.257 R354 (Offset = 0x162)

Return to the Summary Table.

Table 1-259. R354 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT_31:24	R	0x0	See Register 357

1.258 R355 (Offset = 0x163)

Return to the Summary Table.

Table 1-260. R355 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT_23:16	R	0x0	See Register 357

1.259 R356 (Offset = 0x164)

Return to the Summary Table.

Table 1-261. R356 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT_15:8	R	0x0	See Register 357

1.260 R357 (Offset = 0x165)

Return to the Summary Table.

Table 1-262. R357 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT	R	0x0	Readback DPLL Feedback Divider Numerator value as a result of DCO mode ROM=N, EEPROM=N

1.261 R358 (Offset = 0x166)

Return to the Summary Table.

Table 1-263. R358 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	DPLL1_REF0_DBLR_EN	R/W	0x0	DPLL Reference 0 Doubler Enable ROM=Y, EEPROM=N
2	DPLL1_REF1_DBLR_EN	R/W	0x0	DPLL Reference 1 Doubler Enable ROM=Y, EEPROM=N
1	DPLL1_REF2_DBLR_EN	R/W	0x0	DPLL Reference 2 Doubler Enable ROM=Y, EEPROM=N
0	DPLL1_REF3_DBLR_EN	R/W	0x0	DPLL Reference 3 Doubler Enable ROM=Y, EEPROM=N

1.262 R359 (Offset = 0x167)

Return to the Summary Table.

Table 1-264. R359 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF0_RDIV_15:8	R/W	0x0	See Register 360

1.263 R360 (Offset = 0x168)

Return to the Summary Table.

Table 1-265. R360 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF0_RDIV	R/W	0x7D	DPLL REF0 R-divider value ROM=Y, EEPROM=N

1.264 R361 (Offset = 0x169)

Return to the Summary Table.

Table 1-266. R361 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF1_RDIV_15:8	R/W	0x0	See Register 362

1.265 R362 (Offset = 0x16A)

Return to the Summary Table.

Table 1-267. R362 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF1_RDIV	R/W	0x8	DPLL REF1 R-divider value ROM=Y, EEPROM=N

1.266 R363 (Offset = 0x16B)

Return to the Summary Table.

Table 1-268. R363 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF2_RDIV_15:8	R/W	0x0	See Register 364

1.267 R364 (Offset = 0x16C)

Return to the Summary Table.

Table 1-269. R364 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF2_RDIV	R/W	0x0	DPLL REF2 R-divider value ROM=Y, EEPROM=N

1.268 R365 (Offset = 0x16D)

Return to the Summary Table.

Table 1-270. R365 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF3_RDIV_15:8	R/W	0x0	See Register 366

1.269 R366 (Offset = 0x16E)

Return to the Summary Table.

Table 1-271. R366 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF3_RDIV	R/W	0x0	DPLL REF3 R-divider value ROM=Y, EEPROM=N

1.270 R367 (Offset = 0x16F)

Return to the Summary Table.

Table 1-272. R367 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF4_RDIV_15:8	R/W	0x0	See Register 368

1.271 R368 (Offset = 0x170)

Return to the Summary Table.

Table 1-273. R368 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF4_RDIV	R/W	0x14	DPLL REF4 R-divider value ROM=Y, EEPROM=N

1.272 R369 (Offset = 0x171)

Return to the Summary Table.

Table 1-274. R369 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF5_RDIV_15:8	R/W	0x0	DPLL REF5 R-divider value. For use when DPLL1 uses output of VCO3 as a reference. ROM=Y, EEPROM=N

1.273 R370 (Offset = 0x172)

Return to the Summary Table.

Table 1-275. R370 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF5_RDIV	R/W	0x0	DPLL REF5 R-divider value. For use when DPLL1 uses output of VCO3 as a reference. ROM=Y, EEPROM=N

1.274 R373 (Offset = 0x175)

Return to the Summary Table.

Table 1-276. R373 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL2_REF0_AUTO_PRTY	R/W	0x2	REF0 Priority for Automatic Switchover. Sets the priority for REF0 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL2_REF1_AUTO_PRTY	R/W	0x0	REF1 Priority for Automatic Switchover. Sets the priority for REF1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.275 R374 (Offset = 0x176)

Return to the Summary Table.

Table 1-277. R374 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL2_REF2_AUTO_PRTY	R/W	0x0	REF2 Priority for Automatic Switchover. Sets the priority for REF2 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL2_REF3_AUTO_PRTY	R/W	0x0	REF3 Priority for Automatic Switchover. Sets the priority for REF3 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.276 R375 (Offset = 0x177)

Return to the Summary Table.

Table 1-278. R375 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL2_REF4_AUTO_PRTY	R/W	0x0	REF4 Priority for Automatic Switchover. Sets the priority for REF4 feedback from APLL1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

Table 1-278. R375 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DPLL2_REF5_AUTO_PRTY	R/W	0x0	REF5 Priority for Automatic Switchover. Sets the priority for REF5 feedback from APLL3 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.277 R376 (Offset = 0x178)

Return to the Summary Table.

Table 1-279. R376 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5:3	DPLL2_MAN_REFSEL	R/W	0x0	DPLL2 Manual Reference Selection ROM=Y, EEPROM=N 0x0 = REF0 0x1 = REF1 0x2 = REF2 0x3 = REF3 0x4 = PLL1 0x5 = PLL3
2	DPLL2_MAN_SWITCH_PIN_MODE	R/W	0x0	DPLL2 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = Register 0x1 = Pin
1:0	DPLL2_SWITCH_MODE	R/W	0x1	DPLL2 Reference Switchover Mode. Selects between Automatic Non-revertive, Automatic Revertive, Manual Selection with Automatic Fallback, and Manual Selection with Automatic Holdover. ROM=Y, EEPROM=N 0x0 = Auto non-revertive 0x1 = Auto revertive 0x2 = Manual with fallback 0x3 = Manual with holdover

1.278 R377 (Offset = 0x179)

Return to the Summary Table.

Table 1-280. R377 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_REFSEL_STAT	R	0x1	Reads the DPLL2 selected reference ROM=N, EEPROM=N 0x0 = Holdover 0x1 = REF0 0x2 = REF1 0x4 = REF2 0x8 = REF3 0x10 = APLL1 0x20 = APLL3

1.279 R378 (Offset = 0x17A)

Return to the Summary Table.

Table 1-281. R378 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_LOCKDET_PPM_EN	R/W	0x0	DPLL frequency lock detect enable ROM=Y, EEPROM=N
6:0	DPLL2_LOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 379

1.280 R379 (Offset = 0x17B)

Return to the Summary Table.

Table 1-282. R379 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_MAX	R/W	0xA	DPLL frequency lock detect in-lock threshold ROM=Y, EEPROM=N

1.281 R380 (Offset = 0x17C)

Return to the Summary Table.

Table 1-283. R380 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-283. R380 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	DPLL2_UNLOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 381

1.282 R381 (Offset = 0x17D)

Return to the Summary Table.

Table 1-284. R381 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_UNLOCKDET_PPM_MAX	R/W	0x64	DPLL frequency lock detect out-of-lock threshold ROM=Y, EEPROM=N

1.283 R382 (Offset = 0x17E)

Return to the Summary Table.

Table 1-285. R382 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_LOCKDET2_PPM_CNTSTRT_29:24	R/W	0x0	See Register 385

1.284 R383 (Offset = 0x17F)

Return to the Summary Table.

Table 1-286. R383 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET2_PPM_CNTSTRT_23:16	R/W	0x0	See Register 385

1.285 R384 (Offset = 0x180)

Return to the Summary Table.

Table 1-287. R384 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET2_PPM_CNTSTRT_15:8	R/W	0x9	See Register 385

1.286 R385 (Offset = 0x181)

Return to the Summary Table.

Table 1-288. R385 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET2_PPM_CNTSTRT	R/W	0xC5	DPLL frequency lock detect reference count value used with DPLL2 feedback configuration 2 ROM=Y, EEPROM=N

1.287 R386 (Offset = 0x182)

Return to the Summary Table.

Table 1-289. R386 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_LOCKDET_PPM_CNTSTRT_29:24	R/W	0x0	See Register 389

1.288 R387 (Offset = 0x183)

Return to the Summary Table.

Table 1-290. R387 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_CNTSTRT_23:16	R/W	0xF	See Register 389

1.289 R388 (Offset = 0x184)

Return to the Summary Table.

Table 1-291. R388 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_CNTSTRT_15:8	R/W	0xE5	See Register 389

1.290 R389 (Offset = 0x185)

Return to the Summary Table.

Table 1-292. R389 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_CNTSTRT	R/W	0x3	DPLL frequency lock detect reference count value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.291 R390 (Offset = 0x186)

Return to the Summary Table.

Table 1-293. R390 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_29:24	R/W	0x0	See Register 393

1.292 R391 (Offset = 0x187)

Return to the Summary Table.

Table 1-294. R391 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_23:16	R/W	0x98	See Register 393

1.293 R392 (Offset = 0x188)

Return to the Summary Table.

Table 1-295. R392 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_VCO_PPM_CNT STRT_15:8	R/W	0x96	See Register 393

1.294 R393 (Offset = 0x189)

Return to the Summary Table.

Table 1-296. R393 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_VCO_PPM_CNT STRT	R/W	0x83	DPLL frequency lock detect VCO count value ROM=Y, EEPROM=N

1.295 R394 (Offset = 0x18A)

Return to the Summary Table.

Table 1-297. R394 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R	0x0	Reserved
0	DPLL2_STATUS_PPM_LOCK	R	0x1	Readback lock indicator from DPLL PPM Checker ROM=N, EEPROM=N

1.296 R397 (Offset = 0x18D)

Return to the Summary Table.

Table 1-298. R397 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_LOOP_EN	R/W	0x0	Enable DPLL2 loop filter and R-Div mash engine ROM=Y, EEPROM=N
6	DPLL2_PHASE_CANCEL_EN	R/W	0x1	Enable Phase Cancellation ROM=Y, EEPROM=N
5	DPLL2_FASTLOCK_ALWAYS	R/W	0x0	Always perform fastlock. No phase cancellation is done. ROM=Y, EEPROM=N
4	DPLL2_PHS1_EN	R/W	0x1	Enable holdover exit phase slew control . ROM=Y, EEPROM=N
3	DPLL2_ZDM_EN	R/W	0x0	Enable Zero Delay ROM=Y, EEPROM=N

Table 1-298. R397 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DPLL2_HIST_EN	R/W	0x1	Enable History word to be used during holdover ROM=Y, EEPROM=N
1	DPLL2_PHASE_CANCEL_ALWAYS	R/W	0x0	Force phase cancellation to always occur when DPLL is acquiring lock ROM=Y, EEPROM=N
0	RESERVED	R	0x0	Reserved

1.297 R398 (Offset = 0x18E)

Return to the Summary Table.

Table 1-299. R398 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_HOLD_SLEW_LIM_EN	R/W	0x0	Enable slew limiter when entering holdover ROM=Y, EEPROM=N
6:0	RESERVED	R	0x0	Reserved

1.298 R400 (Offset = 0x190)

Return to the Summary Table.

Table 1-300. R400 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL2_PH_OFFSET_44:40	R/W	0x0	See Register 405

1.299 R401 (Offset = 0x191)

Return to the Summary Table.

Table 1-301. R401 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_39:32	R/W	0x0	See Register 405

1.300 R402 (Offset = 0x192)

Return to the Summary Table.

Table 1-302. R402 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_31:24	R/W	0x0	See Register 405

1.301 R403 (Offset = 0x193)

Return to the Summary Table.

Table 1-303. R403 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_23:16	R/W	0x0	See Register 405

1.302 R404 (Offset = 0x194)

Return to the Summary Table.

Table 1-304. R404 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_15:8	R/W	0x0	See Register 405

1.303 R405 (Offset = 0x195)

Return to the Summary Table.

Table 1-305. R405 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET	R/W	0x0	Phase offset to adjust and calibrate input to output phase in ZDM. This is a 2s complement number. ROM=Y, EEPROM=N

1.304 R406 (Offset = 0x196)

Return to the Summary Table.

Table 1-306. R406 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_39:32	R/W	0x0	See Register 410

1.305 R407 (Offset = 0x197)

Return to the Summary Table.

Table 1-307. R407 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_31:24	R/W	0x0	See Register 410

1.306 R408 (Offset = 0x198)

Return to the Summary Table.

Table 1-308. R408 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_23:16	R/W	0x0	See Register 410

1.307 R409 (Offset = 0x199)

Return to the Summary Table.

Table 1-309. R409 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_15:8	R/W	0x0	See Register 410

1.308 R410 (Offset = 0x19A)

Return to the Summary Table.

Table 1-310. R410 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN	R/W	0x0	DPLL2 starting word. Also non-history holdover word. ROM=Y, EEPROM=N

1.309 R411 (Offset = 0x19B)

Return to the Summary Table.

Table 1-311. R411 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-311. R411 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DPLL2_1PPS_MODE	R/W	0x0	Set when using 1-PPS input ROM=Y, EEPROM=N
5	DPLL2_1PPS_EN	R/W	0x0	Set when using 1-PPS input ROM=Y, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.310 R440 (Offset = 0x1B8)

Return to the Summary Table.

Table 1-312. R440 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_LCK_TIMER_9:8	R/W	0x2	See Register 441

1.311 R441 (Offset = 0x1B9)

Return to the Summary Table.

Table 1-313. R441 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LCK_TIMER	R/W	0xB	Minimum amount of time until DPLL2_LOPL will be deasserted after starting to lock. Timer begins once device is within valid phase lock window. ROM=Y, EEPROM=N

1.312 R442 (Offset = 0x1BA)

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Table 1-314. R442 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_HIST_TIMER_9:8	R/W	0x1	See Register 443

1.313 R443 (Offset = 0x1BB)

Return to the Summary Table.

Table 1-315. R443 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_HIST_TIMER	R/W	0x92	Time interval between history update events. ROM=Y, EEPROM=N

1.314 R444 (Offset = 0x1BC)

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Table 1-316. R444 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_HOLD_TIMER_9:8	R/W	0x1	See Register 445

1.315 R445 (Offset = 0x1BD)

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Table 1-317. R445 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_HOLD_TIMER	R/W	0x42	Rate of change to DPLL or APLL numerator during phase slew control. See DPLLx_HOLD_SLEW_STEP. ROM=Y, EEPROM=N

1.316 R446 (Offset = 0x1BE)

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Table 1-318. R446 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_PHS1_TIMER_9:8	R/W	0x1	See Register 447

1.317 R447 (Offset = 0x1BF)

Return to the Summary Table.

Table 1-319. R447 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PHS1_TIMER	R/W	0x40	Holdover exit phase slew control. Timer controlling update period. ROM=Y, EEPROM=N

1.318 R452 (Offset = 0x1C4)

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Table 1-320. R452 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL2_HIST_GAIN	R/W	0x8	History filter gain ROM=Y, EEPROM=N

1.319 R453 (Offset = 0x1C5)

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Table 1-321. R453 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_PL_THRESH	R/W	0x20	Phase lock in-lock threshold ROM=Y, EEPROM=N

1.320 R454 (Offset = 0x1C6)

Return to the Summary Table.

Table 1-322. R454 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_PL_UNLK_THRESH	R/W	0x22	Phase lock out-of-lock threshold ROM=Y, EEPROM=N

1.321 R455 (Offset = 0x1C7)

Return to the Summary Table.

Table 1-323. R455 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_PHS1_THRESH	R/W	0x7	Holdover exit phase slew control. Change per timer event. ROM=Y, EEPROM=N

1.322 R458 (Offset = 0x1CA)

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Table 1-324. R458 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_HOLD_SLEW_STEP	R/W	0x3F	When DPLL exits holdover, rate of phase change relates to DPLLx_HOLD_SLEW_STEP over DPLLx_HOLD_TIMER. DPLLx_HOLD_SLEW_STEP is applied to DPLL numerator when exiting holdover or APLL numerator when using APLL relative DCO. ROM=Y, EEPROM=N

1.323 R460 (Offset = 0x1CC)

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Table 1-325. R460 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	DPLL2_STATUS_PL	R	0x1	Readback the phase lock status ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.324 R461 (Offset = 0x1CD)

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Table 1-326. R461 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	DPLL2_DCO_SLEW_ACTIVE	R	0x0	Readback DCO slew status ROM=N, EEPROM=N

Table 1-326. R461 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	R	0x0	Reserved

1.325 R464 (Offset = 0x1D0)

Return to the Summary Table.

Table 1-327. R464 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB_DIV_32:32	R/W	0x0	See Register 468

1.326 R465 (Offset = 0x1D1)

Return to the Summary Table.

Table 1-328. R465 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV_31:24	R/W	0x0	See Register 468

1.327 R466 (Offset = 0x1D2)

Return to the Summary Table.

Table 1-329. R466 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV_23:16	R/W	0x0	See Register 468

1.328 R467 (Offset = 0x1D3)

Return to the Summary Table.

Table 1-330. R467 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV_15:8	R/W	0x2	See Register 468

1.329 R468 (Offset = 0x1D4)

Return to the Summary Table.

Table 1-331. R468 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV	R/W	0x40	DPLL Feedback Divider N Value used with DPLL2 feedback configuration 1. Divide value is programmed value except when using ZDM mode with FB div, actual divide value is +1. ROM=Y, EEPROM=N

1.330 R469 (Offset = 0x1D5)

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Table 1-332. R469 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_39:32	R/W	0x0	See Register 473

1.331 R470 (Offset = 0x1D6)

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Table 1-333. R470 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_31:24	R/W	0x0	See Register 473

1.332 R471 (Offset = 0x1D7)

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Table 1-334. R471 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_23:16	R/W	0x0	See Register 473

1.333 R472 (Offset = 0x1D8)

Return to the Summary Table.

Table 1-335. R472 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_15:8	R/W	0x0	See Register 473

1.334 R473 (Offset = 0x1D9)

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Table 1-336. R473 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM	R/W	0x0	DPLL Feedback Divider Numerator Value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.335 R474 (Offset = 0x1DA)

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Table 1-337. R474 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_39:32	R/W	0x0	See Register 478

1.336 R475 (Offset = 0x1DB)

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Table 1-338. R475 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_31:24	R/W	0x0	See Register 478

1.337 R476 (Offset = 0x1DC)

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Table 1-339. R476 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_23:16	R/W	0x0	See Register 478

1.338 R477 (Offset = 0x1DD)

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Table 1-340. R477 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_15:8	R/W	0x0	See Register 478

1.339 R478 (Offset = 0x1DE)

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Table 1-341. R478 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.340 R479 (Offset = 0x1DF)

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Table 1-342. R479 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB2_DIV_32:32	R/W	0x0	See Register 483

1.341 R480 (Offset = 0x1E0)

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Table 1-343. R480 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV_31:24	R/W	0x0	See Register 483

1.342 R481 (Offset = 0x1E1)

Return to the Summary Table.

Table 1-344. R481 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV_23:16	R/W	0x0	See Register 483

1.343 R482 (Offset = 0x1E2)

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Table 1-345. R482 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV_15:8	R/W	0x2	See Register 483

1.344 R483 (Offset = 0x1E3)

Return to the Summary Table.

Table 1-346. R483 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV	R/W	0x32	DPLL Feedback Divider N Value used with DPLL2 feedback configuration 2. Divide value is programmed value except when using ZDM mode with FB div, actual divide value is +1. ROM=Y, EEPROM=N

1.345 R484 (Offset = 0x1E4)

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Table 1-347. R484 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_39:32	R/W	0x80	See Register 488

1.346 R485 (Offset = 0x1E5)

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Table 1-348. R485 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_31:24	R/W	0x0	See Register 488

1.347 R486 (Offset = 0x1E6)

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Table 1-349. R486 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_23:16	R/W	0x0	See Register 488

1.348 R487 (Offset = 0x1E7)

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Table 1-350. R487 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_15:8	R/W	0x0	See Register 488

1.349 R488 (Offset = 0x1E8)

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Table 1-351. R488 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM	R/W	0x0	DPLL Feedback Divider Numerator Value used with DPLL2 feedback configuration 2 ROM=Y, EEPROM=N

1.350 R489 (Offset = 0x1E9)

Return to the Summary Table.

Table 1-352. R489 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_39:32	R/W	0x0	See Register 493

1.351 R490 (Offset = 0x1EA)

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Table 1-353. R490 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_31:24	R/W	0x0	See Register 493

1.352 R491 (Offset = 0x1EB)

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Table 1-354. R491 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_23:16	R/W	0x0	See Register 493

1.353 R492 (Offset = 0x1EC)

Return to the Summary Table.

Table 1-355. R492 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_15:8	R/W	0x0	See Register 493

1.354 R493 (Offset = 0x1ED)

Return to the Summary Table.

Table 1-356. R493 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL2 feedback configuration 2 ROM=Y, EEPROM=N

1.355 R494 (Offset = 0x1EE)

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Table 1-357. R494 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL2_REF5_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF3. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
4	DPLL2_REF4_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF4. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

Table 1-357. R494 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DPLL2_REF3_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF3. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
2	DPLL2_REF2_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF2. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
1	DPLL2_REF1_FB_SEL	R/W	0x1	DPLL Feedback N, NUM, DEN select for REF1. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
0	DPLL2_REF0_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF0. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

1.356 R495 (Offset = 0x1EF)

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Table 1-358. R495 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:3	RESERVED	R	0x0	Reserved
2:0	DPLL2_FB_MASH_ORDER	R/W	0x2	DPLL Feedback Divider MASH Order. ROM=Y, EEPROM=N 0x0 = Integer 0x1 = 1st order 0x2 = 2nd order 0x3 = 3rd order 0x4 = 4th order

1.357 R496 (Offset = 0x1F0)

Return to the Summary Table.

Table 1-359. R496 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_FB_FDEV_37:32	R/W	0x0	See Register 500

1.358 R497 (Offset = 0x1F1)

Return to the Summary Table.

Table 1-360. R497 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV_31:24	R/W	0x0	See Register 500

1.359 R498 (Offset = 0x1F2)

Return to the Summary Table.

Table 1-361. R498 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV_23:16	R/W	0x0	See Register 500

1.360 R499 (Offset = 0x1F3)

Return to the Summary Table.

Table 1-362. R499 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV_15:8	R/W	0x0	See Register 500

1.361 R500 (Offset = 0x1F4)

Return to the Summary Table.

Table 1-363. R500 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV	R/W	0x0	DPLL Feedback Divider DCO Frequency Deviation Value ROM=Y, EEPROM=N

1.362 R501 (Offset = 0x1F5)

Return to the Summary Table.

Table 1-364. R501 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB_FDEV_UPDATE	R/W	0x0	Increment/Decrement DPLL Feedback Numerator value with DPLL_FB_FDEV value ROM=Y, EEPROM=N

1.363 R502 (Offset = 0x1F6)

Return to the Summary Table.

Table 1-365. R502 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB_FDEV_EN	R/W	0x0	Enable DPLL DCO mode ROM=Y, EEPROM=N

1.364 R503 (Offset = 0x1F7)

Return to the Summary Table.

Table 1-366. R503 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_39:32	R	0x0	See Register 507

1.365 R504 (Offset = 0x1F8)

Return to the Summary Table.

Table 1-367. R504 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_31:24	R	0x0	See Register 507

1.366 R505 (Offset = 0x1F9)

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Table 1-368. R505 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_23:16	R	0x0	See Register 507

1.367 R506 (Offset = 0x1FA)

Return to the Summary Table.

Table 1-369. R506 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_15:8	R	0x0	See Register 507

1.368 R507 (Offset = 0x1FB)

Return to the Summary Table.

Table 1-370. R507 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT	R	0x0	Readback DPLL Feedback Divider Numerator value as a result of DCO mode ROM=N, EEPROM=N

1.369 R508 (Offset = 0x1FC)

Return to the Summary Table.

Table 1-371. R508 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	DPLL2_REF0_DBLR_EN	R/W	0x0	DPLL Reference 0 Doubler Enable ROM=Y, EEPROM=N
2	DPLL2_REF1_DBLR_EN	R/W	0x0	DPLL Reference 1 Doubler Enable ROM=Y, EEPROM=N
1	DPLL2_REF2_DBLR_EN	R/W	0x0	DPLL Reference 2 Doubler Enable ROM=Y, EEPROM=N
0	DPLL2_REF3_DBLR_EN	R/W	0x0	DPLL Reference 3 Doubler Enable ROM=Y, EEPROM=N

1.370 R509 (Offset = 0x1FD)

Return to the Summary Table.

Table 1-372. R509 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF0_RDIV_15:8	R/W	0x0	See Register 510

1.371 R510 (Offset = 0x1FE)

Return to the Summary Table.

Table 1-373. R510 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF0_RDIV	R/W	0x10	DPLL Reference 0 R divider value ROM=Y, EEPROM=N

1.372 R511 (Offset = 0x1FF)

Return to the Summary Table.

Table 1-374. R511 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF1_RDIV_15:8	R/W	0x0	See Register 512

1.373 R512 (Offset = 0x200)

Return to the Summary Table.

Table 1-375. R512 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF1_RDIV	R/W	0x0	DPLL Reference 1 R divider value ROM=Y, EEPROM=N

1.374 R513 (Offset = 0x201)

Return to the Summary Table.

Table 1-376. R513 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF2_RDIV_15:8	R/W	0x0	See Register 514

1.375 R514 (Offset = 0x202)

Return to the Summary Table.

Table 1-377. R514 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF2_RDIV	R/W	0x0	DPLL Reference 2 R divider value ROM=Y, EEPROM=N

1.376 R515 (Offset = 0x203)

Return to the Summary Table.

Table 1-378. R515 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF3_RDIV_15:8	R/W	0x0	See Register 516

1.377 R516 (Offset = 0x204)

Return to the Summary Table.

Table 1-379. R516 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF3_RDIV	R/W	0x0	DPLL Reference 3 R divider value ROM=Y, EEPROM=N

1.378 R517 (Offset = 0x205)

Return to the Summary Table.

Table 1-380. R517 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF4_RDIV_15:8	R/W	0x0	See Register 518

1.379 R518 (Offset = 0x206)

Return to the Summary Table.

Table 1-381. R518 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF4_RDIV	R/W	0x0	DPLL REF4 R-divider value ROM=Y, EEPROM=N

1.380 R519 (Offset = 0x207)

Return to the Summary Table.

Table 1-382. R519 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF5_RDIV_15:8	R/W	0x0	See Register 520

1.381 R520 (Offset = 0x208)

Return to the Summary Table.

Table 1-383. R520 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF5_RDIV	R/W	0x0	DPLL Reference 3 R divider value ROM=Y, EEPROM=N

1.382 R523 (Offset = 0x20B)

Return to the Summary Table.

Table 1-384. R523 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-384. R523 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	DPLL3_REF0_AUTO_PRTY	R/W	0x2	REF0 Priority for Automatic Switchover. Sets the priority for REF0 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL3_REF1_AUTO_PRTY	R/W	0x1	REF1 Priority for Automatic Switchover. Sets the priority for REF1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.383 R524 (Offset = 0x20C)

Return to the Summary Table.

Table 1-385. R524 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL3_REF2_AUTO_PRTY	R/W	0x0	REF2 Priority for Automatic Switchover. Sets the priority for REF2 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

Table 1-385. R524 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DPLL3_REF3_AUTO_PRTY	R/W	0x0	REF3 Priority for Automatic Switchover. Sets the priority for REF3 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.384 R525 (Offset = 0x20D)

Return to the Summary Table.

Table 1-386. R525 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL3_REF4_AUTO_PRTY	R/W	0x0	REF4 Priority for Automatic Switchover. Sets the priority for REF4 feedback from APLL1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL3_REF5_AUTO_PRTY	R/W	0x0	REF5 Priority for Automatic Switchover. Sets the priority for REF5 feedback from APLL2 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.385 R526 (Offset = 0x20E)

Return to the Summary Table.

Table 1-387. R526 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5:3	DPLL3_MAN_REFSEL	R/W	0x0	DPLL3 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = REF0 0x1 = REF1 0x2 = REF2 0x3 = REF3 0x4 = PLL1 0x5 = PLL2
2	DPLL3_MAN_SWITCH_PIN_MODE	R/W	0x0	DPLL3 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = Register 0x1 = Pin
1:0	DPLL3_SWITCH_MODE	R/W	0x1	DPLL3 Reference Switchover Mode. Selects between Automatic Non-revertive, Automatic Revertive, Manual Selection with Automatic Fallback, and Manual Selection with Automatic Holdover. ROM=Y, EEPROM=N 0x0 = Auto non-revertive 0x1 = Auto revertive 0x2 = Manual with fallback 0x3 = Manual with holdover

1.386 R527 (Offset = 0x20F)

Return to the Summary Table.

Table 1-388. R527 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-388. R527 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DPLL3_REFSEL_STAT	R	0x2	Reads the DPLL3 selected reference ROM=N, EEPROM=N 0x0 = Holdover 0x1 = REF0 0x2 = REF1 0x4 = REF2 0x8 = REF3 0x10 = APLL1 0x20 = APLL2

1.387 R528 (Offset = 0x210)

Return to the Summary Table.

Table 1-389. R528 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL3_LOCKDET_PPM_EN	R/W	0x1	DPLL frequency lock detect enable ROM=Y, EEPROM=N
6:0	DPLL3_LOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 529

1.388 R529 (Offset = 0x211)

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Table 1-390. R529 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_PPM_MAX	R/W	0xA	DPLL frequency lock detect in-lock threshold ROM=Y, EEPROM=N

1.389 R530 (Offset = 0x212)

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Table 1-391. R530 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL3_UNLOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 531

1.390 R531 (Offset = 0x213)

Return to the Summary Table.

Table 1-392. R531 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_UNLOCKDET_PPM_MAX	R/W	0x64	DPLL frequency lock detect out-of-lock threshold ROM=Y, EEPROM=N

1.391 R532 (Offset = 0x214)

Return to the Summary Table.

Table 1-393. R532 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_LOCKDET2_PPM_CNTSTRT_29:24	R/W	0x0	See Register 535

1.392 R533 (Offset = 0x215)

Return to the Summary Table.

Table 1-394. R533 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET2_PPM_CNTSTRT_23:16	R/W	0x3	See Register 535

1.393 R534 (Offset = 0x216)

Return to the Summary Table.

Table 1-395. R534 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET2_PPM_CNTSTRT_15:8	R/W	0xD	See Register 535

1.394 R535 (Offset = 0x217)

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Table 1-396. R535 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET2_PPM_CNTSTRT	R/W	0x40	DPLL frequency lock detect reference count value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.395 R536 (Offset = 0x218)

Return to the Summary Table.

Table 1-397. R536 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_LOCKDET_PPM_CNTSTRT_29:24	R/W	0x0	See Register 539

1.396 R537 (Offset = 0x219)

Return to the Summary Table.

Table 1-398. R537 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_PPM_CNTSTRT_23:16	R/W	0x1	See Register 539

1.397 R538 (Offset = 0x21A)

Return to the Summary Table.

Table 1-399. R538 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_PPM_CNTSTRT_15:8	R/W	0xDC	See Register 539

1.398 R539 (Offset = 0x21B)

Return to the Summary Table.

Table 1-400. R539 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_PPM_CNTSTRT	R/W	0xD7	DPLL frequency lock detect reference count value used with DPLL3 feedback configuration 1 ROM=Y, EEPROM=N

1.399 R540 (Offset = 0x21C)

Return to the Summary Table.

Table 1-401. R540 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_LOCKDET_VCO_PPM_CNTSTRT_29:24	R/W	0x0	See Register 543

1.400 R541 (Offset = 0x21D)

Return to the Summary Table.

Table 1-402. R541 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_VCO_PPM_CNTSTRT_23:16	R/W	0x98	See Register 543

1.401 R542 (Offset = 0x21E)

Return to the Summary Table.

Table 1-403. R542 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_VCO_PPM_CNTSTRT_15:8	R/W	0x96	See Register 543

1.402 R543 (Offset = 0x21F)

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Table 1-404. R543 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_VCO_PPM_CNTSTRT	R/W	0xB8	DPLL frequency lock detect VCO count value ROM=Y, EEPROM=N

1.403 R544 (Offset = 0x220)

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Table 1-405. R544 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R	0x0	Reserved
0	DPLL3_STATUS_PPM_LOCK	R	0x1	Readback lock indicator from DPLL PPM Checker ROM=N, EEPROM=N

1.404 R547 (Offset = 0x223)

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Table 1-406. R547 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL3_LOOP_EN	R/W	0x1	Enable DPLL3 loop filter and R-Div mash engine ROM=Y, EEPROM=N
6	DPLL3_PHASE_CANCEL_EN	R/W	0x1	Enable Phase Cancellation ROM=Y, EEPROM=N
5	DPLL3_FASTLOCK_ALWAYS	R/W	0x0	Always perform fastlock. No phase cancellation is done. ROM=Y, EEPROM=N
4	DPLL3_PHS1_EN	R/W	0x1	Enable holdover exit phase slew control . ROM=Y, EEPROM=N
3	DPLL3_ZDM_EN	R/W	0x0	Enable Zero Delay mode ROM=Y, EEPROM=N
2	DPLL3_HIST_EN	R/W	0x1	Enable History word to be used during holdover ROM=Y, EEPROM=N
1	DPLL3_PHASE_CANCEL_ALWAYS	R/W	0x0	Force phase cancellation to always occur when DPLL is acquiring lock. ROM=Y, EEPROM=N
0	RESERVED	R	0x0	Reserved

1.405 R548 (Offset = 0x224)

Return to the Summary Table.

Table 1-407. R548 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL3_HOLD_SLEW_LIM_EN	R/W	0x0	During holdover enable slew limiter ROM=Y, EEPROM=N
6:0	RESERVED	R	0x0	Reserved

1.406 R550 (Offset = 0x226)

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Table 1-408. R550 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL3_PH_OFFSET_44:40	R/W	0x0	See Register 555

1.407 R551 (Offset = 0x227)

Return to the Summary Table.

Table 1-409. R551 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET_39:32	R/W	0x0	See Register 555

1.408 R552 (Offset = 0x228)

Return to the Summary Table.

Table 1-410. R552 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET_31:24	R/W	0x0	See Register 555

1.409 R553 (Offset = 0x229)

Return to the Summary Table.

Table 1-411. R553 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET_23:16	R/W	0x0	See Register 555

1.410 R554 (Offset = 0x22A)

Return to the Summary Table.

Table 1-412. R554 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET_15:8	R/W	0x0	See Register 555

1.411 R555 (Offset = 0x22B)

Return to the Summary Table.

Table 1-413. R555 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET	R/W	0x0	Phase offset to adjust and calibrate input to output phase in ZDM. This is a 2s complement number. ROM=Y, EEPROM=N

1.412 R556 (Offset = 0x22C)

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Table 1-414. R556 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN_39:32	R/W	0x0	See Register 560

1.413 R557 (Offset = 0x22D)

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Table 1-415. R557 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN_31:24	R/W	0x0	See Register 560

1.414 R558 (Offset = 0x22E)

Return to the Summary Table.

Table 1-416. R558 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN_23:16	R/W	0x0	See Register 560

1.415 R559 (Offset = 0x22F)

Return to the Summary Table.

Table 1-417. R559 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN_15:8	R/W	0x0	See Register 560

1.416 R560 (Offset = 0x230)

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Table 1-418. R560 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN	R/W	0x0	DPLL starting word. Also non-history holdover word. ROM=Y, EEPROM=N

1.417 R561 (Offset = 0x231)

Return to the Summary Table.

Table 1-419. R561 Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL3_PPM_REF_SEL	R/W	0x0	PPM Detector Reference Selection for DPLL3 LOFL. When set to 0, the selected DPLL input reference is used resulting in DPLL3 LOFL as expected. When set to 1, the XO is used as a frequency enabling LOFL for APLL3, no DPLL is required. This bit enables a "BAW LOCK" indicator. ROM=Y, EEPROM=N 0x0 = LOFL_DPLL3 = DPLL3 DLD 0x1 = LOFL_DPLL3 = APLL3 DLD
6	DPLL3_1PPS_MODE	R/W	0x0	Set when using 1-PPS input ROM=Y, EEPROM=N
5	DPLL3_1PPS_EN	R/W	0x0	Set when using 1-PPS input ROM=Y, EEPROM=N

Table 1-419. R561 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	RESERVED	R	0x0	Reserved

1.418 R590 (Offset = 0x24E)

Return to the Summary Table.

Table 1-420. R590 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL3_LCK_TIMER_9:8	R/W	0x2	See Register 591

1.419 R591 (Offset = 0x24F)

Return to the Summary Table.

Table 1-421. R591 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LCK_TIMER	R/W	0x90	Minimum amount of time until DPLL3_LOPL will be deasserted after starting to lock. Timer begins once device is within valid phase lock window. ROM=Y, EEPROM=N

1.420 R592 (Offset = 0x250)

Return to the Summary Table.

Table 1-422. R592 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL3_HIST_TIMER_9:8	R/W	0x1	See Register 593

1.421 R593 (Offset = 0x251)

Return to the Summary Table.

Table 1-423. R593 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_HIST_TIMER	R/W	0x92	History timer ROM=Y, EEPROM=N

1.422 R594 (Offset = 0x252)

Return to the Summary Table.

Table 1-424. R594 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R	0x0	Reserved
1:0	DPLL3_HOLD_TIMER_9:8	R/W	0x1	See Register 595

1.423 R595 (Offset = 0x253)

Return to the Summary Table.

Table 1-425. R595 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_HOLD_TIMER	R/W	0x42	Rate of change to DPLL or APLL numerator during phase slew control. See DPLLx_HOLD_SLEW_STEP. ROM=Y, EEPROM=N

1.424 R596 (Offset = 0x254)

Return to the Summary Table.

Table 1-426. R596 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL3_PHS1_TIMER_9:8	R/W	0x1	See Register 597

1.425 R597 (Offset = 0x255)

Return to the Summary Table.

Table 1-427. R597 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PHS1_TIMER	R/W	0x40	Holdover exit phase slew control. Timer controlling update period. ROM=Y, EEPROM=N

1.426 R602 (Offset = 0x25A)

Return to the Summary Table.

Table 1-428. R602 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL3_HIST_GAIN	R/W	0x8	History filter gain ROM=Y, EEPROM=N

1.427 R603 (Offset = 0x25B)

Return to the Summary Table.

Table 1-429. R603 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_PL_THRESH	R/W	0x24	Phase lock in-lock threshold ROM=Y, EEPROM=N

1.428 R604 (Offset = 0x25C)

Return to the Summary Table.

Table 1-430. R604 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_PL_UNLK_THRESH	R/W	0x26	Phase lock out-of-lock threshold ROM=Y, EEPROM=N

1.429 R605 (Offset = 0x25D)

Return to the Summary Table.

Table 1-431. R605 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_PHS1_THRESH	R/W	0x7	Holdover exit phase slew control. Change per timer event. ROM=Y, EEPROM=N

1.430 R610 (Offset = 0x262)

Return to the Summary Table.

Table 1-432. R610 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	DPLL3_STATUS_PL	R	0x1	Readback the phase lock status ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.431 R611 (Offset = 0x263)

Return to the Summary Table.

Table 1-433. R611 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	DPLL3_DCO_SLEW_ACTIVE	R	0x0	Readback DCO slew status ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.432 R614 (Offset = 0x266)

Return to the Summary Table.

Table 1-434. R614 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL3_FB_DIV_32:32	R/W	0x0	See Register 618

1.433 R615 (Offset = 0x267)

Return to the Summary Table.

Table 1-435. R615 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DIV_31:24	R/W	0x0	See Register 618

1.434 R616 (Offset = 0x268)

Return to the Summary Table.

Table 1-436. R616 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DIV_23:16	R/W	0x0	See Register 618

1.435 R617 (Offset = 0x269)

Return to the Summary Table.

Table 1-437. R617 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DIV_15:8	R/W	0x7	See Register 618

1.436 R618 (Offset = 0x26A)

Return to the Summary Table.

Table 1-438. R618 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DIV	R/W	0xAE	DPLL Feedback Divider N Value used with DPLL3 feedback configuration 1. Divide value is programmed value except when using ZDM mode with FB div, actual divide value is +1. ROM=Y, EEPROM=N

1.437 R619 (Offset = 0x26B)

Return to the Summary Table.

Table 1-439. R619 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_39:32	R/W	0x14	See Register 623

1.438 R620 (Offset = 0x26C)

Return to the Summary Table.

Table 1-440. R620 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_31:24	R/W	0x7A	See Register 623

1.439 R621 (Offset = 0x26D)

Return to the Summary Table.

Table 1-441. R621 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_23:16	R/W	0xE1	See Register 623

1.440 R622 (Offset = 0x26E)

Return to the Summary Table.

Table 1-442. R622 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_15:8	R/W	0x47	See Register 623

1.441 R623 (Offset = 0x26F)

Return to the Summary Table.

Table 1-443. R623 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM	R/W	0xAE	DPLL Feedback Divider Numerator Value used with DPLL3 feedback configuration 1 ROM=Y, EEPROM=N

1.442 R624 (Offset = 0x270)

Return to the Summary Table.

Table 1-444. R624 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN_39:32	R/W	0xFF	See Register 628

1.443 R625 (Offset = 0x271)

Return to the Summary Table.

Table 1-445. R625 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN_31:24	R/W	0xFF	See Register 628

1.444 R626 (Offset = 0x272)

Return to the Summary Table.

Table 1-446. R626 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN_23:16	R/W	0xFF	See Register 628

1.445 R627 (Offset = 0x273)

Return to the Summary Table.

Table 1-447. R627 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN_15:8	R/W	0xFF	See Register 628

1.446 R628 (Offset = 0x274)

Return to the Summary Table.

Table 1-448. R628 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN	R/W	0xFF	DPLL Feedback Divider Denominator Value used with DPLL3 feedback configuration 1 ROM=Y, EEPROM=N

1.447 R629 (Offset = 0x275)

Return to the Summary Table.

Table 1-449. R629 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL3_FB2_DIV_32:32	R/W	0x0	See Register 633

1.448 R630 (Offset = 0x276)

Return to the Summary Table.

Table 1-450. R630 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DIV_31:24	R/W	0x0	See Register 633

1.449 R631 (Offset = 0x277)

Return to the Summary Table.

Table 1-451. R631 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DIV_23:16	R/W	0x0	See Register 633

1.450 R632 (Offset = 0x278)

Return to the Summary Table.

Table 1-452. R632 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DIV_15:8	R/W	0x0	See Register 633

1.451 R633 (Offset = 0x279)

Return to the Summary Table.

Table 1-453. R633 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DIV	R/W	0xF5	DPLL Feedback Divider N Value used with DPLL3 feedback configuration 2. Divide value is programmed value except when using ZDM mode with FB div, actual divide value is +1. ROM=Y, EEPROM=N

1.452 R634 (Offset = 0x27A)

Return to the Summary Table.

Table 1-454. R634 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM_39:32	R/W	0xC2	See Register 638

1.453 R635 (Offset = 0x27B)

Return to the Summary Table.

Table 1-455. R635 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM_31:24	R/W	0x8F	See Register 638

1.454 R636 (Offset = 0x27C)

Return to the Summary Table.

Table 1-456. R636 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM_23:16	R/W	0x5C	See Register 638

1.455 R637 (Offset = 0x27D)

Return to the Summary Table.

Table 1-457. R637 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM_15:8	R/W	0x28	See Register 638

1.456 R638 (Offset = 0x27E)

Return to the Summary Table.

Table 1-458. R638 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM	R/W	0xF5	DPLL Feedback Divider Numerator Value used with DPLL3 feedback configuration 2 ROM=Y, EEPROM=N

1.457 R639 (Offset = 0x27F)

Return to the Summary Table.

Table 1-459. R639 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN_39:32	R/W	0xFF	See Register 643

1.458 R640 (Offset = 0x280)

Return to the Summary Table.

Table 1-460. R640 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN_31:24	R/W	0xFF	See Register 643

1.459 R641 (Offset = 0x281)

Return to the Summary Table.

Table 1-461. R641 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN_23:16	R/W	0xFF	See Register 643

1.460 R642 (Offset = 0x282)

Return to the Summary Table.

Table 1-462. R642 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN_15:8	R/W	0xFF	See Register 643

1.461 R643 (Offset = 0x283)

Return to the Summary Table.

Table 1-463. R643 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN	R/W	0xFF	DPLL Feedback Divider Denominator Value used with DPLL3 feedback configuration 2 ROM=Y, EEPROM=N

1.462 R644 (Offset = 0x284)

Return to the Summary Table.

Table 1-464. R644 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL3_REF5_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF5. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
4	DPLL3_REF4_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF4. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
3	DPLL3_REF3_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF3. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
2	DPLL3_REF2_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF2. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
1	DPLL3_REF1_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF1. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

Table 1-464. R644 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DPLL3_REF0_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF0. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

1.463 R645 (Offset = 0x285)

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Table 1-465. R645 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:3	RESERVED	R	0x0	Reserved
2:0	DPLL3_FB_MASH_ORDER	R/W	0x2	DPLL Feedback Divider MASH Order. ROM=Y, EEPROM=N 0x0 = Integer 0x1 = 1st order 0x2 = 2nd order 0x3 = 3rd order 0x4 = 4th order

1.464 R646 (Offset = 0x286)

Return to the Summary Table.

Table 1-466. R646 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_FB_FDEV_37:32	R/W	0x0	See Register 650

1.465 R647 (Offset = 0x287)

Return to the Summary Table.

Table 1-467. R647 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_FDEV_31:24	R/W	0x0	See Register 650

1.466 R648 (Offset = 0x288)

Return to the Summary Table.

Table 1-468. R648 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_FDEV_23:16	R/W	0x0	See Register 650

1.467 R649 (Offset = 0x289)

Return to the Summary Table.

Table 1-469. R649 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_FDEV_15:8	R/W	0x0	See Register 650

1.468 R650 (Offset = 0x28A)

Return to the Summary Table.

Table 1-470. R650 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_FDEV	R/W	0x0	DPLL Feedback Divider DCO Frequency Deviation Value ROM=Y, EEPROM=N

1.469 R651 (Offset = 0x28B)

Return to the Summary Table.

Table 1-471. R651 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL3_FB_FDEV_UPDATE	R/W	0x0	Increment/Decrement DPLL Feedback Numerator value with DPLL_FB_FDEV value ROM=Y, EEPROM=N

1.470 R652 (Offset = 0x28C)

Return to the Summary Table.

Table 1-472. R652 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL3_FB_FDEV_EN	R/W	0x0	Enable DPLL DCO mode ROM=Y, EEPROM=N

1.471 R653 (Offset = 0x28D)

Return to the Summary Table.

Table 1-473. R653 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT_39:32	R	0x14	See Register 657

1.472 R654 (Offset = 0x28E)

Return to the Summary Table.

Table 1-474. R654 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT_31:24	R	0x7A	See Register 657

1.473 R655 (Offset = 0x28F)

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Table 1-475. R655 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT_23:16	R	0xE1	See Register 657

1.474 R656 (Offset = 0x290)

Return to the Summary Table.

Table 1-476. R656 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT_15:8	R	0x47	See Register 657

1.475 R657 (Offset = 0x291)

Return to the Summary Table.

Table 1-477. R657 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT	R	0xAE	Readback DPLL Feedback Divider Numerator value as a result of DCO mode ROM=N, EEPROM=N

1.476 R658 (Offset = 0x292)

Return to the Summary Table.

Table 1-478. R658 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	DPLL3_REF0_DBLR_EN	R/W	0x0	DPLL Reference 0 Doubler Enable ROM=Y, EEPROM=N
2	DPLL3_REF1_DBLR_EN	R/W	0x0	DPLL Reference 1 Doubler Enable ROM=Y, EEPROM=N
1	DPLL3_REF2_DBLR_EN	R/W	0x0	DPLL Reference 2 Doubler Enable ROM=Y, EEPROM=N
0	DPLL3_REF3_DBLR_EN	R/W	0x1	DPLL Reference 3 Doubler Enable ROM=Y, EEPROM=N

1.477 R659 (Offset = 0x293)

Return to the Summary Table.

Table 1-479. R659 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF0_RDIV_15:8	R/W	0x0	See Register 660

1.478 R660 (Offset = 0x294)

Return to the Summary Table.

Table 1-480. R660 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF0_RDIV	R/W	0x7D	DPLL Reference 0 R divider value ROM=Y, EEPROM=N

1.479 R661 (Offset = 0x295)

Return to the Summary Table.

Table 1-481. R661 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF1_RDIV_15:8	R/W	0x0	See Register 662

1.480 R662 (Offset = 0x296)

Return to the Summary Table.

Table 1-482. R662 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF1_RDIV	R/W	0x8	DPLL Reference 1 R divider value ROM=Y, EEPROM=N

1.481 R663 (Offset = 0x297)

Return to the Summary Table.

Table 1-483. R663 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF2_RDIV_15:8	R/W	0x0	See Register 664

1.482 R664 (Offset = 0x298)

Return to the Summary Table.

Table 1-484. R664 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF2_RDIV	R/W	0x0	DPLL Reference 2 R divider value ROM=Y, EEPROM=N

1.483 R665 (Offset = 0x299)

Return to the Summary Table.

Table 1-485. R665 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF3_RDIV_15:8	R/W	0x0	See Register 666

1.484 R666 (Offset = 0x29A)

Return to the Summary Table.

Table 1-486. R666 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF3_RDIV	R/W	0x0	DPLL Reference 3 R divider value ROM=Y, EEPROM=N

1.485 R667 (Offset = 0x29B)

Return to the Summary Table.

Table 1-487. R667 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF4_RDIV_15:8	R/W	0x0	See Register 668

1.486 R668 (Offset = 0x29C)

Return to the Summary Table.

Table 1-488. R668 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF4_RDIV	R/W	0x0	DPLL Reference 4 R divider value ROM=Y, EEPROM=N

1.487 R669 (Offset = 0x29D)

Return to the Summary Table.

Table 1-489. R669 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF5_RDIV_15:8	R/W	0x1	See Register 670

1.488 R670 (Offset = 0x29E)

Return to the Summary Table.

Table 1-490. R670 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF5_RDIV	R/W	0x1	DPLL Reference 5 R divider value ROM=Y, EEPROM=N

1.489 R707 (Offset = 0x2C3)

Return to the Summary Table.

Table 1-491. R707 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_CP_PU_R	R/W	0x6D	PLL charge pump pull-up resistor selection ROM=Y, EEPROM=N 0x0 = Disabled 0x1 = 78 kΩ 0x2 = 39 kΩ 0x3 = 26 kΩ 0x4 = 20 kΩ 0x5 = 15.9 kΩ 0x6 = 13.2 kΩ 0x7 = 11.3 kΩ 0x8 = 9.8 kΩ 0x9 = 8.71 kΩ 0xA = 7.83 kΩ 0xB = 7.12 kΩ 0xC = 6.58 kΩ 0xD = 6.07 kΩ 0xE = 5.63 kΩ 0xF = 5.25 kΩ 0x10 = 4.9 kΩ 0x11 = 4.61 kΩ 0x12 = 4.35 kΩ 0x13 = 4.12 kΩ 0x14 = 3.94 kΩ 0x15 = 3.75 kΩ 0x16 = 3.57 kΩ 0x17 = 3.42 kΩ 0x18 = 3.27 kΩ 0x19 = 3.14 kΩ 0x1A = 3.01 kΩ 0x1B = 2.9 kΩ 0x1C = 2.81 kΩ 0x1D = 2.71 kΩ 0x1E = 2.62 kΩ 0x1F = 2.53 kΩ 0x20 = 2.4 kΩ 0x21 = 2.33 kΩ 0x22 = 2.26 kΩ 0x23 = 2.2 kΩ 0x24 = 2.14 kΩ 0x25 = 2.09 kΩ 0x26 = 2.03 kΩ 0x27 = 1.98 kΩ 0x28 = 1.93 kΩ 0x29 = 1.88 kΩ 0x2A = 1.84 kΩ 0x2B = 1.79 kΩ 0x2C = 1.76 kΩ 0x2D = 1.72 kΩ 0x2E = 1.68 kΩ

Table 1-491. R707 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 1.65 kΩ 0x30 = 1.61 kΩ 0x31 = 1.58 kΩ 0x32 = 1.55 kΩ 0x33 = 1.52 kΩ 0x34 = 1.49 kΩ 0x35 = 1.46 kΩ 0x36 = 1.44 kΩ 0x37 = 1.41 kΩ 0x38 = 1.38 kΩ 0x39 = 1.36 kΩ 0x3A = 1.34 kΩ 0x3B = 1.31 kΩ 0x3C = 1.29 kΩ 0x3D = 1.27 kΩ 0x3E = 1.25 kΩ 0x3F = 1.23 kΩ 0x40 = 1.2 kΩ 0x41 = 1.18 kΩ 0x42 = 1.16 kΩ 0x43 = 1.15 kΩ 0x44 = 1.13 kΩ 0x45 = 1.12 kΩ 0x46 = 1.1 kΩ 0x47 = 1.08 kΩ 0x48 = 1.07 kΩ 0x49 = 1.05 kΩ 0x4A = 1.04 kΩ 0x4B = 1.03 kΩ 0x4C = 1.01 kΩ 0x4D = 1 kΩ 0x4E = 0.989 kΩ 0x4F = 0.977 kΩ 0x50 = 0.964 kΩ 0x51 = 0.952 kΩ 0x52 = 0.941 kΩ 0x53 = 0.929 kΩ 0x54 = 0.92 kΩ 0x55 = 0.909 kΩ 0x56 = 0.898 kΩ 0x57 = 0.888 kΩ 0x58 = 0.878 kΩ 0x59 = 0.868 kΩ 0x5A = 0.858 kΩ 0x5B = 0.849 kΩ 0x5C = 0.841 kΩ 0x5D = 0.832 kΩ 0x5E = 0.823 kΩ 0x5F = 0.814 kΩ

Table 1-491. R707 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = 0.8 kΩ 0x61 = 0.792 kΩ 0x62 = 0.784 kΩ 0x63 = 0.776 kΩ 0x64 = 0.769 kΩ 0x65 = 0.762 kΩ 0x66 = 0.754 kΩ 0x67 = 0.747 kΩ 0x68 = 0.74 kΩ 0x69 = 0.733 kΩ 0x6A = 0.726 kΩ 0x6B = 0.719 kΩ 0x6C = 0.713 kΩ 0x6D = 0.707 kΩ 0x6E = 0.7 kΩ 0x6F = 0.694 kΩ 0x70 = 0.688 kΩ 0x71 = 0.682 kΩ 0x72 = 0.676 kΩ 0x73 = 0.67 kΩ 0x74 = 0.665 kΩ 0x75 = 0.659 kΩ 0x76 = 0.654 kΩ 0x77 = 0.648 kΩ 0x78 = 0.643 kΩ 0x79 = 0.637 kΩ 0x7A = 0.632 kΩ 0x7B = 0.627 kΩ 0x7C = 0.623 kΩ 0x7D = 0.618 kΩ 0x7E = 0.613 kΩ 0x7F = 0.608 kΩ 0x80 = 0.6 kΩ 0x81 = 0.595 kΩ 0x82 = 0.591 kΩ 0x83 = 0.586 kΩ 0x84 = 0.583 kΩ 0x85 = 0.578 kΩ 0x86 = 0.574 kΩ 0x87 = 0.57 kΩ 0x88 = 0.565 kΩ 0x89 = 0.561 kΩ 0x8A = 0.557 kΩ 0x8B = 0.553 kΩ 0x8C = 0.55 kΩ 0x8D = 0.546 kΩ 0x8E = 0.542 kΩ 0x8F = 0.538 kΩ 0x90 = 0.535 kΩ

Table 1-491. R707 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x91 = 0.531 kΩ 0x92 = 0.527 kΩ 0x93 = 0.524 kΩ 0x94 = 0.521 kΩ 0x95 = 0.517 kΩ 0x96 = 0.514 kΩ 0x97 = 0.51 kΩ 0x98 = 0.507 kΩ 0x99 = 0.504 kΩ 0x9A = 0.5 kΩ 0x9B = 0.497 kΩ 0x9C = 0.494 kΩ 0x9D = 0.491 kΩ 0x9E = 0.488 kΩ 0x9F = 0.485 kΩ 0xA0 = 0.48 kΩ 0xA1 = 0.477 kΩ 0xA2 = 0.474 kΩ 0xA3 = 0.471 kΩ 0xA4 = 0.469 kΩ 0xA5 = 0.466 kΩ 0xA6 = 0.463 kΩ 0xA7 = 0.46 kΩ 0xA8 = 0.458 kΩ 0xA9 = 0.455 kΩ 0xAA = 0.452 kΩ 0xAB = 0.45 kΩ 0xAC = 0.447 kΩ 0xAD = 0.445 kΩ 0xAE = 0.442 kΩ 0xAF = 0.44 kΩ 0xB0 = 0.437 kΩ 0xB1 = 0.435 kΩ 0xB2 = 0.432 kΩ 0xB3 = 0.43 kΩ 0xB4 = 0.428 kΩ 0xB5 = 0.425 kΩ 0xB6 = 0.423 kΩ 0xB7 = 0.421 kΩ 0xB8 = 0.419 kΩ 0xB9 = 0.416 kΩ 0xBA = 0.414 kΩ 0xBB = 0.412 kΩ 0xBC = 0.41 kΩ 0xBD = 0.408 kΩ 0xBE = 0.406 kΩ 0xBF = 0.404 kΩ 0xC0 = 0.4 kΩ 0xC1 = 0.398 kΩ

Table 1-491. R707 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xC2 = 0.396 kΩ 0xC3 = 0.394 kΩ 0xC4 = 0.392 kΩ 0xC5 = 0.39 kΩ 0xC6 = 0.388 kΩ 0xC7 = 0.386 kΩ 0xC8 = 0.384 kΩ 0xC9 = 0.382 kΩ 0xCA = 0.381 kΩ 0xCB = 0.379 kΩ 0xCC = 0.377 kΩ 0xCD = 0.375 kΩ 0xCE = 0.373 kΩ 0xCF = 0.372 kΩ 0xD0 = 0.37 kΩ 0xD1 = 0.368 kΩ 0xD2 = 0.366 kΩ 0xD3 = 0.365 kΩ 0xD4 = 0.363 kΩ 0xD5 = 0.361 kΩ 0xD6 = 0.36 kΩ 0xD7 = 0.358 kΩ 0xD8 = 0.356 kΩ 0xD9 = 0.355 kΩ 0xDA = 0.353 kΩ 0xDB = 0.352 kΩ 0xDC = 0.35 kΩ 0xDD = 0.349 kΩ 0xDE = 0.347 kΩ 0xDF = 0.345 kΩ 0xE0 = 0.343 kΩ 0xE1 = 0.341 kΩ 0xE2 = 0.34 kΩ 0xE3 = 0.338 kΩ 0xE4 = 0.337 kΩ 0xE5 = 0.336 kΩ 0xE6 = 0.334 kΩ 0xE7 = 0.333 kΩ 0xE8 = 0.331 kΩ 0xE9 = 0.33 kΩ 0xEA = 0.328 kΩ 0xEB = 0.327 kΩ 0xEC = 0.326 kΩ 0xED = 0.325 kΩ 0xEE = 0.323 kΩ 0xEF = 0.322 kΩ 0xF0 = 0.32 kΩ 0xF1 = 0.319 kΩ 0xF2 = 0.318 kΩ

Table 1-491. R707 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xF3 = 0.317 kΩ 0xF4 = 0.315 kΩ 0xF5 = 0.314 kΩ 0xF6 = 0.313 kΩ 0xF7 = 0.312 kΩ 0xF8 = 0.31 kΩ 0xF9 = 0.309 kΩ 0xFA = 0.308 kΩ 0xFB = 0.307 kΩ 0xFC = 0.306 kΩ 0xFD = 0.304 kΩ 0xFE = 0.303 kΩ 0xFF = 0.302 kΩ

1.490 R708 (Offset = 0x2C4)

Return to the Summary Table.

Table 1-492. R708 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	PLL1_CPG	R/W	0x3	PLL charge pump gain Pump up/down. ROM=Y, EEPROM=Y 0x0 = 1.6 mA 0x1 = 3.2 mA 0x2 = 4.8 mA 0x3 = 6.4 mA

1.491 R709 (Offset = 0x2C5)

Return to the Summary Table.

Table 1-493. R709 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-493. R709 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R2	R/W	0x9	PLL Loop Filter R2 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.262 kΩ 0x2 = 0.357 kΩ 0x3 = 0.166 kΩ 0x4 = 0.642 kΩ 0x5 = 0.199 kΩ 0x6 = 0.244 kΩ 0x7 = 0.142 kΩ 0x8 = 1.14 kΩ 0x9 = 0.222 kΩ 0xA = 0.283 kΩ 0xB = 0.152 kΩ 0xC = 0.425 kΩ 0xD = 0.177 kΩ 0xE = 0.21 kΩ 0xF = 0.132 kΩ 0x10 = 0.847 kΩ 0x11 = 1.06 kΩ 0x12 = 1.16 kΩ 0x13 = 0.966 kΩ 0x14 = 1.44 kΩ 0x15 = 0.998 kΩ 0x16 = 1.04 kΩ 0x17 = 0.941 kΩ 0x18 = 1.94 kΩ 0x19 = 1.02 kΩ 0x1A = 1.08 kΩ 0x1B = 0.951 kΩ 0x1C = 1.22 kΩ 0x1D = 0.976 kΩ 0x1E = 1.01 kΩ 0x1F = 0.931 kΩ 0x20 = 1.66 kΩ 0x21 = 1.88 kΩ 0x22 = 1.97 kΩ 0x23 = 1.78 kΩ 0x24 = 2.26 kΩ 0x25 = 1.81 kΩ 0x26 = 1.86 kΩ 0x27 = 1.76 kΩ 0x28 = 2.75 kΩ 0x29 = 1.84 kΩ 0x2A = 1.9 kΩ 0x2B = 1.77 kΩ 0x2C = 2.04 kΩ 0x2D = 1.79 kΩ 0x2E = 1.82 kΩ

Table 1-493. R709 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 1.75 kΩ 0x30 = 2.46 kΩ 0x31 = 2.68 kΩ 0x32 = 2.77 kΩ 0x33 = 2.58 kΩ 0x34 = 3.06 kΩ 0x35 = 2.61 kΩ 0x36 = 2.66 kΩ 0x37 = 2.56 kΩ 0x38 = 3.55 kΩ 0x39 = 2.64 kΩ 0x3A = 2.7 kΩ 0x3B = 2.57 kΩ 0x3C = 2.84 kΩ 0x3D = 2.59 kΩ 0x3E = 2.62 kΩ 0x3F = 2.55 kΩ

1.492 R710 (Offset = 0x2C6)

Return to the Summary Table.

Table 1-494. R710 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-494. R710 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R3	R/W	0x2	PLL Loop Filter R3 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ

Table 1-494. R710 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.493 R711 (Offset = 0x2C7)

Return to the Summary Table.

Table 1-495. R711 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-495. R711 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R4	R/W	0x2	PLL Loop Filter R4 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ

Table 1-495. R711 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.494 R712 (Offset = 0x2C8)

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Table 1-496. R712 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PLL1_DISABLE_3RD4TH	R/W	0x3	PLL Loop Filter Disconnects C3 and C4 ROM=Y, EEPROM=N 0x0 = C3/C4 Disconnected 0x1 = C3=Enabled, C4=Disconnected 0x2 = C3=Disconnected, C4=Enabled 0x3 = C3=Enabled, C4=Enabled
5:3	PLL1_LF_C3	R/W	0x7	PLL Loop Filter C3 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

Table 1-496. R712 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	PLL1_LF_C4	R/W	0x7	PLL Loop Filter C4 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

1.495 R713 (Offset = 0x2C9)

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Table 1-497. R713 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL1_RDIV_8:8	R/W	0x0	See Register 714

1.496 R714 (Offset = 0x2CA)

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Table 1-498. R714 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_RDIV	R/W	0x8	PLL R Divider ROM=Y, EEPROM=Y

1.497 R715 (Offset = 0x2CB)

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Table 1-499. R715 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL1_RDIV_XO_EN	R/W	0x0	APLL reference source is from XO. Must also enable XO to drive this APLL with XO_OUT_BUF_EN[1] = 1 ROM=Y, EEPROM=Y

Table 1-499. R715 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PLL1_RDIV_XO_DBLR_EN	R/W	0x0	Enables XO Doubler ROM=Y, EEPROM=Y
2	PLL1_RDIV_BYPASS_EN	R/W	0x0	Bypass R Divider ROM=Y, EEPROM=Y
1:0	PLL1_RDIV_MUX_SEL	R/W	0x2	Select R Divider input. When enabling reference from feedback divider, the APLL PLLx_VCO_BUF_2REF_EN bit must also be set appropriately. ROM=Y, EEPROM=Y 0x0 = XO 0x1 = VCO2 feedback divider 0x2 = VCO3 feedback divider

1.498 R716 (Offset = 0x2CC)

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Table 1-500. R716 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL1_NDIV_8:8	R/W	0x0	See Register 717

1.499 R717 (Offset = 0x2CD)

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Table 1-501. R717 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NDIV	R/W	0x28	PLL N Divider ROM=Y, EEPROM=Y

1.500 R718 (Offset = 0x2CE)

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Table 1-502. R718 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_MSB	R/W	0x58	When PLL1_MODE is set for 24 bit fractional. PLL1_NUM_MSB is effective PLL1_NUM[23:16]. Other PLL1_NUM and PLL1_DEN bits in programmable mode are in PLL1_NUM field. When in 40-bit fixed denominator PLL mode, then PLL1_NUM_MSB is unused. ROM=Y, EEPROM=Y

1.501 R719 (Offset = 0x2CF)

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Table 1-503. R719 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_39:32	R/W	0x56	See Register 723

1.502 R720 (Offset = 0x2D0)

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Table 1-504. R720 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_31:24	R/W	0x6	See Register 723

1.503 R721 (Offset = 0x2D1)

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Table 1-505. R721 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_23:16	R/W	0x80	See Register 723

1.504 R722 (Offset = 0x2D2)

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Table 1-506. R722 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_15:8	R/W	0x1	See Register 723

1.505 R723 (Offset = 0x2D3)

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Table 1-507. R723 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM	R/W	0x0	When PLL1_MODE = 1 (40-bit fixed denominator) mode then PLL1_NUM contains the APLL1 numerator. When PLL1_MODE = 0 (24-bit programmable denominator) then PLL1_NUM[23:0] stores the programmable PLL1 denominator and PLL1_NUM[39:24] stores the 16 LSBs of the PLL1 numerator. Total PLL1 numerator is calculated with PLL1_NUM_MSB as the 8 MSBs. In 24-bit programmable denominator mode PLL1_NUM[23:0] = 0 is 2^{24}. ROM=Y, EEPROM=Y

1.506 R724 (Offset = 0x2D4)

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Table 1-508. R724 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	PLL1_DTHRMODE	R/W	0x3	PLL MASH Dither Mode ROM=Y, EEPROM=N 0x0 = Constant Dither MACC2 0x1 = Constant Dither MACC2 and MACC3 0x2 = LFSR Dither MACC2 0x3 = Dither Disabled
3:1	PLL1_ORDER	R/W	0x3	PLL MASH Order ROM=Y, EEPROM=N 0x0 = Integer Mode Divider 0x1 = 1st 0x2 = 2nd 0x3 = 3rd
0	PLL1_MODE	R/W	0x0	In APLL 24-bit num/den mode, APLL denominator is programmable. Recommended not for use with DPLL mode. In 24-bit mode, the denominator is stored in PLL1_NUM[23:0] The numerator is stored in (PLL1_NUM_MSB << 16) + PLL1_NUM[39:24]. In APLL 40-bit mode, APLL denominator is fixed. For use with DPLL. ROM=Y, EEPROM=Y 0x0 = APLL 24-bit num/den 0x1 = APLL 40-bit num (Req for DPLL)

1.507 R725 (Offset = 0x2D5)

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Table 1-509. R725 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_39:32	R	0x0	See Register 729

1.508 R726 (Offset = 0x2D6)

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Table 1-510. R726 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_31:24	R	0x0	See Register 729

1.509 R727 (Offset = 0x2D7)

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Table 1-511. R727 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_23:16	R	0x0	See Register 729

1.510 R728 (Offset = 0x2D8)

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Table 1-512. R728 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_15:8	R	0x0	See Register 729

1.511 R729 (Offset = 0x2D9)

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Table 1-513. R729 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT	R	0x0	Readback current effective APLL1 Numerator after FDEV and/or DPLL correction ROM=N, EEPROM=N

1.512 R731 (Offset = 0x2DB)

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Table 1-514. R731 Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL1_PRI_DIV_SYNC_EN	R/W	0x1	PLL1 P1 Divider Sync Enable. Enables synchronization of PLL1 P1 post-divider. ROM=Y, EEPROM=N
6	PLL1_PRI_DIV_EN	R/W	0x1	Enables the VCO1 P1 divider ROM=Y, EEPROM=Y
5:3	PLL1_PRI_DIV	R/W	0x4	Sets the VCO post-divider VCO1 P1 from 2 to 7. ROM=Y, EEPROM=Y 0x0 = 2 (Reserved) 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7
2	PLL1_P1_DIV_OUT0_1_EN	R/W	0x0	Enables VCO1 P1 divider output driver to channel output bank OUT0_1 ROM=Y, EEPROM=Y
1	PLL1_P1_DIV_OUT2_3_EN	R/W	0x0	Enables VCO1 P1 divider output driver to channel output bank OUT2_3 ROM=Y, EEPROM=Y
0	PLL1_P1_DIV_OUT14_15_EN	R/W	0x0	Enables VCO1 P1 divider output driver to channel output bank OUT14_15 ROM=Y, EEPROM=Y

1.513 R732 (Offset = 0x2DC)

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Table 1-515. R732 Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL1_SEC_DIV_SYNC_EN	R/W	0x1	PLL1 P2 Divider Sync Enable. Enables synchronization of PLL1 P2 post-divider. ROM=Y, EEPROM=N
6	PLL1_SEC_DIV_EN	R/W	0x0	Enables the VCO1 P2 divider ROM=Y, EEPROM=Y
5:3	PLL1_SEC_DIV	R/W	0x4	Sets the VCO post-divider VCO1 P2 from 2 to 7. ROM=Y, EEPROM=Y 0x0 = 2 (Reserved) 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7

Table 1-515. R732 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PLL1_P2_DIV_OUT0_1_EN	R/W	0x0	Enables the VCO1 P2 divider output driver to channel output bank OUT0_1 ROM=Y, EEPROM=Y
1	RESERVED	R	0x0	Enables the VCO1 P2 divider output driver to channel output bank Reserved ROM=Y, EEPROM=Y
0	RESERVED	R	0x0	Enables the VCO1 P2 divider output driver to channel output bank Reserved ROM=Y, EEPROM=Y

1.514 R733 (Offset = 0x2DD)

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Table 1-516. R733 Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL1_VCO_BUF_EN	R/W	0x0	Enables the VCO1 Buffer which drives the DPLL feedback, reference window detector, DPLL reference for cascade mode, and test mode ROM=Y, EEPROM=N
6:5	PLL1_VCO_BUF_2REF_EN	R/W	0x0	Enables the APLL1 Div-by-4 cascade divider to APLL2/3 reference input for cascade mode. [0] - > APLL2, [1] -> APLL3 ROM=Y, EEPROM=Y
4	PLL1_VCO_BUF_2DPLL_EN	R/W	0x0	Enables the VCO1 Buffer output driver to DPLL feedback divider ROM=Y, EEPROM=N
3	RESERVED	R	0x0	Reserved
2	PLL1_VCO_BUF_PPM_CHECK_EN	R/W	0x0	Enables the APLL1 Div-by-4/8 cascade divider to DPLL/PPM frequency detector ROM=Y, EEPROM=N
1:0	PLL1_VCO_BUF_FB_TDC_EN	R/W	0x0	Enables APLL1 Div-by-8 cacade divider to TDC2 and TDC3 for cascade mode [0] = TDC2 driver enable [1] = TDC3 driver enable ROM=Y, EEPROM=N

1.515 R736 (Offset = 0x2E0)

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Table 1-517. R736 Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL1_NCLK_TEST_EN	R/W	0x0	Unused ROM=N, EEPROM=N
6:4	RESERVED	R	0x0	Reserved
3	PLL1_RDIV_OUTPUT_EN	R/W	0x0	If GPIOx_SEL selects PLL1 R/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N

Table 1-517. R736 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	R	0x0	Reserved

1.516 R741 (Offset = 0x2E5)

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Table 1-518. R741 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL1_VM_INSIDE	R	0x1	Denotes if the VCO tuning voltage is within operational range. ROM=N, EEPROM=N
4	PLL1_VM_HI	R	0x0	Denotes if the charge pump voltage is too high and outside range. If PLL1_VM_INSIDE = 0 and VM_HI = 0, then charge pump voltage is too low. ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.517 R745 (Offset = 0x2E9)

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Table 1-519. R745 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	PLL1_NDIV_OUTPUT_EN	R/W	0x0	If GPIOx_SEL selects PLL1 N/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.518 R746 (Offset = 0x2EA)

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Table 1-520. R746 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved

Table 1-520. R746 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PLL1_VCO_PREBUF_EN	R/W	0x1	Set to same value as APLL1_EN. ROM=Y, EEPROM=Y

1.519 R773 (Offset = 0x305)

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Table 1-521. R773 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	RESERVED	R	0x0	Reserved

1.520 R777 (Offset = 0x309)

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Table 1-522. R777 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_CP_PU_R	R/W	0x22	PLL charge pump pull-up resistor selection ROM=Y, EEPROM=N 0x0 = Disabled 0x1 = 78 kΩ 0x2 = 39 kΩ 0x3 = 26 kΩ 0x4 = 20 kΩ 0x5 = 15.9 kΩ 0x6 = 13.2 kΩ 0x7 = 11.3 kΩ 0x8 = 9.8 kΩ 0x9 = 8.71 kΩ 0xA = 7.83 kΩ 0xB = 7.12 kΩ 0xC = 6.58 kΩ 0xD = 6.07 kΩ 0xE = 5.63 kΩ 0xF = 5.25 kΩ 0x10 = 4.9 kΩ 0x11 = 4.61 kΩ 0x12 = 4.35 kΩ 0x13 = 4.12 kΩ 0x14 = 3.94 kΩ 0x15 = 3.75 kΩ 0x16 = 3.57 kΩ 0x17 = 3.42 kΩ 0x18 = 3.27 kΩ 0x19 = 3.14 kΩ 0x1A = 3.01 kΩ 0x1B = 2.9 kΩ 0x1C = 2.81 kΩ 0x1D = 2.71 kΩ 0x1E = 2.62 kΩ 0x1F = 2.53 kΩ 0x20 = 2.4 kΩ 0x21 = 2.33 kΩ 0x22 = 2.26 kΩ 0x23 = 2.2 kΩ 0x24 = 2.14 kΩ 0x25 = 2.09 kΩ 0x26 = 2.03 kΩ 0x27 = 1.98 kΩ 0x28 = 1.93 kΩ 0x29 = 1.88 kΩ 0x2A = 1.84 kΩ 0x2B = 1.79 kΩ 0x2C = 1.76 kΩ 0x2D = 1.72 kΩ 0x2E = 1.68 kΩ

Table 1-522. R777 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 1.65 kΩ 0x30 = 1.61 kΩ 0x31 = 1.58 kΩ 0x32 = 1.55 kΩ 0x33 = 1.52 kΩ 0x34 = 1.49 kΩ 0x35 = 1.46 kΩ 0x36 = 1.44 kΩ 0x37 = 1.41 kΩ 0x38 = 1.38 kΩ 0x39 = 1.36 kΩ 0x3A = 1.34 kΩ 0x3B = 1.31 kΩ 0x3C = 1.29 kΩ 0x3D = 1.27 kΩ 0x3E = 1.25 kΩ 0x3F = 1.23 kΩ 0x40 = 1.2 kΩ 0x41 = 1.18 kΩ 0x42 = 1.16 kΩ 0x43 = 1.15 kΩ 0x44 = 1.13 kΩ 0x45 = 1.12 kΩ 0x46 = 1.1 kΩ 0x47 = 1.08 kΩ 0x48 = 1.07 kΩ 0x49 = 1.05 kΩ 0x4A = 1.04 kΩ 0x4B = 1.03 kΩ 0x4C = 1.01 kΩ 0x4D = 1 kΩ 0x4E = 0.989 kΩ 0x4F = 0.977 kΩ 0x50 = 0.964 kΩ 0x51 = 0.952 kΩ 0x52 = 0.941 kΩ 0x53 = 0.929 kΩ 0x54 = 0.92 kΩ 0x55 = 0.909 kΩ 0x56 = 0.898 kΩ 0x57 = 0.888 kΩ 0x58 = 0.878 kΩ 0x59 = 0.868 kΩ 0x5A = 0.858 kΩ 0x5B = 0.849 kΩ 0x5C = 0.841 kΩ 0x5D = 0.832 kΩ 0x5E = 0.823 kΩ 0x5F = 0.814 kΩ

Table 1-522. R777 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = 0.8 kΩ 0x61 = 0.792 kΩ 0x62 = 0.784 kΩ 0x63 = 0.776 kΩ 0x64 = 0.769 kΩ 0x65 = 0.762 kΩ 0x66 = 0.754 kΩ 0x67 = 0.747 kΩ 0x68 = 0.74 kΩ 0x69 = 0.733 kΩ 0x6A = 0.726 kΩ 0x6B = 0.719 kΩ 0x6C = 0.713 kΩ 0x6D = 0.707 kΩ 0x6E = 0.7 kΩ 0x6F = 0.694 kΩ 0x70 = 0.688 kΩ 0x71 = 0.682 kΩ 0x72 = 0.676 kΩ 0x73 = 0.67 kΩ 0x74 = 0.665 kΩ 0x75 = 0.659 kΩ 0x76 = 0.654 kΩ 0x77 = 0.648 kΩ 0x78 = 0.643 kΩ 0x79 = 0.637 kΩ 0x7A = 0.632 kΩ 0x7B = 0.627 kΩ 0x7C = 0.623 kΩ 0x7D = 0.618 kΩ 0x7E = 0.613 kΩ 0x7F = 0.608 kΩ 0x80 = 0.6 kΩ 0x81 = 0.595 kΩ 0x82 = 0.591 kΩ 0x83 = 0.586 kΩ 0x84 = 0.583 kΩ 0x85 = 0.578 kΩ 0x86 = 0.574 kΩ 0x87 = 0.57 kΩ 0x88 = 0.565 kΩ 0x89 = 0.561 kΩ 0x8A = 0.557 kΩ 0x8B = 0.553 kΩ 0x8C = 0.55 kΩ 0x8D = 0.546 kΩ 0x8E = 0.542 kΩ 0x8F = 0.538 kΩ 0x90 = 0.535 kΩ

Table 1-522. R777 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x91 = 0.531 kΩ 0x92 = 0.527 kΩ 0x93 = 0.524 kΩ 0x94 = 0.521 kΩ 0x95 = 0.517 kΩ 0x96 = 0.514 kΩ 0x97 = 0.51 kΩ 0x98 = 0.507 kΩ 0x99 = 0.504 kΩ 0x9A = 0.5 kΩ 0x9B = 0.497 kΩ 0x9C = 0.494 kΩ 0x9D = 0.491 kΩ 0x9E = 0.488 kΩ 0x9F = 0.485 kΩ 0xA0 = 0.48 kΩ 0xA1 = 0.477 kΩ 0xA2 = 0.474 kΩ 0xA3 = 0.471 kΩ 0xA4 = 0.469 kΩ 0xA5 = 0.466 kΩ 0xA6 = 0.463 kΩ 0xA7 = 0.46 kΩ 0xA8 = 0.458 kΩ 0xA9 = 0.455 kΩ 0xAA = 0.452 kΩ 0xAB = 0.45 kΩ 0xAC = 0.447 kΩ 0xAD = 0.445 kΩ 0xAE = 0.442 kΩ 0xAF = 0.44 kΩ 0xB0 = 0.437 kΩ 0xB1 = 0.435 kΩ 0xB2 = 0.432 kΩ 0xB3 = 0.43 kΩ 0xB4 = 0.428 kΩ 0xB5 = 0.425 kΩ 0xB6 = 0.423 kΩ 0xB7 = 0.421 kΩ 0xB8 = 0.419 kΩ 0xB9 = 0.416 kΩ 0xBA = 0.414 kΩ 0xBB = 0.412 kΩ 0xBC = 0.41 kΩ 0xBD = 0.408 kΩ 0xBE = 0.406 kΩ 0xBF = 0.404 kΩ 0xC0 = 0.4 kΩ 0xC1 = 0.398 kΩ

Table 1-522. R777 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xC2 = 0.396 kΩ 0xC3 = 0.394 kΩ 0xC4 = 0.392 kΩ 0xC5 = 0.39 kΩ 0xC6 = 0.388 kΩ 0xC7 = 0.386 kΩ 0xC8 = 0.384 kΩ 0xC9 = 0.382 kΩ 0xCA = 0.381 kΩ 0xCB = 0.379 kΩ 0xCC = 0.377 kΩ 0xCD = 0.375 kΩ 0xCE = 0.373 kΩ 0xCF = 0.372 kΩ 0xD0 = 0.37 kΩ 0xD1 = 0.368 kΩ 0xD2 = 0.366 kΩ 0xD3 = 0.365 kΩ 0xD4 = 0.363 kΩ 0xD5 = 0.361 kΩ 0xD6 = 0.36 kΩ 0xD7 = 0.358 kΩ 0xD8 = 0.356 kΩ 0xD9 = 0.355 kΩ 0xDA = 0.353 kΩ 0xDB = 0.352 kΩ 0xDC = 0.35 kΩ 0xDD = 0.349 kΩ 0xDE = 0.347 kΩ 0xDF = 0.345 kΩ 0xE0 = 0.343 kΩ 0xE1 = 0.341 kΩ 0xE2 = 0.34 kΩ 0xE3 = 0.338 kΩ 0xE4 = 0.337 kΩ 0xE5 = 0.336 kΩ 0xE6 = 0.334 kΩ 0xE7 = 0.333 kΩ 0xE8 = 0.331 kΩ 0xE9 = 0.33 kΩ 0xEA = 0.328 kΩ 0xEB = 0.327 kΩ 0xEC = 0.326 kΩ 0xED = 0.325 kΩ 0xEE = 0.323 kΩ 0xEF = 0.322 kΩ 0xF0 = 0.32 kΩ 0xF1 = 0.319 kΩ 0xF2 = 0.318 kΩ

Table 1-522. R777 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xF3 = 0.317 kΩ 0xF4 = 0.315 kΩ 0xF5 = 0.314 kΩ 0xF6 = 0.313 kΩ 0xF7 = 0.312 kΩ 0xF8 = 0.31 kΩ 0xF9 = 0.309 kΩ 0xFA = 0.308 kΩ 0xFB = 0.307 kΩ 0xFC = 0.306 kΩ 0xFD = 0.304 kΩ 0xFE = 0.303 kΩ 0xFF = 0.302 kΩ

1.521 R778 (Offset = 0x30A)

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Table 1-523. R778 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL2_CP_PU_DIS	R/W	0x0	PLL charge pump - pump up disable ROM=Y, EEPROM=N
3:0	PLL2_CPG	R/W	0x9	PLL charge pump gain ROM=Y, EEPROM=Y 0x0 = 0 mA 0x1 = 0.4 mA 0x2 = 0.8 mA 0x3 = 1.2 mA 0x4 = 1.6 mA 0x5 = 2.0 mA 0x6 = 2.4 mA 0x7 = 2.8 mA 0x8 = 3.0 mA 0x9 = 3.4 mA 0xA = 3.8 mA 0xB = 4.2 mA 0xC = 4.6 mA 0xD = 5.0 mA 0xE = 5.4 mA 0xF = 5.8 mA

1.522 R779 (Offset = 0x30B)

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Table 1-524. R779 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_LF_R2	R/W	0x7	PLL Loop Filter R2 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.301 kΩ 0x2 = 0.551 kΩ 0x3 = 0.209 kΩ 0x4 = 1.05 kΩ 0x5 = 0.244 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 2.05 kΩ 0x9 = 0.269 kΩ 0xA = 0.444 kΩ 0xB = 0.194 kΩ 0xC = 0.709 kΩ 0xD = 0.224 kΩ 0xE = 0.0446 kΩ 0xF = 0.0421 kΩ 0x10 = 0.932 kΩ 0x11 = 1.18 kΩ 0x12 = 1.43 kΩ 0x13 = 1.09 kΩ 0x14 = 1.93 kΩ 0x15 = 1.13 kΩ 0x16 = 1.26 kΩ 0x17 = 1.07 kΩ 0x18 = 2.93 kΩ 0x19 = 1.15 kΩ 0x1A = 1.33 kΩ 0x1B = 1.08 kΩ 0x1C = 1.59 kΩ 0x1D = 1.11 kΩ 0x1E = 0.929 kΩ 0x1F = 0.926 kΩ 0x20 = 1.83 kΩ 0x21 = 2.08 kΩ 0x22 = 2.33 kΩ 0x23 = 1.99 kΩ 0x24 = 2.83 kΩ 0x25 = 2.03 kΩ 0x26 = 2.16 kΩ 0x27 = 1.97 kΩ 0x28 = 3.83 kΩ 0x29 = 2.05 kΩ 0x2A = 2.23 kΩ 0x2B = 1.98 kΩ 0x2C = 2.49 kΩ 0x2D = 2.01 kΩ 0x2E = 1.83 kΩ

Table 1-524. R779 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 1.83 kΩ 0x30 = 2.72 kΩ 0x31 = 2.97 kΩ 0x32 = 3.22 kΩ 0x33 = 2.88 kΩ 0x34 = 3.72 kΩ 0x35 = 2.91 kΩ 0x36 = 3.04 kΩ 0x37 = 2.85 kΩ 0x38 = 4.72 kΩ 0x39 = 2.94 kΩ 0x3A = 3.11 kΩ 0x3B = 2.86 kΩ 0x3C = 3.38 kΩ 0x3D = 2.89 kΩ 0x3E = 2.71 kΩ 0x3F = 2.71 kΩ

1.523 R780 (Offset = 0x30C)

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Table 1-525. R780 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-525. R780 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL2_LF_R3	R/W	0x2	PLL Loop Filter R3 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ

Table 1-525. R780 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.524 R781 (Offset = 0x30D)

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Table 1-526. R781 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-526. R781 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL2_LF_R4	R/W	0x2	PLL Loop Filter R4 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ

Table 1-526. R781 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.525 R782 (Offset = 0x30E)

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Table 1-527. R782 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PLL2_DISABLE_3RD4TH	R/W	0x3	PLL Loop Filter Disconnects C3 and C4 ROM=Y, EEPROM=N 0x0 = C3/C4 Disconnected 0x1 = C3=Enabled, C4=Disconnected 0x2 = C3=Disconnected, C4=Enabled 0x3 = C3=Enabled, C4=Enabled
5:3	PLL2_LF_C3	R/W	0x7	PLL Loop Filter C3 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

Table 1-527. R782 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	PLL2_LF_C4	R/W	0x7	PLL Loop Filter C4 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

1.526 R783 (Offset = 0x30F)

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Table 1-528. R783 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL2_RDIV_8:8	R/W	0x0	See Register 784

1.527 R784 (Offset = 0x310)

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Table 1-529. R784 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_RDIV	R/W	0x8	PLL R Divider ROM=Y, EEPROM=Y

1.528 R785 (Offset = 0x311)

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Table 1-530. R785 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL2_RDIV_XO_EN	R/W	0x0	APLL reference source is from XO. Must also enable XO to drive this APLL with XO_OUT_BUF_EN[2] = 1 ROM=Y, EEPROM=Y

Table 1-530. R785 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PLL2_RDIV_XO_DBLR_EN	R/W	0x0	Enables XO Doubler ROM=Y, EEPROM=Y
2	PLL2_RDIV_BYPASS_EN	R/W	0x0	Bypass R Divider ROM=Y, EEPROM=Y
1:0	PLL2_RDIV_MUX_SEL	R/W	0x2	Select R Divider input: 0=XO, 1=VCO1 feedback divider, 2=VCO3 feedback divider ROM=Y, EEPROM=Y 0x0 = XO 0x1 = VCO1 feedback divider 0x2 = VCO3 feedback divider

1.529 R786 (Offset = 0x312)

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Table 1-531. R786 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL2_NDIV_8:8	R/W	0x0	See Register 787

1.530 R787 (Offset = 0x313)

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Table 1-532. R787 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NDIV	R/W	0x2D	PLL N Divider ROM=Y, EEPROM=Y

1.531 R788 (Offset = 0x314)

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Table 1-533. R788 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_MSB	R/W	0x63	When PLL2_MODE is set for 24 bit fractional. PLL2_NUM_MSB is effective PLL2_NUM[23:16]. Other PLL2_NUM and PLL2_DEN bits in programmable mode are in PLL2_NUM field. When in 40-bit fixed denominator PLL mode, then PLL2_NUM_MSB is unused. ROM=Y, EEPROM=Y

1.532 R789 (Offset = 0x315)

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Table 1-534. R789 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_39:32	R/W	0x60	See Register 793

1.533 R790 (Offset = 0x316)

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Table 1-535. R790 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_31:24	R/W	0x0	See Register 793

1.534 R791 (Offset = 0x317)

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Table 1-536. R791 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_23:16	R/W	0x80	See Register 793

1.535 R792 (Offset = 0x318)

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Table 1-537. R792 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_15:8	R/W	0x0	See Register 793

1.536 R793 (Offset = 0x319)

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Table 1-538. R793 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM	R/W	0x0	When PLL2_MODE = 1 (40-bit fixed denominator) mode then PLL2_NUM contains the APLL2 numerator. When PLL2_MODE = 0 (24-bit programmable denominator) then PLL2_NUM[23:0] stores the programmable PLL2 denominator and PLL2_NUM[39:24] stores the 16 LSBs of the PLL2 numerator. Total PLL2 numerator is calculated with PLL2_NUM_MSB as the 8 MSBs. In 24-bit programmable denominator mode PLL2_NUM[23:0] = 0 is 2^{24}. ROM=Y, EEPROM=Y

1.537 R794 (Offset = 0x31A)

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Table 1-539. R794 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	PLL2_DTHRMODE	R/W	0x0	PLL MASH Dither Mode ROM=Y, EEPROM=N 0x0 = Constant Dither MACC2 0x1 = Constant Dither MACC2 and MACC3 0x2 = LFSR Dither MACC2 0x3 = Dither Disabled
3:1	PLL2_ORDER	R/W	0x3	PLL MASH Order ROM=Y, EEPROM=N 0x0 = Integer Mode Divider 0x1 = 1st 0x2 = 2nd 0x3 = 3rd
0	PLL2_MODE	R/W	0x0	In APLL 24-bit num/den mode, APLL denominator is programmable. Not for use with DPLL mode. In 24-bit mode, the denominator is stored in PLL2_NUM[23:0] The numerator is stored in (PLL2_NUM_MSB << 16) + PLL2_NUM[39:24]. In APLL 40-bit mode, APLL denominator is fixed. For use with DPLL. ROM=Y, EEPROM=Y 0x0 = APLL 24-bit num/den 0x1 = APLL 40-bit num (Req for DPLL)

1.538 R795 (Offset = 0x31B)

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Table 1-540. R795 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT_39:32	R	0x40	See Register 799

1.539 R796 (Offset = 0x31C)

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Table 1-541. R796 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT_31:24	R	0x0	See Register 799

1.540 R797 (Offset = 0x31D)

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Table 1-542. R797 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT_23:16	R	0x80	See Register 799

1.541 R798 (Offset = 0x31E)

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Table 1-543. R798 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT_15:8	R	0x0	See Register 799

1.542 R799 (Offset = 0x31F)

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Table 1-544. R799 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT	R	0x0	Readback current effective APLL2 Numerator after FDEV and/or DPLL correction ROM=N, EEPROM=N

1.543 R803 (Offset = 0x323)

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Table 1-545. R803 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved

Table 1-545. R803 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PLL2_VCO_BUF_EN	R/W	0x0	Enables the VCO2 Buffer which drives the DPLL feedback, reference window detector, DPLL reference for cascade mode, and test mode ROM=Y, EEPROM=N
3:2	PLL2_VCO_BUF_2REF_EN	R/W	0x0	Enables the APLL2 Div-by-4 cascade divider to [0] -> APLL1 and [1] -> APLL3 reference input for cascade mode. ROM=Y, EEPROM=Y
1	PLL2_VCO_BUF_2DPLL_EN	R/W	0x0	Enables the VCO2 Buffer output driver to DPLL2 feedback divider ROM=Y, EEPROM=N
0	PLL2_VCO_BUF_2WNDDET_EN	R/W	0x0	Enables the APLL2 Div-by-5 cascade divider to reference window detectors input buffer and prepares pre-divided clock for DPLL2 loop filter and PPM/Frequency detector. ROM=Y, EEPROM=N

1.544 R804 (Offset = 0x324)

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Table 1-546. R804 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL2_VCO_DIV_SYNC_EN	R/W	0x1	PLL2 Divider Sync Enable. Enables synchronization of post-dividers and reference dividers for PLL2. ROM=Y, EEPROM=N
4	PLL2_VCO_DIV_EN	R/W	0x1	Enables the VCO2 Div By 2 to 13 divide block. ROM=Y, EEPROM=Y
3:0	PLL2_VCO_DIV	R/W	0x9	Sets the VCO2 divider divide value from 2 to 13 ROM=Y, EEPROM=Y 0x0 = 2 (Reserved) 0x1 = 2 (Reserved) 0x2 = 2 0x3 = 3 0x4 = 4 0x5 = 5 0x6 = 6 0x7 = 7 0x8 = 8 0x9 = 9 0xA = 10 0xB = 11 0xC = 12 0xD = 13

1.545 R805 (Offset = 0x325)

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Table 1-547. R805 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	PLL2_VCO_BUF_FB_TDC_EN	R/W	0x0	Enables APLL2 Div-by-10 cascade divider to TDC1 and TDC3 for cascade mode [0] = TDC1 driver enable [1] = TDC3 driver enable ROM=Y, EEPROM=N
4	PLL2_P1_OUT14_15_EN	R/W	0x0	Enable VCO2 P1 divider output driver to channel output bank OUT14_15 ROM=Y, EEPROM=Y
3	PLL2_P1_OUT8_13_EN	R/W	0x0	Enable VCO2 P1 divider output driver to channel output bank OUT8_13 ROM=Y, EEPROM=Y
2	PLL2_P1_OUT4_7_EN	R/W	0x0	Enable VCO2 P1 divider output driver to channel output bank OUT4_7 ROM=Y, EEPROM=Y
1	PLL2_P1_OUT2_3_EN	R/W	0x0	Enable VCO2 P1 divider output driver to channel output bank OUT2_3 ROM=Y, EEPROM=Y
0	PLL2_P1_OUT0_1_EN	R/W	0x0	Enable VCO2 P1 divider output driver to channel output bank OUT0_1 ROM=Y, EEPROM=Y

1.546 R808 (Offset = 0x328)

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Table 1-548. R808 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	PLL2_RDIV_OUTPUT_EN	R/W	0x0	If GPIOx_SEL selects PLL2 R/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.547 R813 (Offset = 0x32D)

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Table 1-549. R813 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL2_VM_INSIDE	R	0x1	Denotes if the VCO tuning voltage is within operational range. ROM=N, EEPROM=N

Table 1-549. R813 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PLL2_VM_HI	R	0x0	Denotes if the charge pump voltage is too high and outside range. If PLL2_VM_INSIDE = 0 and VM_HI = 0, then charge pump voltage is too low. ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.548 R818 (Offset = 0x332)

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Table 1-550. R818 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	PLL2_NDIV_OUTPUT_EN	R/W	0x0	If GPIOx_SEL selects PLL2 N/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.549 R819 (Offset = 0x333)

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Table 1-551. R819 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL2_VCO_PREBUF_EN	R/W	0x1	Set to same value as APLL2_EN. ROM=Y, EEPROM=Y

1.550 R840 (Offset = 0x348)

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Table 1-552. R840 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_CPBAW_BLEED	R/W	0x22	PLL charge pump pull-up resistor selection ROM=Y, EEPROM=N 0x0 = Disabled 0x1 = 78 kΩ 0x2 = 39 kΩ 0x3 = 26 kΩ 0x4 = 20 kΩ 0x5 = 15.9 kΩ 0x6 = 13.2 kΩ 0x7 = 11.3 kΩ 0x8 = 9.8 kΩ 0x9 = 8.71 kΩ 0xA = 7.83 kΩ 0xB = 7.12 kΩ 0xC = 6.58 kΩ 0xD = 6.07 kΩ 0xE = 5.63 kΩ 0xF = 5.25 kΩ 0x10 = 4.9 kΩ 0x11 = 4.61 kΩ 0x12 = 4.35 kΩ 0x13 = 4.12 kΩ 0x14 = 3.94 kΩ 0x15 = 3.75 kΩ 0x16 = 3.57 kΩ 0x17 = 3.42 kΩ 0x18 = 3.27 kΩ 0x19 = 3.14 kΩ 0x1A = 3.01 kΩ 0x1B = 2.9 kΩ 0x1C = 2.81 kΩ 0x1D = 2.71 kΩ 0x1E = 2.62 kΩ 0x1F = 2.53 kΩ 0x20 = 2.4 kΩ 0x21 = 2.33 kΩ 0x22 = 2.26 kΩ 0x23 = 2.2 kΩ 0x24 = 2.14 kΩ 0x25 = 2.09 kΩ 0x26 = 2.03 kΩ 0x27 = 1.98 kΩ 0x28 = 1.93 kΩ 0x29 = 1.88 kΩ 0x2A = 1.84 kΩ 0x2B = 1.79 kΩ 0x2C = 1.76 kΩ 0x2D = 1.72 kΩ 0x2E = 1.68 kΩ

Table 1-552. R840 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 1.65 kΩ 0x30 = 1.61 kΩ 0x31 = 1.58 kΩ 0x32 = 1.55 kΩ 0x33 = 1.52 kΩ 0x34 = 1.49 kΩ 0x35 = 1.46 kΩ 0x36 = 1.44 kΩ 0x37 = 1.41 kΩ 0x38 = 1.38 kΩ 0x39 = 1.36 kΩ 0x3A = 1.34 kΩ 0x3B = 1.31 kΩ 0x3C = 1.29 kΩ 0x3D = 1.27 kΩ 0x3E = 1.25 kΩ 0x3F = 1.23 kΩ 0x40 = 1.2 kΩ 0x41 = 1.18 kΩ 0x42 = 1.16 kΩ 0x43 = 1.15 kΩ 0x44 = 1.13 kΩ 0x45 = 1.12 kΩ 0x46 = 1.1 kΩ 0x47 = 1.08 kΩ 0x48 = 1.07 kΩ 0x49 = 1.05 kΩ 0x4A = 1.04 kΩ 0x4B = 1.03 kΩ 0x4C = 1.01 kΩ 0x4D = 1 kΩ 0x4E = 0.989 kΩ 0x4F = 0.977 kΩ 0x50 = 0.964 kΩ 0x51 = 0.952 kΩ 0x52 = 0.941 kΩ 0x53 = 0.929 kΩ 0x54 = 0.92 kΩ 0x55 = 0.909 kΩ 0x56 = 0.898 kΩ 0x57 = 0.888 kΩ 0x58 = 0.878 kΩ 0x59 = 0.868 kΩ 0x5A = 0.858 kΩ 0x5B = 0.849 kΩ 0x5C = 0.841 kΩ 0x5D = 0.832 kΩ 0x5E = 0.823 kΩ 0x5F = 0.814 kΩ

Table 1-552. R840 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x60 = 0.8 kΩ 0x61 = 0.792 kΩ 0x62 = 0.784 kΩ 0x63 = 0.776 kΩ 0x64 = 0.769 kΩ 0x65 = 0.762 kΩ 0x66 = 0.754 kΩ 0x67 = 0.747 kΩ 0x68 = 0.74 kΩ 0x69 = 0.733 kΩ 0x6A = 0.726 kΩ 0x6B = 0.719 kΩ 0x6C = 0.713 kΩ 0x6D = 0.707 kΩ 0x6E = 0.7 kΩ 0x6F = 0.694 kΩ 0x70 = 0.688 kΩ 0x71 = 0.682 kΩ 0x72 = 0.676 kΩ 0x73 = 0.67 kΩ 0x74 = 0.665 kΩ 0x75 = 0.659 kΩ 0x76 = 0.654 kΩ 0x77 = 0.648 kΩ 0x78 = 0.643 kΩ 0x79 = 0.637 kΩ 0x7A = 0.632 kΩ 0x7B = 0.627 kΩ 0x7C = 0.623 kΩ 0x7D = 0.618 kΩ 0x7E = 0.613 kΩ 0x7F = 0.608 kΩ 0x80 = 0.6 kΩ 0x81 = 0.595 kΩ 0x82 = 0.591 kΩ 0x83 = 0.586 kΩ 0x84 = 0.583 kΩ 0x85 = 0.578 kΩ 0x86 = 0.574 kΩ 0x87 = 0.57 kΩ 0x88 = 0.565 kΩ 0x89 = 0.561 kΩ 0x8A = 0.557 kΩ 0x8B = 0.553 kΩ 0x8C = 0.55 kΩ 0x8D = 0.546 kΩ 0x8E = 0.542 kΩ 0x8F = 0.538 kΩ 0x90 = 0.535 kΩ

Table 1-552. R840 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x91 = 0.531 kΩ 0x92 = 0.527 kΩ 0x93 = 0.524 kΩ 0x94 = 0.521 kΩ 0x95 = 0.517 kΩ 0x96 = 0.514 kΩ 0x97 = 0.51 kΩ 0x98 = 0.507 kΩ 0x99 = 0.504 kΩ 0x9A = 0.5 kΩ 0x9B = 0.497 kΩ 0x9C = 0.494 kΩ 0x9D = 0.491 kΩ 0x9E = 0.488 kΩ 0x9F = 0.485 kΩ 0xA0 = 0.48 kΩ 0xA1 = 0.477 kΩ 0xA2 = 0.474 kΩ 0xA3 = 0.471 kΩ 0xA4 = 0.469 kΩ 0xA5 = 0.466 kΩ 0xA6 = 0.463 kΩ 0xA7 = 0.46 kΩ 0xA8 = 0.458 kΩ 0xA9 = 0.455 kΩ 0xAA = 0.452 kΩ 0xAB = 0.45 kΩ 0xAC = 0.447 kΩ 0xAD = 0.445 kΩ 0xAE = 0.442 kΩ 0xAF = 0.44 kΩ 0xB0 = 0.437 kΩ 0xB1 = 0.435 kΩ 0xB2 = 0.432 kΩ 0xB3 = 0.43 kΩ 0xB4 = 0.428 kΩ 0xB5 = 0.425 kΩ 0xB6 = 0.423 kΩ 0xB7 = 0.421 kΩ 0xB8 = 0.419 kΩ 0xB9 = 0.416 kΩ 0xBA = 0.414 kΩ 0xBB = 0.412 kΩ 0xBC = 0.41 kΩ 0xBD = 0.408 kΩ 0xBE = 0.406 kΩ 0xBF = 0.404 kΩ 0xC0 = 0.4 kΩ 0xC1 = 0.398 kΩ

Table 1-552. R840 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xC2 = 0.396 kΩ 0xC3 = 0.394 kΩ 0xC4 = 0.392 kΩ 0xC5 = 0.39 kΩ 0xC6 = 0.388 kΩ 0xC7 = 0.386 kΩ 0xC8 = 0.384 kΩ 0xC9 = 0.382 kΩ 0xCA = 0.381 kΩ 0xCB = 0.379 kΩ 0xCC = 0.377 kΩ 0xCD = 0.375 kΩ 0xCE = 0.373 kΩ 0xCF = 0.372 kΩ 0xD0 = 0.37 kΩ 0xD1 = 0.368 kΩ 0xD2 = 0.366 kΩ 0xD3 = 0.365 kΩ 0xD4 = 0.363 kΩ 0xD5 = 0.361 kΩ 0xD6 = 0.36 kΩ 0xD7 = 0.358 kΩ 0xD8 = 0.356 kΩ 0xD9 = 0.355 kΩ 0xDA = 0.353 kΩ 0xDB = 0.352 kΩ 0xDC = 0.35 kΩ 0xDD = 0.349 kΩ 0xDE = 0.347 kΩ 0xDF = 0.345 kΩ 0xE0 = 0.343 kΩ 0xE1 = 0.341 kΩ 0xE2 = 0.34 kΩ 0xE3 = 0.338 kΩ 0xE4 = 0.337 kΩ 0xE5 = 0.336 kΩ 0xE6 = 0.334 kΩ 0xE7 = 0.333 kΩ 0xE8 = 0.331 kΩ 0xE9 = 0.33 kΩ 0xEA = 0.328 kΩ 0xEB = 0.327 kΩ 0xEC = 0.326 kΩ 0xED = 0.325 kΩ 0xEE = 0.323 kΩ 0xEF = 0.322 kΩ 0xF0 = 0.32 kΩ 0xF1 = 0.319 kΩ 0xF2 = 0.318 kΩ

Table 1-552. R840 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xF3 = 0.317 kΩ 0xF4 = 0.315 kΩ 0xF5 = 0.314 kΩ 0xF6 = 0.313 kΩ 0xF7 = 0.312 kΩ 0xF8 = 0.31 kΩ 0xF9 = 0.309 kΩ 0xFA = 0.308 kΩ 0xFB = 0.307 kΩ 0xFC = 0.306 kΩ 0xFD = 0.304 kΩ 0xFE = 0.303 kΩ 0xFF = 0.302 kΩ

1.551 R841 (Offset = 0x349)

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Table 1-553. R841 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL3_CP_PU_DIS	R/W	0x1	PLL charge pump pump-up disable ROM=Y, EEPROM=N
3:0	PLL3_CPG	R/W	0x5	PLL charge pump gain ROM=Y, EEPROM=N 0x0 = 0 mA 0x1 = 0.4 mA 0x2 = 0.8 mA 0x3 = 1.2 mA 0x4 = 1.6 mA 0x5 = 2.0 mA 0x6 = 2.4 mA 0x7 = 2.8 mA 0x8 = 3.0 mA 0x9 = 3.4 mA 0xA = 3.8 mA 0xB = 4.2 mA 0xC = 4.6 mA 0xD = 5.0 mA 0xE = 5.4 mA 0xF = 5.8 mA

1.552 R842 (Offset = 0x34A)

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Table 1-554. R842 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-554. R842 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL3_LF_R2	R/W	0x1	PLL Loop Filter R2 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.301 kΩ 0x2 = 0.551 kΩ 0x3 = 0.209 kΩ 0x4 = 1.05 kΩ 0x5 = 0.244 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 2.05 kΩ 0x9 = 0.269 kΩ 0xA = 0.444 kΩ 0xB = 0.194 kΩ 0xC = 0.709 kΩ 0xD = 0.224 kΩ 0xE = 0.0446 kΩ 0xF = 0.0421 kΩ 0x10 = 0.932 kΩ 0x11 = 1.18 kΩ 0x12 = 1.43 kΩ 0x13 = 1.09 kΩ 0x14 = 1.93 kΩ 0x15 = 1.13 kΩ 0x16 = 1.26 kΩ 0x17 = 1.07 kΩ 0x18 = 2.93 kΩ 0x19 = 1.15 kΩ 0x1A = 1.33 kΩ 0x1B = 1.08 kΩ 0x1C = 1.59 kΩ 0x1D = 1.11 kΩ 0x1E = 0.929 kΩ 0x1F = 0.926 kΩ 0x20 = 1.83 kΩ 0x21 = 2.08 kΩ 0x22 = 2.33 kΩ 0x23 = 1.99 kΩ 0x24 = 2.83 kΩ 0x25 = 2.03 kΩ 0x26 = 2.16 kΩ 0x27 = 1.97 kΩ 0x28 = 3.83 kΩ 0x29 = 2.05 kΩ 0x2A = 2.23 kΩ 0x2B = 1.98 kΩ 0x2C = 2.49 kΩ 0x2D = 2.01 kΩ 0x2E = 1.83 kΩ

Table 1-554. R842 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 1.83 kΩ 0x30 = 2.72 kΩ 0x31 = 2.97 kΩ 0x32 = 3.22 kΩ 0x33 = 2.88 kΩ 0x34 = 3.72 kΩ 0x35 = 2.91 kΩ 0x36 = 3.04 kΩ 0x37 = 2.85 kΩ 0x38 = 4.72 kΩ 0x39 = 2.94 kΩ 0x3A = 3.11 kΩ 0x3B = 2.86 kΩ 0x3C = 3.38 kΩ 0x3D = 2.89 kΩ 0x3E = 2.71 kΩ 0x3F = 2.71 kΩ

1.553 R843 (Offset = 0x34B)

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Table 1-555. R843 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-555. R843 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL3_LF_R3	R/W	0xD	PLL Loop Filter R3 setting ROM=Y, EEPROM=N 0x0 = 0.0139 kΩ 0x1 = 0.51 kΩ 0x2 = 0.826 kΩ 0x3 = 1.23 kΩ 0x4 = 1.85 kΩ 0x5 = 2.26 kΩ 0x6 = 2.57 kΩ 0x7 = 2.97 kΩ 0x8 = 3.3 kΩ 0x9 = 3.75 kΩ 0xA = 4.07 kΩ 0xB = 4.47 kΩ 0xC = 5.09 kΩ 0xD = 5.5 kΩ 0xE = 5.81 kΩ 0xF = 6.22 kΩ 0x10 = 6.57 kΩ 0x11 = 7.01 kΩ 0x12 = 7.33 kΩ 0x13 = 7.73 kΩ 0x14 = 8.36 kΩ 0x15 = 8.76 kΩ 0x16 = 9.08 kΩ 0x17 = 9.48 kΩ 0x18 = 9.81 kΩ 0x19 = 10.3 kΩ 0x1A = 10.6 kΩ 0x1B = 11 kΩ 0x1C = 11.6 kΩ 0x1D = 12 kΩ 0x1E = 12.3 kΩ 0x1F = 12.7 kΩ 0x20 = 13 kΩ 0x21 = 13.5 kΩ 0x22 = 13.8 kΩ 0x23 = 14.2 kΩ 0x24 = 14.8 kΩ 0x25 = 15.2 kΩ 0x26 = 15.6 kΩ 0x27 = 16 kΩ 0x28 = 16.3 kΩ 0x29 = 16.7 kΩ 0x2A = 17.1 kΩ 0x2B = 17.5 kΩ 0x2C = 18.1 kΩ 0x2D = 18.5 kΩ 0x2E = 18.8 kΩ

Table 1-555. R843 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 19.2 kΩ 0x30 = 19.6 kΩ 0x31 = 20 kΩ 0x32 = 20.3 kΩ 0x33 = 20.7 kΩ 0x34 = 21.3 kΩ 0x35 = 21.7 kΩ 0x36 = 22.1 kΩ 0x37 = 22.5 kΩ 0x38 = 22.8 kΩ 0x39 = 23.2 kΩ 0x3A = 23.6 kΩ 0x3B = 24 kΩ 0x3C = 24.6 kΩ 0x3D = 25 kΩ 0x3E = 25.3 kΩ 0x3F = 25.7 kΩ

1.554 R844 (Offset = 0x34C)

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Table 1-556. R844 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-556. R844 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL3_LF_R4	R/W	0xD	PLL Loop Filter R4 setting ROM=Y, EEPROM=N 0x0 = 0.0139 kΩ 0x1 = 0.51 kΩ 0x2 = 0.826 kΩ 0x3 = 1.23 kΩ 0x4 = 1.85 kΩ 0x5 = 2.26 kΩ 0x6 = 2.57 kΩ 0x7 = 2.97 kΩ 0x8 = 3.3 kΩ 0x9 = 3.75 kΩ 0xA = 4.07 kΩ 0xB = 4.47 kΩ 0xC = 5.09 kΩ 0xD = 5.5 kΩ 0xE = 5.81 kΩ 0xF = 6.22 kΩ 0x10 = 6.57 kΩ 0x11 = 7.01 kΩ 0x12 = 7.33 kΩ 0x13 = 7.73 kΩ 0x14 = 8.36 kΩ 0x15 = 8.76 kΩ 0x16 = 9.08 kΩ 0x17 = 9.48 kΩ 0x18 = 9.81 kΩ 0x19 = 10.3 kΩ 0x1A = 10.6 kΩ 0x1B = 11 kΩ 0x1C = 11.6 kΩ 0x1D = 12 kΩ 0x1E = 12.3 kΩ 0x1F = 12.7 kΩ 0x20 = 13 kΩ 0x21 = 13.5 kΩ 0x22 = 13.8 kΩ 0x23 = 14.2 kΩ 0x24 = 14.8 kΩ 0x25 = 15.2 kΩ 0x26 = 15.6 kΩ 0x27 = 16 kΩ 0x28 = 16.3 kΩ 0x29 = 16.7 kΩ 0x2A = 17.1 kΩ 0x2B = 17.5 kΩ 0x2C = 18.1 kΩ 0x2D = 18.5 kΩ 0x2E = 18.8 kΩ

Table 1-556. R844 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x2F = 19.2 kΩ 0x30 = 19.6 kΩ 0x31 = 20 kΩ 0x32 = 20.3 kΩ 0x33 = 20.7 kΩ 0x34 = 21.3 kΩ 0x35 = 21.7 kΩ 0x36 = 22.1 kΩ 0x37 = 22.5 kΩ 0x38 = 22.8 kΩ 0x39 = 23.2 kΩ 0x3A = 23.6 kΩ 0x3B = 24 kΩ 0x3C = 24.6 kΩ 0x3D = 25 kΩ 0x3E = 25.3 kΩ 0x3F = 25.7 kΩ

1.555 R845 (Offset = 0x34D)

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Table 1-557. R845 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	PLL3_LF_C3	R/W	0x7	PLL Loop Filter C3 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

Table 1-557. R845 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	PLL3_LF_C4	R/W	0x7	PLL Loop Filter C4 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

1.556 R846 (Offset = 0x34E)

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Table 1-558. R846 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL3_RDIV_8:8	R/W	0x0	See Register 847

1.557 R847 (Offset = 0x34F)

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Table 1-559. R847 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_RDIV	R/W	0x0	PLL R Divider ROM=Y, EEPROM=Y

1.558 R848 (Offset = 0x350)

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Table 1-560. R848 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL3_RDIV_XO_EN	R/W	0x1	APLL reference source is from XO. Must also enable XO to drive this APLL with XO_OUT_BUF_EN[3] = 1 ROM=Y, EEPROM=Y

Table 1-560. R848 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PLL3_RDIV_XO_DBLR_EN	R/W	0x1	Enables XO Doubler ROM=Y, EEPROM=Y
2	PLL3_RDIV_BYPASS_EN	R/W	0x1	Bypass R Divider ROM=Y, EEPROM=Y
1:0	PLL3_RDIV_MUX_SEL	R/W	0x0	Select R Divider input: 0=XO, 1=VCO1 feedback divider, 2=VCO2 feedback divider ROM=Y, EEPROM=Y 0x0 = XO 0x1 = VCO1 feedback divider 0x2 = VCO2 feedback divider

1.559 R849 (Offset = 0x351)

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Table 1-561. R849 Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL3_NDIV_8:8	R/W	0x0	See Register 850

1.560 R850 (Offset = 0x352)

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Table 1-562. R850 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NDIV	R/W	0x19	PLL N Divider ROM=Y, EEPROM=Y

1.561 R851 (Offset = 0x353)

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Table 1-563. R851 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_MSB	R/W	0x4C	When PLL3_MODE is set for 24 bit fractional. PLL3_NUM_MSB is effective PLL3_NUM[23:16]. Other PLL3_NUM and PLL3_DEN bits in programmable mode are in PLL3_NUM field. When in 40-bit fixed denominator PLL mode, then PLL3_NUM_MSB is unused. ROM=Y, EEPROM=Y

1.562 R852 (Offset = 0x354)

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Table 1-564. R852 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_39:32	R/W	0x99	See Register 856

1.563 R853 (Offset = 0x355)

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Table 1-565. R853 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_31:24	R/W	0x99	See Register 856

1.564 R854 (Offset = 0x356)

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Table 1-566. R854 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_23:16	R/W	0x99	See Register 856

1.565 R855 (Offset = 0x357)

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Table 1-567. R855 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_15:8	R/W	0x99	See Register 856

1.566 R856 (Offset = 0x358)

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Table 1-568. R856 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM	R/W	0x9A	When PLL3_MODE = 1 (40-bit fixed denominator) mode then PLL3_NUM contains the APLL3 numerator. When PLL3_MODE = 0 (24-bit programmable denominator) then PLL3_NUM[23:0] stores the programmable PLL3 denominator and PLL3_NUM[39:24] stores the 16 LSBs of the PLL3 numerator. Total PLL3 numerator is calculated with PLL3_NUM_MSB as the 8 MSBs. In 24-bit programmable denominator mode PLL3_NUM[23:0] = 0 is 2^{24}. ROM=Y, EEPROM=Y

1.567 R857 (Offset = 0x359)

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Table 1-569. R857 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	PLL3_DTHRMODE	R/W	0x0	PLL MASH Dither Mode ROM=Y, EEPROM=N 0x0 = Constant Dither MACC2 0x1 = Constant Dither MACC2 and MACC3 0x2 = LFSR Dither MACC2 0x3 = Dither Disabled
3:1	PLL3_ORDER	R/W	0x2	PLL MASH Order ROM=Y, EEPROM=N 0x0 = Integer Mode Divider 0x1 = 1st 0x2 = 2nd 0x3 = 3rd
0	PLL3_MODE	R/W	0x1	In APLL 24-bit num/den mode, APLL denominator is programmable. Recommended not for use with DPLL mode. In 24-bit mode, the denominator is stored in PLL3_NUM[23:0] The numerator is stored in (PLL3_NUM_MSB << 16) + PLL3_NUM[39:24]. In APLL 40-bit mode, APLL denominator is fixed. For use with DPLL. ROM=Y, EEPROM=Y 0x0 = APLL 24-bit num/den 0x1 = APLL 40-bit num (Req for DPLL)

1.568 R858 (Offset = 0x35A)

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Table 1-570. R858 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL3_NUM_STAT_39:32	R	0x9A	See Register 862

1.569 R859 (Offset = 0x35B)

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Table 1-571. R859 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL3_NUM_STAT_31:24	R	0xDD	See Register 862

1.570 R860 (Offset = 0x35C)

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Table 1-572. R860 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL3_NUM_STAT_23:16	R	0x3C	See Register 862

1.571 R861 (Offset = 0x35D)

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Table 1-573. R861 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL3_NUM_STAT_15:8	R	0xC	See Register 862

1.572 R862 (Offset = 0x35E)

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Table 1-574. R862 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL3_NUM_STAT	R	0xA4	Readback current effective APLL3 Numerator after FDEV and/or DPLL correction ROM=N, EEPROM=N

1.573 R864 (Offset = 0x360)

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Table 1-575. R864 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	PLL3_VCO_BUF_OUT_EN	R/W	0xF	Enables VCO3 to: [0] -> VCO3 Post-divider, [1] -> VCO3 Auxiliary Buffer (TDC1 Reference Clock Buffer, TDC2 Reference Clock Buffer, APLL1 Reference Clock Buffer, APLL2 Reference Clock Buffer, Window Monitor), [2] -> APLL3 N-Divider, [3] -> DPLL3 N-Divider ROM=Y, EEPROM=Y
3	PLL3_VCO_DIV_SYNC_EN	R/W	0x0	PLL3 Divider Sync Enable. Enables synchronization of post-dividers and reference dividers for PLL3. ROM=Y, EEPROM=N
2:0	PLL3_PRI_DIV	R/W	0x4	Sets the VCO3 primary divider divide value from 1 to 8 (div = field value + 1) ROM=Y, EEPROM=Y 0x0 = 1 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = 8

1.574 R865 (Offset = 0x361)

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Table 1-576. R865 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PLL3_VCO_DIV_SEL	R/W	0x0	Selects APLL3 P1 post-divider block or APLL3 P1 followed by additional divide-by 2 block. ROM=Y, EEPROM=Y 0x0 = PLL3 drive off 0x1 = Reserved 0x2 = Divide-by-1-to-8 direct 0x3 = Divide-by-1-to-8 and /2
5	PLL3_VCO_CHAN_DRVR_IN_EN	R/W	0x1	Enables the selected clock (div1to8 or div2) to the VCO3 to Outputs Output Buffer. See PLL3_VCO_DIV1TO8_EN and PLL3_VCO_DIV2_EN. Optimization to prevent unused domain from interacting with active domains. Always on if using PLL3. Might be on to help reduce crosstalk from APLL3. ROM=Y, EEPROM=Y
4	PLL3_P1_OUT14_15_EN	R/W	0x0	Enable VCO3 P1 divider output driver to channel output bank OUT14_15 ROM=Y, EEPROM=Y
3	PLL3_P1_OUT8_13_EN	R/W	0x0	Enable VCO3 P1 divider output driver to channel output bank OUT8_13 ROM=Y, EEPROM=Y
2	PLL3_P1_OUT4_7_EN	R/W	0x0	Enable VCO3 P1 divider output driver to channel output bank OUT4_7 ROM=Y, EEPROM=Y
1	PLL3_P1_OUT2_3_EN	R/W	0x0	Enable VCO3 P1 divider output driver to channel output bank OUT2_3 ROM=Y, EEPROM=Y

Table 1-576. R865 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PLL3_P1_OUT0_1_EN	R/W	0x0	Enable VCO3 P1 divider output driver to channel output bank OUT0_1 ROM=Y, EEPROM=Y

1.575 R866 (Offset = 0x362)

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Table 1-577. R866 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:3	PLL3_VCO_BUF_2REF_EN	R/W	0x3	Enables the APLL3 Div-by-2 cascade divider to [0] -> APLL1 and [1] -> APLL2 reference input for cascade mode. ROM=Y, EEPROM=Y
2	PLL3_WIN_DET_DRVR_EN	R/W	0x1	Enables the APLL3 Div-by-2 cascade divider to reference window detectors input buffer, ROM=Y, EEPROM=N
1:0	PLL3_VCO_BUF_FB_TDC_EN	R/W	0x0	Enables APLL3 Div-by-4 cascade divider to TDC1 and TDC2 for cascade mode [0] = TDC1 driver enable [1] = TDC2 driver enable. ROM=Y, EEPROM=N

1.576 R872 (Offset = 0x368)

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Table 1-578. R872 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	RESERVED	R	0x0	Reserved
3	PLL3_RDIV_OUTPUT_EN	R/W	0x0	If GPIOx_SEL selects PLL3 R/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.577 R882 (Offset = 0x372)

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Table 1-579. R882 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-579. R882 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESERVED	R	0x0	Reserved
5	PLL3_NDIV_OUTPUT_EN	R/W	0x0	If GPIOx_SEL selects PLL3 N/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.578 R961 (Offset = 0x3C1)

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Table 1-580. R961 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_0_EN	R/W	0x1	OUT0 Enable. If CMOS on OUT0 is used, this enable must also be set. ROM=Y, EEPROM=Y
5:0	OUT_0_FMT	R/W	0x0	Remix of OUT_0_VOD and OUT_0_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.579 R962 (Offset = 0x3C2)

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Table 1-581. R962 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_0_CAP_EN	R/W	0x1	If enable, this output capacitor reduces the slew rate of the output clock. ROM=Y, EEPROM=N

Table 1-581. R962 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_0_STATIC_LOW	R/W	0x0	When OUT0 is forced to a static output, this bit determines if the output voltage will be 0: Static Low 1: Static High ROM=Y, EEPROM=N 0x0 = L 0x1 = H
5	OUT_0_P_CMOS_EN	R/W	0x0	OUT0P CMOS Enable. Overrides the OUT_0_VOD setting and makes OUT_0 CMOS. Setting this bit enables of the positive terminal of OUT0 for CMOS outputs. OUT_0_ENABLE must also be set. ROM=Y, EEPROM=Y
4	OUT_0_N_CMOS_EN	R/W	0x0	OUT0N CMOS Enable. Setting this bit enables of the negative terminal of OUT0 for CMOS outputs. OUT_0_ENABLE must also be set. ROM=Y, EEPROM=Y
3	OUT_0_P_INVERT_POLARITY	R/W	0x0	OUT0P CMOS Invert Polarity. Setting this bit inverts the polarity of the positive terminal of OUT0 for CMOS outputs. ROM=Y, EEPROM=N
2	OUT_0_N_INVERT_POLARITY	R/W	0x0	OUT0N CMOS Invert Polarity. Setting this bit inverts the polarity of the negative terminal of OUT0 for CMOS outputs. ROM=Y, EEPROM=N
1	OUT_0_P_FORCELOW	R/W	0x0	OUT0P CMOS Force Low. Setting this bit forces the positive terminal of OUT0 low. ROM=Y, EEPROM=N
0	OUT_0_N_FORCELOW	R/W	0x0	OUT0N CMOS Force Low. Setting this bit forces the negative terminal of OUT0 low. ROM=Y, EEPROM=N

1.580 R963 (Offset = 0x3C3)

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Table 1-582. R963 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_CONFIGURATION	R/W	0x0	OUT0 configuration. Selects from CH0 Bypass, CH1 Bypass, CHDIV0, CHDIV1, CH0/2 low-noise divide by two path, SYSREF, SYSREF + Analog Delay, or static DC H/L. ROM=Y, EEPROM=Y and N 0x0 = CH0/2 0x14 = CHDIV1 0x20 = SYSREF+ADLY 0x21 = SYSREF 0x22 = Static DC 0x28 = CHDIV0 0x40 = CH1 Bypass 0x80 = CH0 Bypass

1.581 R964 (Offset = 0x3C4)

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Table 1-583. R964 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_1_EN	R/W	0x1	OUT1 Enable. If CMOS on OUT1 is used, this enable must also be set. ROM=Y, EEPROM=Y
5:0	OUT_1_FMT	R/W	0x0	Remix of OUT_1_VOD and OUT_1_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.582 R965 (Offset = 0x3C5)

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Table 1-584. R965 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_1_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
6	OUT_1_STATIC_LOW	R/W	0x0	When OUT1 is forced to a static output, this bit determines if the output voltage will be 0=Static Low or 1=Static High ROM=Y, EEPROM=N 0x0 = L 0x1 = H
5	OUT_1_P_CMOS_EN	R/W	0x0	OUT1P CMOS Enable. Setting this bit enables the positive terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=Y
4	OUT_1_N_CMOS_EN	R/W	0x0	OUT1N CMOS Enable. Setting this bit enables the negative terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=Y

Table 1-584. R965 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT_1_P_INVERT_POLARITY	R/W	0x0	OUT1P CMOS Invert Polarity. Setting this bit inverts the polarity of the positive terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=N
2	OUT_1_N_INVERT_POLARITY	R/W	0x0	OUT1N CMOS Invert Polarity. Setting this bit inverts the polarity of the negative terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=N
1	OUT_1_P_FORCELOW	R/W	0x0	OUT1P CMOS Force Low. Setting this bit forces the positive terminal of OUT1 low. ROM=Y, EEPROM=N
0	OUT_1_N_FORCELOW	R/W	0x0	OUT1N CMOS Force Low. Setting this bit forces the negative terminal of OUT1 low. ROM=Y, EEPROM=N

1.583 R966 (Offset = 0x3C6)

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Table 1-585. R966 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_1_CONFIGURATION	R/W	0x0	OUT1 configuration. Selects from CH0 Bypass, CH1 Bypass, CHDIV0, CHDIV1, CH0/2 low-noise divide by two path, SYSREF, SYSREF + Analog Delay, or static DC H/L. ROM=Y, EEPROM=Y and N 0x0 = CH0/2 0x14 = CHDIV1 0x20 = SYSREF+ADLY 0x21 = SYSREF 0x22 = Static DC 0x28 = CHDIV0 0x40 = CH1 Bypass 0x80 = CH0 Bypass

1.584 R967 (Offset = 0x3C7)

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Table 1-586. R967 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	OUT_0_1_CMOS_OUT_VOLTAGE_SEL	R/W	0x0	CMOS LDO Voltage. Selects CMOS LDO voltage. ROM=Y, EEPROM=Y 0x0 = 1.8 V 0x1 = 2.65 V

Table 1-586. R967 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OUT_0_1_CMOS_OUT_LDO_EN	R/W	0x0	CMOS LDO Enable. Enables LDO used for CMOS outputs. Must be enabled for CMOS mode. ROM=Y, EEPROM=Y

1.585 R968 (Offset = 0x3C8)

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Table 1-587. R968 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:1	OUT_0_1_ZDM_TDC_SEL	R/W	0x0	Select zero delay output to TDC's ROM=Y, EEPROM=N 0x0 = None 0x1 = TDC1 0x2 = TDC2 0x4 = TDC3
0	OUT_0_1_ZDM_EN	R/W	0x0	Enable the output from CH_DIV0_1 to be used as DPLL feedback input for zero delay mode ROM=Y, EEPROM=N

1.586 R969 (Offset = 0x3C9)

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Table 1-588. R969 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_0_1_DIV_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
5	OUT_0_1_DIV_SYNC_EN	R/W	0x1	OUT0_1 Divider Sync Enable. Enables synchronization of chandiv and div2 dividers for OUT0_1. ROM=Y, EEPROM=N
4	OUT_0_1_SR_DIV_SYNC_EN	R/W	0x1	OUT0_1 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT0_1. ROM=Y, EEPROM=N
3	OUT_0_1_CH0_CHAN_POL_SEL	R/W	0x0	OUT0_1 Ch0 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.
2	OUT_0_1_CH1_CHAN_POL_SEL	R/W	0x0	OUT0_1 Ch1 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.

Table 1-588. R969 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OUT_0_1_CH0_DIV_EN	R/W	0x1	OUT0_1 Ch0 ChanDiv Enable. Enables the Ch0 channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y
0	OUT_0_1_CH1_DIV_EN	R/W	0x1	OUT0_1 Ch1 ChanDiv Enable. Enables the Ch1 channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.587 R971 (Offset = 0x3CB)

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Table 1-589. R971 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CLK_IN_SEL	R/W	0x0	OUT0_1 grouped clock input control to CH0 and CH1. ROM=Y, EEPROM=Y 0x0 = CH0 DISABLED, CH1 DISABLED 0x40 = CH0 DISABLED, PLL3 to CH1 0x80 = PLL3 to CH0, CH1 DISABLED 0xC0 = PLL3 to CH0, PLL3 to CH1 0x100 = CH0 DISABLED, REFx to CH1 0x101 = CH0 DISABLED, XO to CH1 0x102 = CH0 DISABLED, PLL1_SEC to CH1 0x103 = CH0 DISABLED, PLL1_PRI to CH1 0x104 = CH0 DISABLED, PLL2 to CH1 0x180 = PLL3 to CH0, REFx to CH1 0x181 = PLL3 to CH0, XO to CH1 0x182 = PLL3 to CH0, PLL1_SEC to CH1 0x183 = PLL3 to CH0, PLL1_PRI to CH1 0x184 = PLL3 to CH0, PLL2 to CH1 0x200 = REFx to CH0, CH1 DISABLED 0x208 = XO to CH0, CH1 DISABLED 0x210 = PLL1_SEC to CH0, CH1 DISABLED 0x218 = PLL1_PRI to CH0, CH1 DISABLED 0x220 = PLL2 to CH0, CH1 DISABLED 0x240 = REFx to CH0, PLL3 to CH1 0x248 = XO to CH0, PLL3 to CH1 0x250 = PLL1_SEC to CH0, PLL3 to CH1 0x258 = PLL1_PRI to CH0, PLL3 to CH1 0x260 = PLL2 to CH0, PLL3 to CH1 0x300 = REFx to CH0, REFx to CH1 0x301 = REFx to CH0, XO to CH1 0x302 = REFx to CH0, PLL1_SEC to CH1 0x303 = REFx to CH0, PLL1_PRI to CH1 0x304 = REFx to CH0, PLL2 to CH1 0x308 = XO to CH0, REFx to CH1 0x309 = XO to CH0, XO to CH1 0x30A = XO to CH0, PLL1_SEC to CH1 0x30B = XO to CH0, PLL1_PRI to CH1 0x30C = XO to CH0, PLL2 to CH1 0x310 = PLL1_SEC to CH0, REFx to CH1 0x311 = PLL1_SEC to CH0, XO to CH1 0x312 = PLL1_SEC to CH0, PLL1_SEC to CH1 0x313 = PLL1_SEC to CH0, PLL1_PRI to CH1 0x314 = PLL1_SEC to CH0, PLL2 to CH1 0x318 = PLL1_PRI to CH0, REFx to CH1 0x319 = PLL1_PRI to CH0, XO to CH1 0x31A = PLL1_PRI to CH0, PLL1_SEC to CH1 0x31B = PLL1_PRI to CH0, PLL1_PRI to CH1 0x31C = PLL1_PRI to CH0, PLL2 to CH1 0x320 = PLL2 to CH0, REFx to CH1 0x321 = PLL2 to CH0, XO to CH1 0x322 = PLL2 to CH0, PLL1_SEC to CH1

Table 1-589. R971 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x323 = PLL2 to CH0, PLL1_PRI to CH1 0x324 = PLL2 to CH0, PLL2 to CH1

1.588 R972 (Offset = 0x3CC)

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Table 1-590. R972 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	OUT_0_1_CH0_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT0_1 Ch0 ChanDiv to SYSREF Input Clock Select. When set, the Ch0 channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N 0x0 = POS POL to SR_DIV 0x1 = NEG POL to SR_DIV
0	RESERVED	R	0x0	Reserved

1.589 R973 (Offset = 0x3CD)

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Table 1-591. R973 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	OUT_0_1_CLK_IN_FANOUT	R/W	0x0	OUT0_1 input clock fanout. Distributes the input clock to the channel dividers and the standalone divide-by-2s. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x3 = IN1 to CHDIV1 0x4 = IN0 to SYSREF 0x7 = IN0 to SYSREF, IN1 to CHDIV1 0xC = IN0 to CHDIV0 0xF = IN0 to CHDIV0, IN1 to CHDIV1 0x10 = IN0 to CH0/2 (OUT0) 0x13 = IN0 to CH0/2 (OUT0), IN1 to CHDIV1 (OUT1) 0x14 = IN0 to CH0/2 (OUT0) and SYSREF (OUT1) 0x1C = IN0 to CH0/2 (OUT0) and CHDIV0 (OUT1) 0x20 = IN0 to CH0/2 (OUT1) 0x23 = IN0 to CH0/2 (OUT1), IN1 to CHDIV1 (OUT0) 0x24 = IN0 to CH0/2 (OUT1) and SYSREF (OUT0) 0x2C = IN0 to CH0/2 (OUT1) and CHDIV0 (OUT0) 0x30 = IN0 to CH0/2 (OUT0 and OUT1)

Table 1-591. R973 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	OUT_0_1_CLK_IN_SEL_9:8	R/W	0x0	OUT0_1 grouped clock input control to CH0 and CH1. ROM=Y, EEPROM=Y 0x0 = CH0 DISABLED, CH1 DISABLED 0x40 = CH0 DISABLED, PLL1 to CH1 0x80 = PLL3 to CH0, CH1 DISABLED 0xC0 = PLL3 to CH0, PLL3 to CH1 0x100 = CH0 DISABLED, REFx to CH1 0x101 = CH0 DISABLED, XO to CH1 0x102 = CH0 DISABLED, PLL1_SEC to CH1 0x103 = CH0 DISABLED, PLL1_PRI to CH1 0x104 = CH0 DISABLED, PLL2 to CH1 0x180 = PLL3 to CH0, REFx to CH1 0x181 = PLL3 to CH0, XO to CH1 0x182 = PLL3 to CH0, PLL1_SEC to CH1 0x183 = PLL3 to CH0, PLL1_PRI to CH1 0x184 = PLL3 to CH0, PLL2 to CH1 0x200 = REFx to CH0, CH1 DISABLED 0x208 = XO to CH0, CH1 DISABLED 0x210 = PLL1_SEC to CH0, CH1 DISABLED 0x218 = PLL1_PRI to CH0, CH1 DISABLED 0x220 = PLL2 to CH0, CH1 DISABLED 0x240 = REFx to CH0, PLL3 to CH1 0x248 = XO to CH0, PLL3 to CH1 0x250 = PLL1_SEC to CH0, PLL3 to CH1 0x258 = PLL1_PRI to CH0, PLL3 to CH1 0x260 = PLL2 to CH0, PLL3 to CH1 0x300 = REFx to CH0, REFx to CH1 0x301 = REFx to CH0, XO to CH1 0x302 = REFx to CH0, PLL1_SEC to CH1 0x303 = REFx to CH0, PLL1_PRI to CH1 0x304 = REFx to CH0, PLL2 to CH1 0x308 = XO to CH0, REFx to CH1 0x309 = XO to CH0, XO to CH1 0x30A = XO to CH0, PLL1_SEC to CH1 0x30B = XO to CH0, PLL1_PRI to CH1 0x30C = XO to CH0, PLL2 to CH1 0x310 = PLL1_SEC to CH0, REFx to CH1 0x311 = PLL1_SEC to CH0, XO to CH1 0x312 = PLL1_SEC to CH0, PLL1_SEC to CH1 0x313 = PLL1_SEC to CH0, PLL1_PRI to CH1 0x314 = PLL1_SEC to CH0, PLL2 to CH1 0x318 = PLL1_PRI to CH0, REFx to CH1 0x319 = PLL1_PRI to CH0, XO to CH1 0x31A = PLL1_PRI to CH0, PLL1_SEC to CH1 0x31B = PLL1_PRI to CH0, PLL1_PRI to CH1 0x31C = PLL1_PRI to CH0, PLL2 to CH1 0x320 = PLL2 to CH0, REFx to CH1 0x321 = PLL2 to CH0, XO to CH1 0x322 = PLL2 to CH0, PLL1_SEC to CH1

Table 1-591. R973 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x323 = PLL2 to CH0, PLL1_PRI to CH1 0x324 = PLL2 to CH0, PLL2 to CH1

1.590 R974 (Offset = 0x3CE)

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Table 1-592. R974 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH0_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 975

1.591 R975 (Offset = 0x3CF)

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Table 1-593. R975 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH0_CH_STATIC_OFFSET	R/W	0x0	CH0_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.592 R976 (Offset = 0x3D0)

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Table 1-594. R976 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH1_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 977

1.593 R977 (Offset = 0x3D1)

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Table 1-595. R977 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH1_CH_STATIC_OFFSET	R/W	0x0	CH1_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.594 R978 (Offset = 0x3D2)

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Table 1-596. R978 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH0_CH_DIV_11:8	R/W	0x0	See Register 979

1.595 R979 (Offset = 0x3D3)

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Table 1-597. R979 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH0_CH_DIV	R/W	0xA	OUT0_1 Ch0 Channel Divider (ChanDiv) Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.596 R980 (Offset = 0x3D4)

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Table 1-598. R980 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH1_CH_DIV_11:8	R/W	0x0	See Register 981

1.597 R981 (Offset = 0x3D5)

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Table 1-599. R981 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH1_CH_DIV	R/W	0xA	OUT0_1 Ch1 Channel Divider (ChanDiv) Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.598 R982 (Offset = 0x3D6)

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Table 1-600. R982 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_0_1_SR_ANA_DELAY	R/W	0x0	OUT0_1 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.599 R983 (Offset = 0x3D7)

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Table 1-601. R983 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_0_1_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT0_1 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_0_1_SR_ANA_DELAY_EN	R/W	0x0	OUT0_1 SYSREF Analog Delay Enable. ROM=Y, EEPROM=N
3	OUT_0_1_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x1	OUT0_1 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N

Table 1-601. R983 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	OUT_0_1_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.600 R984 (Offset = 0x3D8)

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Table 1-602. R984 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_0_1_SR_DDLY	R/W	0x0	OUT0_1 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.601 R985 (Offset = 0x3D9)

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Table 1-603. R985 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_SR_DIV_19:16	R/W	0x0	See Register 987

1.602 R986 (Offset = 0x3DA)

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Table 1-604. R986 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_SR_DIV_15:8	R/W	0x1	See Register 987

1.603 R987 (Offset = 0x3DB)

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Table 1-605. R987 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_SR_DIV	R/W	0x0	OUT0_1 SYSREF Divide Value. ROM=Y, EEPROM=N

1.604 R988 (Offset = 0x3DC)

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Table 1-606. R988 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_0_1_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 989

1.605 R989 (Offset = 0x3DD)

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Table 1-607. R989 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT_0_1_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.606 R990 (Offset = 0x3DE)

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Table 1-608. R990 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_0_1_SR_REQ_MODE	R/W	0x0	OUT0_1 SYSREF Mute Enable ROM=Y, EEPROM=N
6	OUT_0_1_SR_GPIO_EN	R/W	0x0	Enable SYSREF to digital for SYSREF request resampling, continuous SYSREF, 1-PPS GPIO output, 1-PPS phase validation. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved

Table 1-608. R990 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:2	OUT_0_1_PULSE_COUNT	R/W	0x0	OUT0_1 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
1:0	OUT_0_1_SR_MODE	R/W	0x0	OUT0_1 SYSREF Mode. Selects Pulser mode, Continuous mode, or None. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.607 R991 (Offset = 0x3DF)

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Table 1-609. R991 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_0_1_SR_CH0_DIV_BYPASS	R/W	0x1	OUT0_1 cascaded SYSREF bypass mux. If set, bypasses CHDIV0 for the SYSREF input clock. Using CHDIV bypass is practical when SYSREF is required but CHDIV is not used. VCO post divide frequency must be ≤ 2 GHz to bypass CHDIV. ROM=Y, EEPROM=N 0x0 = CHDIV 0x1 = CHDIV Byp
4:0	RESERVED	R	0x0	Reserved

1.608 R1024 (Offset = 0x400)

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Table 1-610. R1024 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_2_EN	R/W	0x1	OUT2 Enable. ROM=Y, EEPROM=Y

Table 1-610. R1024 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	OUT_2_FMT	R/W	0x0	Remix of OUT_2_VOD and OUT_2_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.609 R1025 (Offset = 0x401)

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Table 1-611. R1025 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT_2_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
2:0	OUT_2_CONFIGURATION	R/W	0x0	OUT2 configuration. ROM=Y, EEPROM=Y and N 0x2 = Static DC 0x3 = CHDIV 0x4 = BYPASS 0x5 = BYPASS

1.610 R1026 (Offset = 0x402)

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Table 1-612. R1026 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_2_CHAN_POL_SEL	R/W	0x0	OUT2 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.

Table 1-612. R1026 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	OUT_2_CLK_MUX	R/W	0x0	OUT2 Input Clock Select. Selects the input clock which will be used to drive the output. ROM=Y, EEPROM=Y 0x0 = PLL3 0x1 = PLL2 0x2 = PLL1_PRI
4	RESERVED	R	0x0	Reserved
3	OUT_2_DIV_EN	R/W	0x1	OUT2 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y
2:0	OUT_2_CH_MUX_SEL	R/W	0x7	OUT2 Clock Enable. Bit 2, if set, passes the selected VCO1 clock (VCO1P or VCO1S), to the second stage of clock selection. Bit 1 and Bit0 enable the selected clock to drive the channel divider and the channel divider retimer respectively. ROM=Y, EEPROM=Y 0x0 = PLL2->BYPASS 0x3 = PLL2->CHDIV 0x4 = PLL1->BYPASS 0x7 = PLL1->CHDIV

1.611 R1027 (Offset = 0x403)

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Table 1-613. R1027 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OUT_2_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
3	OUT_2_SYNC_EN	R/W	0x1	OUT2 ChanDiv Sync Enable. Enables synchronization of chandiv dividers for OUT2. ROM=Y, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.612 R1028 (Offset = 0x404)

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Table 1-614. R1028 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_2_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1029

1.613 R1029 (Offset = 0x405)

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Table 1-615. R1029 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_2_CH_STATIC_OFFSET	R/W	0x0	OUT_2_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.614 R1030 (Offset = 0x406)

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Table 1-616. R1030 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_2_CH_DIV_11:8	R/W	0x0	See Register 1031

1.615 R1031 (Offset = 0x407)

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Table 1-617. R1031 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_2_CH_DIV	R/W	0x4	OUT2 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.616 R1056 (Offset = 0x420)

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Table 1-618. R1056 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_3_EN	R/W	0x1	OUT3 Enable. ROM=Y, EEPROM=Y

Table 1-618. R1056 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	OUT_3_FMT	R/W	0x0	Remix of OUT_3_VOD and OUT_3_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.617 R1057 (Offset = 0x421)

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Table 1-619. R1057 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT_3_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
2:0	OUT_3_CONFIGURATION	R/W	0x0	OUT3 configuration. ROM=Y, EEPROM=Y and N 0x2 = Static DC 0x3 = CHDIV 0x4 = BYPASS 0x5 = BYPASS

1.618 R1058 (Offset = 0x422)

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Table 1-620. R1058 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_3_CHAN_POL_SEL	R/W	0x0	OUT3 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.

Table 1-620. R1058 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	OUT_3_CLK_MUX	R/W	0x0	OUT3 Input Clock Select. Selects the input clock which will be used to drive the output. ROM=Y, EEPROM=Y 0x0 = PLL3 0x1 = PLL2 0x2 = PLL1_PRI
4	RESERVED	R	0x0	Reserved
3	OUT_3_DIV_EN	R/W	0x1	OUT3 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y
2:0	OUT_3_CH_MUX_SEL	R/W	0x7	OUT3 Clock Enable. Bit 2, if set, passes the selected VCO1 clock (VCO1P or VCO1S), to the second stage of clock selection. Bit 1 and Bit0 enable the selected clock to drive the channel divider and the channel divider retimer respectively. ROM=Y, EEPROM=Y 0x0 = PLL2->BYPASS 0x3 = PLL2->CHDIV 0x4 = PLL1->BYPASS 0x7 = PLL1->CHDIV

1.619 R1059 (Offset = 0x423)

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Table 1-621. R1059 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OUT_3_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
3	OUT_3_SYNC_EN	R/W	0x1	OUT3 ChanDiv Sync Enable. Enables synchronization of chandiv dividers for OUT3. ROM=Y, EEPROM=N
2:0	RESERVED	R	0x0	Reserved

1.620 R1060 (Offset = 0x424)

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Table 1-622. R1060 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_3_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1061

1.621 R1061 (Offset = 0x425)

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Table 1-623. R1061 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_3_CH_STATIC_OFFSET	R/W	0x0	OUT_3_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.622 R1062 (Offset = 0x426)

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Table 1-624. R1062 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_3_CH_DIV_11:8	R/W	0x0	See Register 1063

1.623 R1063 (Offset = 0x427)

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Table 1-625. R1063 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_3_CH_DIV	R/W	0x2	OUT3 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.624 R1088 (Offset = 0x440)

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Table 1-626. R1088 Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:0	OUT_4_5_SR_ANA_DLY_BIASTRIM	R/W	0x4	Channel Analog Delay Bias Trim ROM=N, EEPROM=Y

1.625 R1089 (Offset = 0x441)

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Table 1-627. R1089 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_4_EN	R/W	0x1	OUT4 Enable. ROM=Y, EEPROM=Y
5:0	OUT_4_FMT	R/W	0x0	Remix of OUT_4_VOD and OUT_4_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.626 R1090 (Offset = 0x442)

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Table 1-628. R1090 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_4_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_4_CONFIGURATION	R/W	0x0	OUT4 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.627 R1091 (Offset = 0x443)

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Table 1-629. R1091 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_5_EN	R/W	0x1	OUT5 Enable. ROM=Y, EEPROM=Y
5:0	OUT_5_FMT	R/W	0x0	Remix of OUT_5_VOD and OUT_5_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.628 R1092 (Offset = 0x444)

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Table 1-630. R1092 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_5_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_5_CONFIGURATION	R/W	0x0	OUT5 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.629 R1093 (Offset = 0x445)

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Table 1-631. R1093 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_4_5_DIV_SYNC_EN	R/W	0x1	OUT4_5 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT4_5. ROM=Y, EEPROM=N
4	OUT_4_5_SR_DIV_SYNC_EN	R/W	0x1	OUT4_5 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT4_5. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_4_5_CHAN_POL_SEL	R/W	0x0	OUT4_5 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.
0	OUT_4_5_DIV_EN	R/W	0x1	OUT4_5 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.630 R1094 (Offset = 0x446)

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Table 1-632. R1094 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_4_5_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	OUT_4_5_ZDM_EN	R/W	0x0	OUT4_5 zero delay output enable ROM=Y, EEPROM=N
5	OUT_4_5_CLK_IN_SEL	R/W	0x0	OUT4_5 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_4_5_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT4_5 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N

Table 1-632. R1094 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT_4_5_CH_MUX_SEL	R/W	0x3	OUT4_5 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT4, [3] -> Div2 to OUT5 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT4 0x5 = DIV2->OUT4, SYSREF->OUT5 0x7 = DIV2->OUT4, CHDIV->OUT5 0x8 = DIV2->OUT5 0x9 = SYSREF->OUT4, DIV2->OUT5 0xB = CHDIV->OUT4, DIV2->OUT5 0xC = DIV2->OUT4, DIV2->OUT5

1.631 R1095 (Offset = 0x447)

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Table 1-633. R1095 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_4_5_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1096

1.632 R1096 (Offset = 0x448)

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Table 1-634. R1096 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_CH_STATIC_OFFSET	R/W	0x0	OUT_4_5_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.633 R1097 (Offset = 0x449)

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Table 1-635. R1097 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_4_5_CH_DIV_11:8	R/W	0x0	See Register 1098

1.634 R1098 (Offset = 0x44A)

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Table 1-636. R1098 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_CH_DIV	R/W	0x2	OUT4_5 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.635 R1099 (Offset = 0x44B)

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Table 1-637. R1099 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_4_5_SR_ANA_DELAY	R/W	0x0	OUT4_5 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.636 R1100 (Offset = 0x44C)

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Table 1-638. R1100 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_4_5_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT4_5 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_4_5_SR_ANA_DELAY_EN	R/W	0x0	OUT4_5 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N

Table 1-638. R1100 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT_4_5_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x1	OUT4_5 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_4_5_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.637 R1101 (Offset = 0x44D)

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Table 1-639. R1101 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_4_5_SR_DDLY	R/W	0x0	OUT4_5 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.638 R1102 (Offset = 0x44E)

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Table 1-640. R1102 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_4_5_SR_DIV_19:16	R/W	0x0	See Register 1104

1.639 R1103 (Offset = 0x44F)

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Table 1-641. R1103 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_SR_DIV_15:8	R/W	0x0	See Register 1104

1.640 R1104 (Offset = 0x450)

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Table 1-642. R1104 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_SR_DIV	R/W	0xB4	OUT4_5 SYSREF Divide Value. ROM=Y, EEPROM=N

1.641 R1105 (Offset = 0x451)

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Table 1-643. R1105 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_4_5_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1106

1.642 R1106 (Offset = 0x452)

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Table 1-644. R1106 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT_4_5_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.643 R1107 (Offset = 0x453)

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Table 1-645. R1107 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-645. R1107 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_4_5_SR_REQ_MODE	R/W	0x0	OUT4_5 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_4_5_PULSE_COUNT	R/W	0x0	OUT4_5 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_4_5_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_4_5_SR_MODE	R/W	0x0	OUT4_5 SYSREF Mode. When these bits are set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in Pulse Mode. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.644 R1108 (Offset = 0x454)

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Table 1-646. R1108 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4	OUT_4_5_SR_CH_DIV_BYPASS	R/W	0x1	OUT4_5 cascaded SYSREF bypass mux. If set, bypasses OUT4_5 channel divider for the SYSREF input clock. Using CHDIV bypass is practical when SYSREF is required but CHDIV is not used. VCO post divide frequency must be ≤ 2 GHz to bypass CHDIV. ROM=Y, EEPROM=N 0x0 = CHDIV 0x1 = CHDIV Byp
3:0	RESERVED	R	0x0	Reserved

1.645 R1121 (Offset = 0x461)

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Table 1-647. R1121 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_6_EN	R/W	0x1	OUT6 Enable. ROM=Y, EEPROM=Y

Table 1-647. R1121 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	OUT_6_FMT	R/W	0x0	Remix of OUT_6_VOD and OUT_6_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.646 R1122 (Offset = 0x462)

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Table 1-648. R1122 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_6_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_6_CONFIGURATION	R/W	0x0	OUT6 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.647 R1123 (Offset = 0x463)

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Table 1-649. R1123 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-649. R1123 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_7_EN	R/W	0x1	OUT7 Enable. ROM=Y, EEPROM=Y
5:0	OUT_7_FMT	R/W	0x0	Remix of OUT_7_VOD and OUT_7_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.648 R1124 (Offset = 0x464)

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Table 1-650. R1124 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_7_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_7_CONFIGURATION	R/W	0x0	OUT7 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.649 R1125 (Offset = 0x465)

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Table 1-651. R1125 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_6_7_DIV_SYNC_EN	R/W	0x1	OUT6_7 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT6_7. ROM=Y, EEPROM=N
4	OUT_6_7_SR_DIV_SYNC_EN	R/W	0x1	OUT6_7 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT6_7. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_6_7_CHAN_POL_SEL	R/W	0x0	OUT6_7 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.
0	OUT_6_7_DIV_EN	R/W	0x1	OUT6_7 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.650 R1126 (Offset = 0x466)

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Table 1-652. R1126 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_6_7_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	RESERVED	R	0x0	Reserved
5	OUT_6_7_CLK_IN_SEL	R/W	0x0	OUT6_7 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_6_7_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT6_7 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N

Table 1-652. R1126 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT_6_7_CH_MUX_SEL	R/W	0x3	OUT6_7 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT6, [3] -> Div2 to OUT7 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT6 0x5 = DIV2->OUT6, SYSREF->OUT7 0x7 = DIV2->OUT6, CHDIV->OUT7 0x8 = DIV2->OUT7 0x9 = SYSREF->OUT6, DIV2->OUT7 0xB = CHDIV->OUT6, DIV2->OUT7 0xC = DIV2->OUT6, DIV2->OUT7

1.651 R1127 (Offset = 0x467)

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Table 1-653. R1127 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_6_7_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1128

1.652 R1128 (Offset = 0x468)

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Table 1-654. R1128 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_CH_STATIC_OFFSET	R/W	0x0	OUT_6_7_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.653 R1129 (Offset = 0x469)

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Table 1-655. R1129 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_6_7_CH_DIV_11:8	R/W	0x0	See Register 1130

1.654 R1130 (Offset = 0x46A)

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Table 1-656. R1130 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_CH_DIV	R/W	0x2	OUT6_7 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.655 R1131 (Offset = 0x46B)

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Table 1-657. R1131 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_6_7_SR_ANA_DELAY	R/W	0x0	OUT6_7 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.656 R1132 (Offset = 0x46C)

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Table 1-658. R1132 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_6_7_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT6_7 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_6_7_SR_ANA_DELAY_EN	R/W	0x0	OUT6_7 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N

Table 1-658. R1132 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT_6_7_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x1	OUT6_7 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_6_7_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.657 R1133 (Offset = 0x46D)

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Table 1-659. R1133 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_6_7_SR_DDLY	R/W	0x0	OUT6_7 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.658 R1134 (Offset = 0x46E)

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Table 1-660. R1134 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_6_7_SR_DIV_19:16	R/W	0x0	See Register 1136

1.659 R1135 (Offset = 0x46F)

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Table 1-661. R1135 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_SR_DIV_15:8	R/W	0x0	See Register 1136

1.660 R1136 (Offset = 0x470)

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Table 1-662. R1136 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_SR_DIV	R/W	0x5A	OUT6_7 SYSREF Divide Value. ROM=Y, EEPROM=N

1.661 R1137 (Offset = 0x471)

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Table 1-663. R1137 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_6_7_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1138

1.662 R1138 (Offset = 0x472)

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Table 1-664. R1138 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT_6_7_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.663 R1139 (Offset = 0x473)

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Table 1-665. R1139 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-665. R1139 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_6_7_SR_REQ_MODE	R/W	0x0	OUT6_7 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_6_7_PULSE_COUNT	R/W	0x0	OUT6_7 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_6_7_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_6_7_SR_MODE	R/W	0x0	OUT6_7 SYSREF Mode. When these bits are set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.664 R1140 (Offset = 0x474)

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Table 1-666. R1140 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4	OUT_6_7_SR_CH_DIV_BYPASS	R/W	0x1	OUT6_7 cascaded SYSREF bypass mux. If set, bypasses OUT6_7 channel divider for the SYSREF input clock. Using CHDIV bypass is practical when SYSREF is required but CHDIV is not used. VCO post divide frequency must be ≤ 2 GHz to bypass CHDIV. ROM=Y, EEPROM=N 0x0 = CHDIV 0x1 = CHDIV Byp
3:0	RESERVED	R	0x0	Reserved

1.665 R1153 (Offset = 0x481)

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Table 1-667. R1153 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_8_EN	R/W	0x1	OUT8 Enable. ROM=Y, EEPROM=Y

Table 1-667. R1153 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	OUT_8_FMT	R/W	0x0	Remix of OUT_8_VOD and OUT_8_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.666 R1154 (Offset = 0x482)

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Table 1-668. R1154 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_8_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_8_CONFIGURATION	R/W	0x0	OUT8 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.667 R1155 (Offset = 0x483)

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Table 1-669. R1155 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-669. R1155 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_9_EN	R/W	0x1	OUT9 Enable. ROM=Y, EEPROM=Y
5:0	OUT_9_FMT	R/W	0x0	Remix of OUT_9_VOD and OUT_9_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.668 R1156 (Offset = 0x484)

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Table 1-670. R1156 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_9_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_9_CONFIGURATION	R/W	0x0	OUT9 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.669 R1157 (Offset = 0x485)

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Table 1-671. R1157 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_8_9_DIV_SYNC_EN	R/W	0x1	OUT8_9 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT8_9. ROM=Y, EEPROM=N
4	OUT_8_9_SR_DIV_SYNC_EN	R/W	0x1	OUT8_9 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT8_9. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_8_9_CHAN_POL_SEL	R/W	0x0	OUT8_9 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.
0	OUT_8_9_DIV_EN	R/W	0x0	OUT8_9 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.670 R1158 (Offset = 0x486)

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Table 1-672. R1158 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_8_9_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	RESERVED	R	0x0	Reserved
5	OUT_8_9_CLK_IN_SEL	R/W	0x1	OUT8_9 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_8_9_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT8_9 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N

Table 1-672. R1158 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT_8_9_CH_MUX_SEL	R/W	0x1	OUT8_9 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT8, [3] -> Div2 to OUT9 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT8 0x5 = DIV2->OUT8, SYSREF->OUT9 0x7 = DIV2->OUT8, CHDIV->OUT9 0x8 = DIV2->OUT9 0x9 = SYSREF->OUT8, DIV2->OUT9 0xB = CHDIV->OUT8, DIV2->OUT9 0xC = DIV2->OUT8, DIV2->OUT9

1.671 R1159 (Offset = 0x487)

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Table 1-673. R1159 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_8_9_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1160

1.672 R1160 (Offset = 0x488)

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Table 1-674. R1160 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_CH_STATIC_OFFSET	R/W	0x0	OUT_8_9_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.673 R1161 (Offset = 0x489)

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Table 1-675. R1161 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_8_9_CH_DIV_11:8	R/W	0x0	See Register 1162

1.674 R1162 (Offset = 0x48A)

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Table 1-676. R1162 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_CH_DIV	R/W	0x4	OUT8_9 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.675 R1163 (Offset = 0x48B)

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Table 1-677. R1163 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_8_9_SR_ANA_DELAY	R/W	0x0	OUT8_9 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.676 R1164 (Offset = 0x48C)

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Table 1-678. R1164 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_8_9_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT8_9 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_8_9_SR_ANA_DELAY_EN	R/W	0x0	OUT8_9 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N

Table 1-678. R1164 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT_8_9_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x1	OUT8_9 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_8_9_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.677 R1165 (Offset = 0x48D)

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Table 1-679. R1165 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_8_9_SR_DDLY	R/W	0x0	OUT8_9 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.678 R1166 (Offset = 0x48E)

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Table 1-680. R1166 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_8_9_SR_DIV_19:16	R/W	0x0	See Register 1168

1.679 R1167 (Offset = 0x48F)

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Table 1-681. R1167 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_SR_DIV_15:8	R/W	0x1	See Register 1168

1.680 R1168 (Offset = 0x490)

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Table 1-682. R1168 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_SR_DIV	R/W	0x0	OUT8_9 SYSREF Divide Value. ROM=Y, EEPROM=N

1.681 R1169 (Offset = 0x491)

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Table 1-683. R1169 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_8_9_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1170

1.682 R1170 (Offset = 0x492)

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Table 1-684. R1170 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT_8_9_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.683 R1171 (Offset = 0x493)

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Table 1-685. R1171 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-685. R1171 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_8_9_SR_REQ_MODE	R/W	0x0	OUT8_9 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_8_9_PULSE_COUNT	R/W	0x0	OUT8_9 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_8_9_SR_GPIO_EN	R/W	0x1	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_8_9_SR_MODE	R/W	0x0	OUT8_9 SYSREF Mode. When these bits are set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.684 R1185 (Offset = 0x4A1)

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Table 1-686. R1185 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_10_EN	R/W	0x1	OUT10 Enable. ROM=Y, EEPROM=Y
5:0	OUT_10_FMT	R/W	0x0	Remix of OUT_10_VOD and OUT_10_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.685 R1186 (Offset = 0x4A2)

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Table 1-687. R1186 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_10_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_10_CONFIGURATION	R/W	0x0	OUT10 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.686 R1187 (Offset = 0x4A3)

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Table 1-688. R1187 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_11_EN	R/W	0x1	OUT11 Enable. ROM=Y, EEPROM=Y
5:0	OUT_11_FMT	R/W	0x0	Remix of OUT_11_VOD and OUT_11_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.687 R1188 (Offset = 0x4A4)

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Table 1-689. R1188 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_11_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_11_CONFIGURATION	R/W	0x0	OUT11 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.688 R1189 (Offset = 0x4A5)

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Table 1-690. R1189 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_10_11_DIV_SYNC_EN	R/W	0x1	OUT10_11 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT10_11. ROM=Y, EEPROM=N
4	OUT_10_11_SR_DIV_SYNC_EN	R/W	0x1	OUT10_11 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT10_11. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_10_11_CHAN_POL_SEL	R/W	0x0	OUT10_11 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.
0	OUT_10_11_DIV_EN	R/W	0x0	OUT10_11 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.689 R1190 (Offset = 0x4A6)

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Table 1-691. R1190 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_10_11_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	OUT_10_11_ZDM_EN	R/W	0x0	OUT10_11 zero delay output enable. ROM=Y, EEPROM=N
5	OUT_10_11_CLK_IN_SEL	R/W	0x1	OUT10_11 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_10_11_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT10_11 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N
3:0	OUT_10_11_CH_MUX_SEL	R/W	0x1	OUT10_11 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT10, [3] -> Div2 to OUT11 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT10 0x5 = DIV2->OUT10, SYSREF->OUT11 0x7 = DIV2->OUT10, CHDIV->OUT11 0x8 = DIV2->OUT11 0x9 = SYSREF->OUT10, DIV2->OUT11 0xB = CHDIV->OUT10, DIV2->OUT11 0xC = DIV2->OUT10, DIV2->OUT11

1.690 R1191 (Offset = 0x4A7)

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Table 1-692. R1191 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_10_11_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1192

1.691 R1192 (Offset = 0x4A8)

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Table 1-693. R1192 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_CH_STATIC_OFFSET	R/W	0x0	OUT_10_11_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.692 R1193 (Offset = 0x4A9)

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Table 1-694. R1193 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_10_11_CH_DIV_11:8	R/W	0x0	See Register 1194

1.693 R1194 (Offset = 0x4AA)

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Table 1-695. R1194 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_CH_DIV	R/W	0x4	OUT10_11 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.694 R1195 (Offset = 0x4AB)

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Table 1-696. R1195 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_10_11_SR_ANA_DELAY	R/W	0x0	OUT10_11 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.695 R1196 (Offset = 0x4AC)

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Table 1-697. R1196 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_10_11_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT10_11 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_10_11_SR_ANA_DELAY_EN	R/W	0x0	OUT10_11 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N
3	OUT_10_11_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x1	OUT10_11 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_10_11_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.696 R1197 (Offset = 0x4AD)

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Table 1-698. R1197 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_10_11_SR_DDLY	R/W	0x0	OUT10_11 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.697 R1198 (Offset = 0x4AE)

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Table 1-699. R1198 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_10_11_SR_DIV_19:16	R/W	0x0	See Register 1200

1.698 R1199 (Offset = 0x4AF)

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Table 1-700. R1199 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_SR_DIV_15:8	R/W	0x1	See Register 1200

1.699 R1200 (Offset = 0x4B0)

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Table 1-701. R1200 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_SR_DIV	R/W	0x0	OUT10_11 SYSREF Divide Value. ROM=Y, EEPROM=N

1.700 R1201 (Offset = 0x4B1)

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Table 1-702. R1201 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_10_11_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1202

1.701 R1202 (Offset = 0x4B2)

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Table 1-703. R1202 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT_10_11_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.702 R1203 (Offset = 0x4B3)

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Table 1-704. R1203 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_10_11_SR_REQ_MODE	R/W	0x0	OUT10_11 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_10_11_PULSE_COUNT	R/W	0x0	OUT10_11 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_10_11_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_10_11_SR_MODE	R/W	0x0	OUT10_11 SYSREF Mode. When these bits are set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.703 R1204 (Offset = 0x4B4)

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Table 1-705. R1204 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4	OUT_10_11_SR_CH_DIV_BYPASS	R/W	0x1	OUT10_11 cascaded SYSREF bypass mux. If set, bypasses OUT10_11 channel divider for the SYSREF input clock. Using CHDIV bypass is practical when SYSREF is required but CHDIV is not used. VCO post divide frequency must be ≤ 2 GHz to bypass CHDIV. ROM=Y, EEPROM=N 0x0 = CHDIV 0x1 = CHDIV Byp

Table 1-705. R1204 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	R	0x0	Reserved

1.704 R1217 (Offset = 0x4C1)

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Table 1-706. R1217 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_12_EN	R/W	0x1	OUT12 Enable. ROM=Y, EEPROM=Y
5:0	OUT_12_FMT	R/W	0x0	Remix of OUT_12_VOD and OUT_12_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.705 R1218 (Offset = 0x4C2)

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Table 1-707. R1218 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_12_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved

Table 1-707. R1218 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	OUT_12_CONFIGURATION	R/W	0x0	OUT12 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.706 R1219 (Offset = 0x4C3)

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Table 1-708. R1219 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_13_EN	R/W	0x1	OUT13 Enable. ROM=Y, EEPROM=Y
5:0	OUT_13_FMT	R/W	0x0	Remix of OUT_13_VOD and OUT_13_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.707 R1220 (Offset = 0x4C4)

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Table 1-709. R1220 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-709. R1220 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT_13_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_13_CONFIGURATION	R/W	0x0	OUT13 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.708 R1221 (Offset = 0x4C5)

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Table 1-710. R1221 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_12_13_DIV_SYNC_EN	R/W	0x1	OUT12_13 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT12_13. ROM=Y, EEPROM=N
4	OUT_12_13_SR_DIV_SYNC_EN	R/W	0x1	OUT12_13 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT12_13. ROM=Y, EEPROM=N
3:2	RESERVED	R	0x0	Reserved
1	OUT_12_13_CHAN_POL_SEL	R/W	0x0	OUT12_13 ChanDiv Polarity Select. This bit flips the polarity of the clock into SYSREF and the polarity of the clock into the channel divider.
0	OUT_12_13_DIV_EN	R/W	0x0	OUT12_13 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.709 R1222 (Offset = 0x4C6)

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Table 1-711. R1222 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_12_13_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	RESERVED	R	0x0	Reserved

Table 1-711. R1222 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	OUT_12_13_CLK_IN_SEL	R/W	0x1	OUT12_13 Input Clock Select. Selects the input clock which will be used to drive the output. For crosstlak performance OUT8 to OUT13 should select the same VCO souce: 0 = VCO2, 1 = VCO3. ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_12_13_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT12_13 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N
3:0	OUT_12_13_CH_MUX_SEL	R/W	0x1	OUT12_13 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT12, [3] -> Div2 to OUT13 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT12 0x5 = DIV2->OUT12, SYSREF->OUT13 0x7 = DIV2->OUT12, CHDIV->OUT13 0x8 = DIV2->OUT13 0x9 = SYSREF->OUT12, DIV2->OUT13 0xB = CHDIV->OUT12, DIV2->OUT13 0xC = DIV2->OUT12, DIV2->OUT13

1.710 R1223 (Offset = 0x4C7)

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Table 1-712. R1223 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_12_13_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1224

1.711 R1224 (Offset = 0x4C8)

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Table 1-713. R1224 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_CH_STATIC_OFFSET	R/W	0x0	OUT_12_13_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.712 R1225 (Offset = 0x4C9)

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Table 1-714. R1225 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_12_13_CH_DIV_11:8	R/W	0x0	See Register 1226

1.713 R1226 (Offset = 0x4CA)

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Table 1-715. R1226 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_CH_DIV	R/W	0x4	OUT12_13 ChanDiv Divide Value. For this 12-bit divider all bits are set by ROM, but 8 LSBs may be overwritten by EEPROM if EEPROM overlay (ROM_PLUS_EE=1) is enabled. ROM=Y, EEPROM=Y

1.714 R1227 (Offset = 0x4CB)

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Table 1-716. R1227 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_12_13_SR_ANA_DELAY	R/W	0x0	OUT12_13 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.715 R1228 (Offset = 0x4CC)

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Table 1-717. R1228 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_12_13_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT12_13 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_12_13_SR_ANA_DELAY_EN	R/W	0x0	OUT12_13 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N
3	OUT_12_13_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x1	OUT12_13 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_12_13_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.716 R1229 (Offset = 0x4CD)

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Table 1-718. R1229 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_12_13_SR_DDLY	R/W	0x0	OUT12_13 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.717 R1230 (Offset = 0x4CE)

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Table 1-719. R1230 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_12_13_SR_DIV_19:16	R/W	0x0	See Register 1232

1.718 R1231 (Offset = 0x4CF)

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Table 1-720. R1231 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_SR_DIV_15:8	R/W	0x1	See Register 1232

1.719 R1232 (Offset = 0x4D0)

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Table 1-721. R1232 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_SR_DIV	R/W	0x0	OUT12_13 SYSREF Divide Value. ROM=Y, EEPROM=N

1.720 R1233 (Offset = 0x4D1)

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Table 1-722. R1233 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_12_13_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1234

1.721 R1234 (Offset = 0x4D2)

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Table 1-723. R1234 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT_12_13_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.722 R1235 (Offset = 0x4D3)

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Table 1-724. R1235 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_12_13_SR_REQ_MODE	R/W	0x0	OUT12_13 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_12_13_PULSE_COUNT	R/W	0x0	OUT12_13 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_12_13_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_12_13_SR_MODE	R/W	0x0	OUT12_13 SYSREF Mode. When these bits are set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.723 R1236 (Offset = 0x4D4)

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Table 1-725. R1236 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R	0x0	Reserved
4	OUT_12_13_SR_CH_DIV_BYPASS	R/W	0x1	OUT12_13 cascaded SYSREF bypass mux. If set, bypasses OUT12_13 channel divider for the SYSREF input clock. Using CHDIV bypass is practical when SYSREF is required but CHDIV is not used. VCO post divide frequency must be ≤ 2 GHz to bypass CHDIV. ROM=Y, EEPROM=N 0x0 = CHDIV 0x1 = CHDIV Byp

Table 1-725. R1236 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	R	0x0	Reserved

1.724 R1248 (Offset = 0x4E0)

Return to the Summary Table.

Table 1-726. R1248 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5:0	OUT_14_FMT	R/W	0x0	Remix of OUT_14_VOD and OUT_14_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

1.725 R1280 (Offset = 0x500)

Return to the Summary Table.

Table 1-727. R1280 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved

Table 1-727. R1280 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	OUT_15_FMT	R/W	0x0	Remix of OUT_15_VOD and OUT_15_VOS to display datasheet specified settings availible to user. ROM=Y, EEPROM=Y 0x8 = HSDS 400 mV, Vcm = 0.35 V 0x9 = HSDS 500 mV, Vcm = 0.4 V 0xA = HSDS 600 mV, Vcm = 0.45 V 0xB = HSDS 700 mV, Vcm = 0.5 V 0xC = HSDS 800 mV, Vcm = 0.55 V 0xD = HSDS 900 mV, Vcm = 0.6 V 0xE = HSDS 1000 mV, Vcm = 0.65 V 0xF = HCSL 750 mV 0x10 = HSDS 400 mV, Vcm = 0.7 V 0x20 = LVDS, Vcm = 1.25 V 0x32 = HSDS 600 mV, Vcm = 0.8 V 0x33 = HSDS 700 mV, Vcm = 0.9 V 0x34 = HSDS 800 mV, Vcm = 1 V

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 31, 2025 to November 30, 2025 (from Revision * (March 2025) to Revision A (November 2025)) **Page**

- Updated Device Registers section.. 3