Programmer's Guide

LMX1204 Register Map

ABSTRACT

The LMX1204 Register Map defines the register set for the LMX1204. Named registers are documented and described in detail, including valid states. Some registers are marked as reserved, but require value updates after device POR or after the RESET bit is toggled. When generating configurations in TICS Pro Software, any exported registers by default will include the required value updates to reserved registers as well. For applications where the register values are defined manually, carefully observe the required updates.

Table of Contents

Trademarks

1 LMX1204 Registers

Table 1-1 lists the memory-mapped registers for the Device registers. All register addresses not listed in Table 1-1 are undocumented addresses and can be considered reserved. Writing to undocumented addresses can prevent the device from working as intended. Unless specifically instructed by TI, do not write to undocumented addresses.

The recommended initial programming sequence starts by writing R0 with RESET = 0x1, followed by writing all registers required for the desired configuration in descending order (largest to smallest address). Registers related to specific features can be skipped if those features are not used, or if desired values do not differ from reset values. Several registers are documented only to allow readback of certain multiplier values, and can be omitted from initial programming or ignored entirely if the multiplier is not used.

Table 1-1. LMX1204 Registers

Address	Acronym	Features Requiring This Register	Section
0x0	R0	Powerdown, Reset, Multiplier Mode Calibration	Go
0x2	R2	Multiplier Mode (State Machine Clock)	Go
0x3	R3	Multiplier Mode (State Machine Clock), Output Enables	Go
0x4	R4	Output Enables, CLKOUT Power	Go
0x5	R5	CLKOUT Power, SYSREFOUT Power	Go
0x6	R6	LOGICLK Enable, SYSREFOUT Power/VCM	Go
0x7	R7	LOGICLK and LOGISYSREF	Go
0x8	R8	LOGICLK and LOGISYSREF	Go
0x9	R9	LOGICLK Divider, SYNC, SYSREFREQ	Go
0xB	R11	SYSREFREQ Windowing (readback)	Go
0xC	R12	SYSREFREQ Windowing (readback)	Go
0xD	R13	SYSREFREQ Windowing	Go
0xE	R14	SYSREFREQ Windowing, SYNC, SYSREF	Go
0xF	R15	SYSREFREQ Windowing, SYNC, SYSREF	Go
0x10	R16	SYSREF	Go
0x11	R17	SYSREF, SYSREFOUT Delay	Go
0x12	R18	SYSREFOUT Delay	Go
0x13	R19	SYSREFOUT Delay	Go
0x14	R20	SYSREFOUT Delay	Go
0x15	R21	SYSREFOUT Delay	Go
0x16	R22	SYSREFOUT Delay	Go
0x17	R23	Temperature Sensor, MUXOUT, SYSREFOUT Delay	Go
0x18	R24	Temperature Sensor	Go
0x19	R25	Multiplier Mode, Divider Mode	Go
0x1C	R28	Multiplier Mode (optional, partial assist calibration)	Go
0x1D	R29	Multiplier Mode (optional, partial assist calibration)	Go
0x21	R33	Multiplier Mode (RESERVED, must write in multiplier mode)	Go
0x22	R34	Multiplier Mode (RESERVED, must write in multiplier mode)	Go
0x41	R65	Multiplier Mode (read-only, optional, for partial assist calibration)	Go
0x43	R67	Multiplier Mode (RESERVED, must write in multiplier mode)	Go
0x48	R72	SYSREF	Go
0x4B	R75	Multiplier Mode (read-only, optional, lock detect)	Go
0x4F	R79	LOGICLK Divider (RESERVED, optional, for divider bypass)	Go
0x56	R86	MUXOUT (RESERVED, optional, for tri-state)	Go
0x5A	R90	LOGICLK Divider (RESERVED, optional, for divider bypass)	Go

Complex bit access types are encoded to fit into small table cells. Device Access Type Codes shows the codes that are used for access types in this section.

Table 1-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

1.1 R0 Register (Offset = 0x0) [Reset = 0x0000]

R0 is shown in Table 1-3.

Return to the Summary Table.

Table 1-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED	R	0x0000	Reserved (not used).
2	POWERDOWN	R/W	0x0	Sets the device in a low-power state. The states of other registers are maintained.
1	RESERVED	R/W	0x0	Reserved. If this register is written, set this bit to 0x0.
0	RESET	R/W	0x0	Soft Reset. Resets the entire logic and registers (equivalent to power-on reset). Self-clearing on next register write.

1.2 R2 Register (Offset = 0x2) [Reset = 0x0223]

R2 is shown in Table 1-4.

Return to the Summary Table.

Table 1-4. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R	0x00	Reserved (not used).
10	RESERVED	R/W	0x0	Reserved. If this register is written, set this bit to 0x0.
9:6	SMCLK_DIV_PRE	R/W	0x8	Sets pre-divider for state machine clock. The state machine clock is divided from CLKIN. The output of the pre-divider must be ≤ 1600 MHz. Values other than those listed below are reserved. 0x2 = ÷2 0x4 = ÷4 0x8 = ÷8
5	SMCLK_EN	R/W	0x1	Enables the state machine clock generator. Only required to calibrate the multiplier, and for multiplier lock detect (including on MUXOUT pin). If the multiplier is not used, or if the multiplier lock detect feature is not used, the state machine clock generator can be disabled to minimize crosstalk.
4:0	RESERVED	R/W	0x03	Reserved. If this register is written, set these bits to 0x03.

1.3 R3 Register (Offset = 0x3) [Reset = 0xFF86]

R3 is shown in Table 1-5.

Return to the Summary Table.

Table 1-5. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CH3_EN	R/W	0x1	Enables CH3 (CLKOUT3, SYSREFOUT3). Setting this bit to 0x0 completely disables all CH3 circuitry, overriding the state of other powerdown/enable bits.
14	CH2_EN	R/W	0x1	Enables CH2 (CLKOUT2, SYSREFOUT2). Setting this bit to 0x0 completely disables all CH2 circuitry, overriding the state of other powerdown/enable bits.
13	CH1_EN	R/W	0x1	Enables CH1 (CLKOUT1, SYSREFOUT1). Setting this bit to 0x0 completely disables all CH1 circuitry, overriding the state of other powerdown/enable bits.
12	CH0_EN	R/W	0x1	Enables CH0 (CLKOUT0, SYSREFOUT0). Setting this bit to 0x0 completely disables all CH0 circuitry, overriding the state of other powerdown/enable bits.
11	LOGIC_MUTE_CAL	R/W	0x1	Mutes LOGIC outputs (LOGICLKOUT, LOGISYSREFOUT) during multiplier calibration.
10	CH3_MUTE_CAL	R/W	0x1	Mutes CH3 (CLKOUT3, SYSREFOUT3) during multiplier calibration.
9	CH2_MUTE_CAL	R/W	0x1	Mutes CH2 (CLKOUT2, SYSREFOUT2) during multiplier calibration.
8	CH1_MUTE_CAL	R/W	0x1	Mutes CH1 (CLKOUT1, SYSREFOUT1) during multiplier calibration.
7	CH0_MUTE_CAL	R/W	0x1	Mutes CH0 (CLKOUT0, SYSREFOUT0) during multiplier calibration.
6:3	RESERVED	R/W	0x0	Reserved. If this register is written, set these bits to 0x0.
2:0	SMCLK_DIV	R/W	0x6	Sets state machine clock divider. Further divides the output of the state machine clock pre-divider. Input frequency from SMCLK_DIV_PRE must be ≤ 1600 MHz. Output frequency must be ≤ 30 MHz. Divide value is 2^{SMCLK_DIV}. 0x0 = ÷1 0x1 = ÷2 0x2 = ÷4 0x3 = ÷8 0x4 = ÷16 0x5 = ÷32 0x6 = ÷64 0x7 = ÷128

1.4 R4 Register (Offset = 0x4) [Reset = 0x360F]

R4 is shown in Table 1-6.

Return to the Summary Table.

Table 1-6. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved (not used).
13:11	CLKOUT1_PWR	R/W	0x6	Sets the output power of CLKOUT1. Larger values correspond to higher output power.
10:8	CLKOUT0_PWR	R/W	0x6	Sets the output power of CLKOUT0. Larger values correspond to higher output power.
7	SYSREFOUT3_EN	R/W	0x0	Enables SYSREFOUT3 output buffer.
6	SYSREFOUT2_EN	R/W	0x0	Enables SYSREFOUT2 output buffer.
5	SYSREFOUT1_EN	R/W	0x0	Enables SYSREFOUT1 output buffer.
4	SYSREFOUT0_EN	R/W	0x0	Enables SYSREFOUT0 output buffer.
3	CLKOUT3_EN	R/W	0x1	Enables CLKOUT3 output buffer.
2	CLKOUT2_EN	R/W	0x1	Enables CLKOUT2 output buffer.
1	CLKOUT1_EN	R/W	0x1	Enables CLKOUT1 output buffer.
0	CLKOUT0_EN	R/W	0x1	Enables CLKOUT0 output buffer.

1.5 R5 Register (Offset = 0x5) [Reset = 0x4936]

R5 is shown in Table 1-7.

Return to the Summary Table.

Table 1-7. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved (not used).
14:12	SYSREFOUT2_PWR	R/W	0x4	Sets the output power of SYSREFOUT2. Larger values correspond to higher output power. SYSREFOUT2_VCM must be set properly to bring the output common-mode voltage within permissible limits. See also R6 Register.
11:9	SYSREFOUT1_PWR	R/W	0x4	Sets the output power of SYSREFOUT1. Larger values correspond to higher output power. SYSREFOUT1_VCM must be set properly to bring the output common-mode voltage within permissible limits. See also R6 Register.
8:6	SYSREFOUT0_PWR	R/W	0x4	Sets the output power of SYSREFOUT0. Larger values correspond to higher output power. SYSREFOUT0_VCM must be set properly to bring the output common-mode voltage within permissible limits. See also R6 Register.
5:3	CLKOUT3_PWR	R/W	0x6	Sets the output power of CLKOUT3. Larger values correspond to higher output power.
2:0	CLKOUT2_PWR	R/W	0x6	Sets the output power of CLKOUT2. Larger values correspond to higher output power.

1.6 R6 Register (Offset = 0x6) [Reset = 0x36D6]

R6 is shown in Table 1-8.

Return to the Summary Table.

Table 1-8. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LOGICLKOUT_EN	R/W	0x0	Enables the LOGICLKOUT output buffer.
14:12	SYSREFOUT3_VCM	R/W	0x3	Sets the output common mode of SYSREFOUT3. SYSREFOUT3_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
11:9	SYSREFOUT2_VCM	R/W	0x3	Sets the output common mode of SYSREFOUT2. SYSREFOUT2_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits. See also R5 Register.
8:6	SYSREFOUT1_VCM	R/W	0x3	Sets the output common mode of SYSREFOUT1. SYSREFOUT1_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits. See also R5 Register.
5:3	SYSREFOUT0_VCM	R/W	0x3	Sets the output common mode of SYSREFOUT0. SYSREFOUT0_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits. See also R5 Register.
2:0	SYSREFOUT3_PWR	R/W	0x4	Sets the output power of SYSREFOUT3. Larger values correspond to higher output power. SYSREFOUT3_VCM must be set properly to bring the output common-mode voltage within permissible limits.

1.7 R7 Register (Offset = 0x7) [Reset = 0x0000]

R7 is shown in Table 1-9.

Return to the Summary Table.

Table 1-9. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved (not used).
14:13	LOGISYSREFOUT_VCM	R/W	0x0	Sets the output common mode of LOGISYSREFOUT in LVDS format. Other output formats (CML, LVPECL) ignore this field. 0x0 = 1.2 V 0x1 = 1.1 V 0x2 = 1.0 V 0x3 = 0.9 V
12:11	LOGICLKOUT_VCM	R/W	0x0	Sets the output common mode of LOGICLKOUT in LVDS format. Other output formats (CML, LVPECL) ignore this field. 0x0 = 1.2 V 0x1 = 1.1 V 0x2 = 1.0 V 0x3 = 0.9 V
10:9	LOGISYSREFOUT_PREDRV_PWR	R/W	0x0	Sets the output power of the LOGISYSREFOUT pre-driver. Larger values correspond to higher output power. Default value is sufficient for typical use.
8:7	LOGICLKOUT_PREDRV_PWR	R/W	0x0	Sets the output power of the LOGICLKOUT pre-driver. Larger values correspond to higher output power. Default value is sufficient for typical use.
6:4	LOGISYSREFOUT_PWR	R/W	0x0	Sets the output power of LOGISYSREFOUT in CML format. Larger values correspond to higher output power. Other output formats (LVDS, LVPECL) ignore this field. Valid range is 0x0 to 0x3.
3:1	LOGICLKOUT_PWR	R/W	0x0	Sets the output power of LOGICLKOUT in CML format. Larger values correspond to higher output power. Other output formats (LVDS, LVPECL) ignore this field. Valid range is 0x0 to 0x3.
0	LOGISYSREFOUT_EN	R/W	0x0	Enables LOGISYSREFOUT output buffer.

1.8 R8 Register (Offset = 0x8) [Reset = 0x0120]

R8 is shown in Table 1-10.

Return to the Summary Table.

Table 1-10. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R	0x00	Reserved (not used).
8:6	LOGICLK_DIV_PRE	R/W	0x4	Sets pre-divider value for logic clock divider. Output of the pre-divider must be ≤ 3.2 GHz. Values other than those listed below are reserved. 0x1 = ÷1 0x2 = ÷2 0x4 = ÷4
5	RESERVED	R/W	0x1	Reserved. If this register is written, set this bit to 0x1.
4	LOGIC_EN	R/W	0x0	Enables LOGICLK subsystem (LOGICLKOUT, LOGISYSREFOUT). Setting this bit to 0x0 completely disables all LOGICLKOUT and LOGISYSREFOUT circuitry, overriding the state of other powerdown/enable bits.
3:2	LOGISYSREFOUT_FMT	R/W	0x0	Selects the output driver format of the LOGISYSREFOUT output. LVDS allows for common mode control with LOGISYSREFOUT_VCM field. CML allows for output power control with LOGISYSREFOUT_PWR field. CML format requires external 50-Ω pull-up resistors. LVPECL requires external 220-Ω emitter resistors to GND when AC-coupled, or 50-Ω to VCC - 2 V (0.5 V) when DC-coupled. See also R7 Register. 0x0 = LVDS 0x1 = LVPECL 0x2 = CML 0x3 = Reserved
1:0	LOGICLKOUT_FMT	R/W	0x0	Selects the output driver format of the LOGICLKOUT output. LVDS allows for common mode control with LOGICLKOUT_VCM field. CML allows for output power control with LOGICLKOUT_PWR field. CML format requires external 50-Ω pull-up resistors. LVPECL requires external 220-Ω emitter resistors to GND when AC-coupled, or 50-Ω to VCC - 2 V (0.5 V) when DC-coupled. See also R7 Register. 0x0 = LVDS 0x1 = LVPECL 0x2 = CML 0x3 = Reserved

1.9 R9 Register (Offset = 0x9) [Reset = 0x001E]

R9 is shown in Table 1-11.

Return to the Summary Table.

Table 1-11. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SYSREFREQ_VCM	R/W	0x0	Sets the internal DC Bias for the SYSREFREQ pins. Bias must be enabled for AC-coupled inputs; but can be enabled and overdriven, or disabled, for DC-coupled inputs. SYSREFREQ DC pin voltage must be in the range of 0.7 V to VCC, including minimum and maximum signal swing. 0x0 = 1.3 V 0x1 = 1.1 V 0x2 = 1.5 V 0x3 = Disabled (DC-coupled only)
13	SYNC_EN	R/W	0x0	Enables synchronization path for the dividers and allows the clock position capture circuitry to be enabled. Used for multi-device synchronization. Redundant if SYSREF_EN = 0x1.
12	LOGICLK_DIV_PD	R/W	0x0	Disables the LOGICLK divider. LOGICLK pre-divider remains enabled. Used to reduce current consumption when bypassing the LOGICLK divider. When LOGICLK_DIV_PRE = 0x2 or 0x4, this bit must be set to 0x0.
11	LOGICLK_DIV_BYPASS	R/W	0x0	Bypasses the LOGICLK divider, deriving LOGICLK output directly from the pre-divider. Used to achieve divide-by-1 when LOGICLK_DIV_PRE = 0x1. When LOGICLK_DIV_PRE = 0x2 or 0x4, this bit must be set to 0x0. When LOGICLK_DIV_BYPASS = 0x1, set R90[6:5] = 0x3 and R79[9:8] = 0x0. When LOGICLK_DIV_BYPASS = 0x0, if R90[6:5] = 0x3 due to previous user setting, set R90[6:5] = 0x0. When LOGICLK_DIV_BYPASS = 0x1, the LOGICLKOUT frequency must be ≤ 800 MHz to avoid amplitude degradation. See also R79 Register and R90 Register.
10	RESERVED	R/W	0x0	Reserved. If this register is written, set this bit to 0x0.
9:0	LOGICLK_DIV	R/W	0x1E	Sets LOGICLK divider value. Maximum input frequency from LOGICLK_DIV_PRE must be ≤ 3200 MHz. The maximum LOGICLKOUT frequency must be ≤ 800 MHz to avoid amplitude degradation. 0x0: Reserved 0x1: Reserved 0x2: ÷2 0x3: ÷3 ... 0x1FF: ÷1023

1.10 R11 Register (Offset = 0xB) [Reset = 0xFFFF]

R11 is shown in Table 1-12.

Return to the Summary Table.

Table 1-12. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	rb_CLKPOS[15:0]	R	0xFFFF	Stores a snapshot of the CLKIN signal rising edge positions relative to a SYSREFREQ rising edge, with the snapshot starting from the LSB and ending at the MSB. Each bit represents a sample of the CLKIN signal, separated by a delay determined by the SYSREFREQ_DELAY_STEPSIZE field. The first and last bits of rb_CLKPOS are always set, indicating uncertainty at the capture window boundary conditions. CLKIN rising edges are represented by every sequence of two set bits from LSB to MSB, including bits at the boundary conditions. The position of the CLKIN rising edges in the snapshot, along with the CLKIN signal period and the delay step size, can be used to compute the value of SYSREFREQ_DELAY_STEP which maximizes setup and hold times for SYNC signals on the SYSREFREQ pins. See also R12 Register, R13 Register, R14 Register, and R15 Register.

1.11 R12 Register (Offset = 0xC) [Reset = 0xFFFF]

R12 is shown in Table 1-13.

Return to the Summary Table.

Table 1-13. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	rb_CLKPOS[31:16]	R	0xFFFF	MSBs of rb_CLKPOS field. See also R11 Register, R13 Register, R14 Register, and R15 Register.

1.12 R13 Register (Offset = 0xD) [Reset = 0x0003]

R13 is shown in Table 1-14.

Return to the Summary Table.

Table 1-14. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED	R	0x0000	Reserved (not used).
1:0	SYSREFREQ_DELAY_STEPSIZE	R/W	0x3	Sets the step size of the delay element used in the SYSREFREQ path, both for SYSREFREQ input delay and for clock position captures. The recommended frequency range for each step size creates the maximum number of usable steps for a given CLKIN frequency. The ranges include some overlap to account for process and temperature variations. If the CLKIN frequency is covered by an overlapping span, larger delay step sizes improve the likelihood of detecting a CLKIN rising edge during a clock position capture. However, since larger values include more delay steps, larger step sizes have greater total delay variation across PVT relative to smaller step sizes. See also R11 Register, R12 Register, R14 Register, and R15 Register. 0x0 = 28 ps (1.4 GHz to 2.7 GHz) 0x1 = 15 ps (2.4 GHz to 4.7 GHz) 0x2 = 11 ps (3.1 GHz to 5.7 GHz) 0x3 = 8 ps (4.5 GHz to 12.8 GHz)

1.13 R14 Register (Offset = 0xE) [Reset = 0x0002]

R14 is shown in Table 1-15.

Return to the Summary Table.

Table 1-15. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R/W	0x00	Reserved. If this register is written, set these bits to 0x00.
8	SYNC_MUTE_PD	R/W	0x0	Removes the mute condition on the SYSREFOUT and LOGISYSREFOUT pins during SYNC mode (SYSREFREQ_MODE = 0x0). Since the SYNC operation also resets the SYSREF dividers, the mute condition is usually desirable, and this bit can be left at the default value.
7:3	RESERVED	R/W	0x00	Reserved. If this register is written, set these bits to 0x00.
2	CLKPOS_CAPTURE_EN	R/W	0x0	Enables the windowing circuit which captures the clock position in the rb_CLKPOS registers with respect to a SYSREF edge. The windowing circuit must be cleared by toggling SYSREFREQ_CLR high then low before a clock position capture. The first rising edge on the SYSREFREQ pins after clearing the windowing circuit triggers the capture. The capture circuitry greatly increases supply current, and does not need to be enabled to delay the SYSREFREQ signal in SYNC or SYSREF modes. Once the desired value of SYSREFREQ_DELAY_STEP is determined, set this bit to 0x0 to minimize current consumption. If SYNC_EN = 0x0 and SYSREF_EN = 0x0, the value of this bit is ignored, and the windowing circuit is disabled. See also R11 Register, R12 Register, R13 Register, and R15 Register.
1	SYSREFREQ_MODE	R/W	0x1	Selects the function of the SYSREFREQ pins. 0x0 = SYNC Pin 0x1 = SYSREFREQ Pin
0	SYSREFREQ_LATCH	R/W	0x0	Latches the internal SYSREFREQ state to logic high on the first rising edge of the SYSREFREQ pins. This latch can be cleared by setting SYSREFREQ_CLR to 0x1, or bypassed by setting SYSREFREQ_LATCH to 0x0. See also R15 Register.

1.14 R15 Register (Offset = 0xF) [Reset = 0x0901]

R15 is shown in Table 1-16.

Return to the Summary Table.

Table 1-16. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0x0	Reserved (not used).
11:10	SYSREF_DIV_PRE	R/W	0x2	Sets the SYSREF pre-divider. Maximum output frequency must be ≤ 3.2 GHz. 0x0 = ÷1 0x1 = ÷2 0x2 = ÷4 0x3 = Reserved
9:8	RESERVED	R/W	0x1	Reserved. If this register is written, set these bits to 0x1.
7	SYSREF_EN	R/W	0x0	Enables SYSREF subsystem (and SYNC subsystem when SYSREFREQ_MODE = 0x0). Setting this bit to 0x0 completely disables all SYNC, SYSREF, and clock position capture circuitry, overriding the state of other powerdown/enable bits *except* SYNC_EN. If SYNC_EN = 0x1, the SYNC path and clock position capture circuitry are still enabled, regardless of the state of SYSREF_EN.
6:1	SYSREFREQ_DELAY_STEP	R/W	0x0	Sets the delay line step for the external SYSREFREQ signal. Each delay line step delays the SYSREFREQ signal by an amount equal to SYSREFREQ_DELAY_STEP x SYSREFREQ_DELAY_STEPSIZE. In SYNC mode, the value for this field can be determined based on the rb_CLKPOS value to satisfy the internal setup and hold time of the SYNC signal with respect to the CLKIN signal. In SYSREF Repeater Mode, the value for this field can be used as a coarse global delay. Values greater than 0x3F are invalid. Since larger values include more delay steps, larger values have greater total step size variation across PVT relative to smaller values. Refer to the data sheet or the device TICS Pro profile for detailed description of the delay step computation procedure. See also R11 Register, R12 Register, R13 Register, and R14 Register.
0	SYSREFREQ_CLR	R/W	0x1	Clears SYSREFREQ_LATCH, which resets the SYSREFREQ input latch, the internal divider synchronization retimers, and the clock position capture flip-flops comprising rb_CLKPOS. When set, holds the internal SYSREFREQ signal low in all modes except SYSREF repeater mode, overriding the state of SYSREFREQ_SPI. This bit must be set and cleared once before the SYNC or clock position capture operations are performed. See also R14 Register.

1.15 R16 Register (Offset = 0x10) [Reset = 0x1003]

R16 is shown in Table 1-17.

Return to the Summary Table.

Table 1-17. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	SYSREF_PULSE_COUNT	R/W	0x1	Programs the number of pulses generated in pulser mode. The pulser is a counter gating the SYSREF divider; consequently, the pulse duration and frequency are equal to the duty cycle and frequency of the SYSREF divider output, respectively. 0x0: Reserved 0x1: 1 pulse 0x2: 2 pulses ... 0xF: 15 pulses
11:0	SYSREF_DIV	R/W	0x3	Sets the SYSREF divider. Maximum input frequency from SYSREF_DIV_PRE must be ≤ 3200 MHz. Maximum output frequency must be ≤ 100 MHz. Odd divides (with duty cycle != 50%) are only allowed when the delay generators are bypassed. See also R72 Register. 0x0: Reserved 0x1: Reserved 0x2: ÷2 0x3: ÷3 ... 0xFFF: ÷4095

1.16 R17 Register (Offset = 0x11) [Reset = 0x07F0]

R17 is shown in Table 1-18.

Return to the Summary Table.

Table 1-18. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R	0x0	Reserved (not used).
10:4	SYSREFOUT0_DELAY_I	R/W	0x7F	Sets the delay step for the SYSREFOUT0 delay generator. Must satisfy SYSREFOUT0_DELAY_I + SYSREFOUT0_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R18 Register and R22 Register.
3:2	SYSREFOUT0_DELAY_PHASE	R/W	0x0	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT0 delay generator retimer. Consult the data sheet for configuration instructions. See also R18 Register and R22 Register. 0x0 = $\overline{\text{ICLK}}$ 0x1 = $\overline{\text{QCLK}}$ 0x2 = QCLK 0x3 = ICLK
1:0	SYSREF_MODE	R/W	0x0	Controls how the SYSREF signal is generated or repeated. See also SYSREF_DELAY_BYPASS in R79 Register for additional configuration options. 0x0 = Continuous (Generator Mode) 0x1 = Pulser (Generator Mode) 0x2 = Repeater (Repeater Mode) 0x3 = Reserved

1.17 R18 Register (Offset = 0x12) [Reset = 0xFE00]

R18 is shown in Table 1-19.

Return to the Summary Table.

Table 1-19. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	SYSREFOUT1_DELAY_I	R/W	0x7F	Sets the delay step for the SYSREFOUT1 delay generator. Must satisfy SYSREFOUT1_DELAY_I + SYSREFOUT1_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R19 Register and R22 Register.
8:7	SYSREFOUT1_DELAY_PHASE	R/W	0x0	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT1 delay generator retimer. Consult the data sheet for configuration instructions. See also R19 Register and R22 Register. 0x0 = $\overline{\text{ICLK}}$ 0x1 = $\overline{\text{QCLK}}$ 0x2 = QCLK 0x3 = ICLK
6:0	SYSREFOUT0_DELAY_Q	R/W	0x0	Sets the delay step for the SYSREFOUT0 delay generator. Must satisfy SYSREFOUT0_DELAY_I + SYSREFOUT0_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R17 Register and R22 Register.

1.18 R19 Register (Offset = 0x13) [Reset = 0xFE00]

R19 is shown in Table 1-20.

Return to the Summary Table.

Table 1-20. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	SYSREFOUT2_DELAY_I	R/W	0x7F	Sets the delay step for the SYSREFOUT2 delay generator. Must satisfy SYSREFOUT2_DELAY_I + SYSREFOUT2_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R20 Register and R23 Register.
8:7	SYSREFOUT2_DELAY_PHASE	R/W	0x0	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT2 delay generator retimer. Consult the data sheet for configuration instructions. See also R20 Register and R23 Register. 0x0 = $\overline{\text{ICLK}}$ 0x1 = $\overline{\text{QCLK}}$ 0x2 = QCLK 0x3 = ICLK
6:0	SYSREFOUT1_DELAY_Q	R/W	0x0	Sets the delay step for the SYSREFOUT1 delay generator. Must satisfy SYSREFOUT1_DELAY_I + SYSREFOUT1_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R18 Register and R22 Register.

1.19 R20 Register (Offset = 0x14) [Reset = 0xFE00]

R20 is shown in Table 1-21.

Return to the Summary Table.

Table 1-21. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	SYSREFOUT3_DELAY_I	R/W	0x7F	Sets the delay step for the SYSREFOUT3 delay generator. Must satisfy SYSREFOUT3_DELAY_I + SYSREFOUT3_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R21 Register and R23 Register.
8:7	SYSREFOUT3_DELAY_PHASE	R/W	0x0	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT3 delay generator retimer. Consult the data sheet for configuration instructions. See also R21 Register and R23 Register. 0x0 = $\overline{\text{ICLK}}$ 0x1 = $\overline{\text{QCLK}}$ 0x2 = QCLK 0x3 = ICLK
6:0	SYSREFOUT2_DELAY_Q	R/W	0x0	Sets the delay step for the SYSREFOUT2 delay generator. Must satisfy SYSREFOUT2_DELAY_I + SYSREFOUT2_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R19 Register and R23 Register.

1.20 R21 Register (Offset = 0x15) [Reset = 0xFE00]

R21 is shown in Table 1-22.

Return to the Summary Table.

Table 1-22. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	LOGISYSREFOUT_DELAY_I	R/W	0x7F	Sets the delay step for the LOGISYSREFOUT delay generator. Must satisfy LOGISYSREFOUT_DELAY_I + LOGISYSREFOUT_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R22 Register and R23 Register.
8:7	LOGISYSREFOUT_DELAY_PHASE	R/W	0x0	Sets the quadrature phase of the interpolator clock used for the LOGISYSREFOUT delay generator retimer. Consult the data sheet for configuration instructions. See also R22 Register and R23 Register. 0x0 = $\overline{\text{ICLK}}$ 0x1 = $\overline{\text{QCLK}}$ 0x2 = QCLK 0x3 = ICLK
6:0	SYSREFOUT3_DELAY_Q	R/W	0x0	Sets the delay step for the SYSREFOUT3 delay generator. Must satisfy SYSREFOUT3_DELAY_I + SYSREFOUT3_DELAY_Q = 0x7F. Consult the data sheet for configuration instructions. See also R20 Register and R23 Register.

1.21 R22 Register (Offset = 0x16) [Reset = 0x0800]

R22 is shown in Table 1-23.

Return to the Summary Table.

Table 1-23. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SYSREFOUT1_DELAY_SCALE	R/W	0x0	Sets the frequency range of the SYSREFOUT1 delay generator. Set according to $f_{INTERPOLATOR}$ frequency. Consult the data sheet for configuration instructions. See also R18 Register and R19 Register. 0x0 = 400 MHz to 800 MHz 0x1 = 200 MHz to 400 MHz 0x2 = 150 MHz to 200 MHz 0x3 = Reserved
13:12	SYSREFOUT0_DELAY_SCALE	R/W	0x0	Sets the frequency range of the SYSREFOUT0 delay generator. Set according to $f_{INTERPOLATOR}$ frequency. Consult the data sheet for configuration instructions. See also R17 Register and R18 Register. 0x0 = 400 MHz to 800 MHz 0x1 = 200 MHz to 400 MHz 0x2 = 150 MHz to 200 MHz 0x3 = Reserved
11:9	SYSREF_DELAY_DIV	R/W	0x4	Sets the delay generator clock division, determining $f_{INTERPOLATOR}$ and the delay generator resolution. Values other than those listed below are reserved. See also R23 Register. 0x0 = ÷2 (≤ 1.6 GHz) 0x1 = ÷4 (1.6 GHz to 3.2 GHz) 0x2 = ÷8 (3.2 GHz to 6.4 GHz) 0x4 = ÷16 (6.4 GHz to 12.8 GHz)
8:7	RESERVED	R/W	0x0	Reserved. If this register is written, set these bits to 0x0.
6:0	LOGISYSREFOUT_DELAY_Q	R/W	0x0	Sets the delay step for the LOGISYSREFOUT delay generator. Must satisfy LOGISYSREFOUT_DELAY_I + LOGISYSREFOUT_DELAY_Q = 0x7F. See also R21 Register and R23 Register.

1.22 R23 Register (Offset = 0x17) [Reset = 0x4000]

R23 is shown in Table 1-24.

Return to the Summary Table.

Table 1-24. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	EN_TEMPSENSE	R/W	0x0	Enables the on-die temperature sensor. Temperature sensor counter (EN_TS_COUNT) must also be enabled for readback. See also R24 Register.
14	RESERVED	R/W	0x1	Reserved. If this register is written, set this bit to 0x1.
13	MUXOUT_EN	R/W	0x0	Enables or tri-states the MUXOUT pin driver. See also R86 Register. 0x0 = Tri-State 0x1 = Push-Pull
12:7	RESERVED	R/W	0x00	Reserved. If this register is written, set these bits to 0x00.
6	MUXOUT_SEL	R/W	0x0	Selects MUXOUT pin function. 0x0 = Lock Detect (Multiplier Only) 0x1 = SDO (SPI readback)
5:4	LOGISYSREFOUT_DELAY_SCALE	R/W	0x0	Sets the frequency range of the LOGISYSREFOUT delay generator. Set according to $f_{INTERPOLATOR}$ frequency. Consult the data sheet for configuration instructions. See also R21 Register and R22 Register. 0x0 = 400 MHz to 800 MHz 0x1 = 200 MHz to 400 MHz 0x2 = 150 MHz to 200 MHz 0x3 = Reserved
3:2	SYSREFOUT3_DELAY_SCALE	R/W	0x0	Sets the frequency range of the SYSREFOUT3 delay generator. Set according to $f_{INTERPOLATOR}$ frequency. Consult the data sheet for configuration instructions. See also R20 Register, R21 Register, and R22 Register. 0x0 = 400 MHz to 800 MHz 0x1 = 200 MHz to 400 MHz 0x2 = 150 MHz to 200 MHz 0x3 = Reserved
1:0	SYSREFOUT2_DELAY_SCALE	R/W	0x0	Sets the frequency range of the SYSREFOUT2 delay generator. Set according to $f_{INTERPOLATOR}$ frequency. Consult the data sheet for configuration instructions. See also R19 Register, R20 Register, and R22 Register. 0x0 = 400 MHz to 800 MHz 0x1 = 200 MHz to 400 MHz 0x2 = 150 MHz to 200 MHz 0x3 = Reserved

1.23 R24 Register (Offset = 0x18) [Reset = 0x0FFE]

R24 is shown in Table 1-25.

Return to the Summary Table.

Table 1-25. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved (not used).
13:12	RESERVED	R/W	0x0	Reserved. If this register is written, set these bits to 0x0.
11:1	rb_TEMPSENSE	R	0x7FF	Output of on-die temperature sensor. Readback code can be converted to junction temperature (in °C) according to the following equation: T_J = 0.65 * rb_TEMPSENSE - 351
0	EN_TS_COUNT	R/W	0x0	Enables temperature sensor counter. Temperature sensor (EN_TEMPSENSE) must be enabled for accurate data. See also R23 Register.

1.24 R25 Register (Offset = 0x19) [Reset = 0x0211]

R25 is shown in Table 1-26.

Return to the Summary Table.

Table 1-26. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED	R/W	0x004	Reserved. If this register is written, set these bits to 0x004.
6	CLK_DIV_RST	R/W	0x0	Resets the main clock divider. If the clock divider value is changed during operation, set this bit high then low after setting the new divider value. Synchronizing the device with the SYSREFREQ pins in SYSREFREQ_MODE = 0x0 and SYNC_EN = 0x1 also resets the main clock divider. This bit has no effect when outside of Divider Mode.
5:3	CLK_DIV CLK_MULT	R/W	0x2	CLK_DIV and CLK_MULT are aliases for the same field. When CLK_MUX = 0x2 (Divider Mode), sets the clock divider equal to CLK_DIV + 1. Valid range is 0x1 to 0x7. Setting CLK_DIV = 0x0 disables the main clock divider and reverts to buffer mode. When CLK_MUX = 0x3 (Multiplier Mode), sets the multiplier equal to CLK_MULT. Valid range is 0x1 to 0x4. Setting CLK_MULT to an invalid value disables the multiplier and reverts to buffer mode. When CLK_MUX = 0x1 (buffer mode), this field is ignored.
2:0	CLK_MUX	R/W	0x1	Selects the function of the device. Multiplier Mode requires writing several other registers (R33, R34, and R67) to values differing from POR defaults, as well as configuring the state machine clock (R2 and R3), before multiplier calibration. Writing any value to R0 (as long as POWERDOWN = 0x0 and RESET = 0x0) triggers a multiplier calibration. Values other than those listed below are reserved. 0x1 = Buffer Mode 0x2 = Divider Mode 0x3 = Multiplier Mode

1.25 R28 Register (Offset = 0x1C) [Reset = 0x0A08]

R28 is shown in Table 1-27.

Return to the Summary Table.

Table 1-27. R28 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved (not used).
12	FORCE_VCO	R/W	0x0	Forces the multiplier PLL's VCO to the value selected by VCO_SEL. Not required for Multiplier Mode programming, but can optionally be used to reduce calibration time.
11:9	VCO_SEL	R/W	0x5	User specified start VCO for multiplier PLL. When FORCE_VCO = 0x0, multiplier calibration starts from the VCO set by this field. When FORCE_VCO = 0x1, this field sets the VCO core used by the multiplier. Not required for Multiplier Mode programming, but can optionally be used to reduce calibration time.
8:0	RESERVED	R/W	0x008	Reserved. If this register is written, set these bits to 0x008.

1.26 R29 Register (Offset = 0x1D) [Reset = 0x05FF]

R29 is shown in Table 1-28.

Return to the Summary Table.

Table 1-28. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved (not used).
12:8	RESERVED	R/W	0x5	Reserved. If this register is written, set these bits to 0x05.
7:0	CAPCTRL	R/W	0xFF	Sets the starting value for the VCO tuning capacitance during multiplier calibration. Not required for Multiplier Mode programming, but can optionally be used to reduce calibration time.

1.27 R33 Register (Offset = 0x21) [Reset = 0x7777]

R33 is shown in Table 1-29.

Return to the Summary Table.

Table 1-29. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	0x7777	Reserved. If the Multiplier Mode is used, set to 0x5666 before calibration. Otherwise, writing this register can be skipped.

1.28 R34 Register (Offset = 0x22) [Reset = 0x0000]

R34 is shown in Table 1-30.

Return to the Summary Table.

Table 1-30. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved (not used).
13:0	RESERVED	R/W	0x0000	Reserved. If the Multiplier Mode is used, set to 0x04C5 before calibration. Otherwise, writing this register can be skipped.

1.29 R65 Register (Offset = 0x41) [Reset = 0x45F0]

R65 is shown in Table 1-31.

Return to the Summary Table.

Table 1-31. R65 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R/W	0x22	Since this register is only used for readback, avoid writing these bits when possible. If this register must be written, set these bits to 0x22. Readback can differ from default and written values.
8:4	rb_VCO_SEL	R	0x1F	Readback multiplier PLL's VCO core selection. Can be optionally used in conjunction with VCO_SEL and FORCE_VCO fields to improve calibration time. 0xF = VCO5 0x17 = VCO4 0x1B = VCO3 0x1D = VCO2 0x1E = VCO1
3:0	RESERVED	R/W	0x0	Since this register is only used for readback, avoid writing these bits when possible. If this register must be written, set these bits to 0x0.

1.30 R67 Register (Offset = 0x43) [Reset = 0x50C8]

R67 is shown in Table 1-32.

Return to the Summary Table.

Table 1-32. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	0x50C8	Reserved. If the Multiplier Mode is used, set to 0x51CB before calibration. Otherwise, writing this register can be skipped.

1.31 R72 Register (Offset = 0x48) [Reset = 0x0000]

R72 is shown in Table 1-33.

Return to the Summary Table.

Table 1-33. R72 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved (not used).
14:4	RESERVED	R/W	0x000	Reserved. Set to 0x000.
3	PULSER_LATCH	R/W	0x0	Latches the pulser input when programmed to 0x1. When this bit is set, external signals on SYSREFREQ pins in pulser mode (SYSREF_MODE = 0x1) can not trigger the pulser more than once, until this bit is cleared. This bit is provided to enable changing SYSREF_MODE in repeater mode without risk of accidentally triggering the pulser.
2	SYSREFREQ_SPI	R/W	0x0	Trigger SYSREFREQ via SPI. Setting this bit emulates the behavior of a logic HIGH at SYSREFREQ pins. External signals on SYSREFREQ pins are ignored while this bit is set.
1:0	SYSREF_DELAY_BYPASS	R/W	0x0	Option to bypass delay generator retiming. Under normal circumstances (SYSREF_DELAY_BYPASS = 0) the delay generator is engaged for continuous or pulser modes (Generator Modes), and bypassed in Repeater Mode. Generally this configuration is desirable: the delay generators rely on a signal generated by the SYSREF_DELAY_DIV from the CLKIN frequency, so the Generator Mode SYSREF signal is always well-aligned to the delay generator; in repeater mode, external signal sources can typically utilize a different delay mechanism. In certain cases, bypassing the delay generator retiming in Generator Mode by setting SYSREF_DELAY_BYPASS = 0x1 can substantially reduce the device current consumption if the SYSREF delay can be compensated at the JESD receiver. In other cases, retiming the SYSREFREQ signal to the delay generators by setting SYSREF_DELAY_BYPASS = 0x2 can improve the accuracy of the SYSREF output phase with respect to the CLKIN phase, or can vary the delay of individual outputs independently, as long as coherent phase relationship exists between the interpolator divider phase and the SYSREFREQ phase. 0x0 = Engage in Generator Mode, Bypass in Repeater Mode 0x1 = Bypass in All Modes 0x2 = Engage in All Modes 0x3 = Reserved

1.32 R75 Register (Offset = 0x4B) [Reset = 0xE716]

R75 is shown in Table 1-34.

Return to the Summary Table.

Table 1-34. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R	0x57	Read-only. Writes to these bits are ignored. Readback can differ from default values.
9:8	rb_LD	R	0x3	Multiplier PLL Lock Detect. Read-only. Field value has no meaning if device is not in Multiplier Mode. 0x0 = Unlocked (VTUNE low) 0x1 = Reserved 0x2 = Locked 0x3 = Unlocked (VTUNE high)
7:4	RESERVED	R	0x1	Read-only. Writes to these bits are ignored. Readback can differ from default values.
3:0	RESERVED	R/W	0x6	Reserved. Since this register is only used for readback, avoid writing these bits when possible. If this register must be written, set to 0x6.

1.33 R79 Register (Offset = 0x4F) [Reset = 0x0104]

R79 is shown in Table 1-35.

Return to the Summary Table.

Table 1-35. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved (not used).
14:0	RESERVED	R/W	0x0104	Reserved. Set to 0x0104 immediately after setting LOGICLK_DIV_BYPASS = 0x1; R90 must also be written immediately afterward. If LOGICLK_DIV_BYPASS is not used or set to 0x0, this register does not need to be written and can be skipped. See also R90 Register.

1.34 R86 Register (Offset = 0x56) [Reset = 0x0000]

R86 is shown in Table 1-36.

Return to the Summary Table.

Table 1-36. R86 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	0x0000	Reserved. This register must be set to 0x0004 to allow MUXOUT_EN to tri-state the MUXOUT pin after SPI readback. If SPI readback is not required, or if tri-state is not required on the MUXOUT pin, writing this register can be skipped, forcing MUXOUT_EN to 0x1 (push-pull mode).

1.35 R90 Register (Offset = 0x5A) [Reset = 0x0000]

R90 is shown in Table 1-37.

Return to the Summary Table.

Table 1-37. R90 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R	0x00	Reserved (not used).
15:0	RESERVED	R/W	0x00	Reserved. Set to 0x60 immediately after setting LOGICLK_DIV_BYPASS = 0x1 and setting R79 = 0x0104. If LOGICLK_DIV_BYPASS is not used or left at the default value, this register does not need to be written and can be skipped. However, if transitioning from LOGICLK_DIV_BYPASS = 0x1 to 0x0, this register must be re-written to 0x00. See also R79 Register.

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2021) to Revision A (September 2022)	Page
• Changed register and field definitions from pre-production to production	2

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265