User's Guide

LMK5C33216EVM User's Guide

ABSTRACT

The LMK5C33216EVM is an evaluation module for the LMK5C33216 Network Clock Generator and Synchronizer. The EVM can be used for device evaluation, compliance testing, and system prototyping.

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Trademarks

1 Introduction

Overview

The LMK5C33216EVM is an evaluation module for the LMK5C33216 Network Clock Generator and Synchronizer. The EVM can be used for device evaluation, compliance testing, and system prototyping. The LMK5C33216 integrates three Analog PLLs (APLL) and three Digital PLLs (DPLL) with programmable loop bandwidth. The EVM includes SMA connectors for clock inputs, oscillator inputs, and clock outputs to interface the device with 50-Ω test equipment.

The onboard TCXO allows the LMK5C33216 to be evaluated in free-running, locked, or holdover mode of operation. The EVM can be configured through the onboard USB microcontroller (MCU) interface using a PC with TI's TICS Pro software graphical user interface (GUI). TICS Pro can be used to program the LMK5C33216 registers.

Features

- LMK5C33216 DUT

What is Included

- LMK5C33216EVM

What is Needed

- Windows PC with TICS Pro Software GUI
- Test Equipment
  - DC power supply (5 V, 2 A)
  - Real-time oscilloscope
  - Source signal analyzer
  - Precision frequency counter
  - Signal generator / reference clock

In Figure 1-1, jumper position is shown by the red markings. Dip switch positions are shown be either a green box (for ON) or red box (for OFF) in the appropriate location.

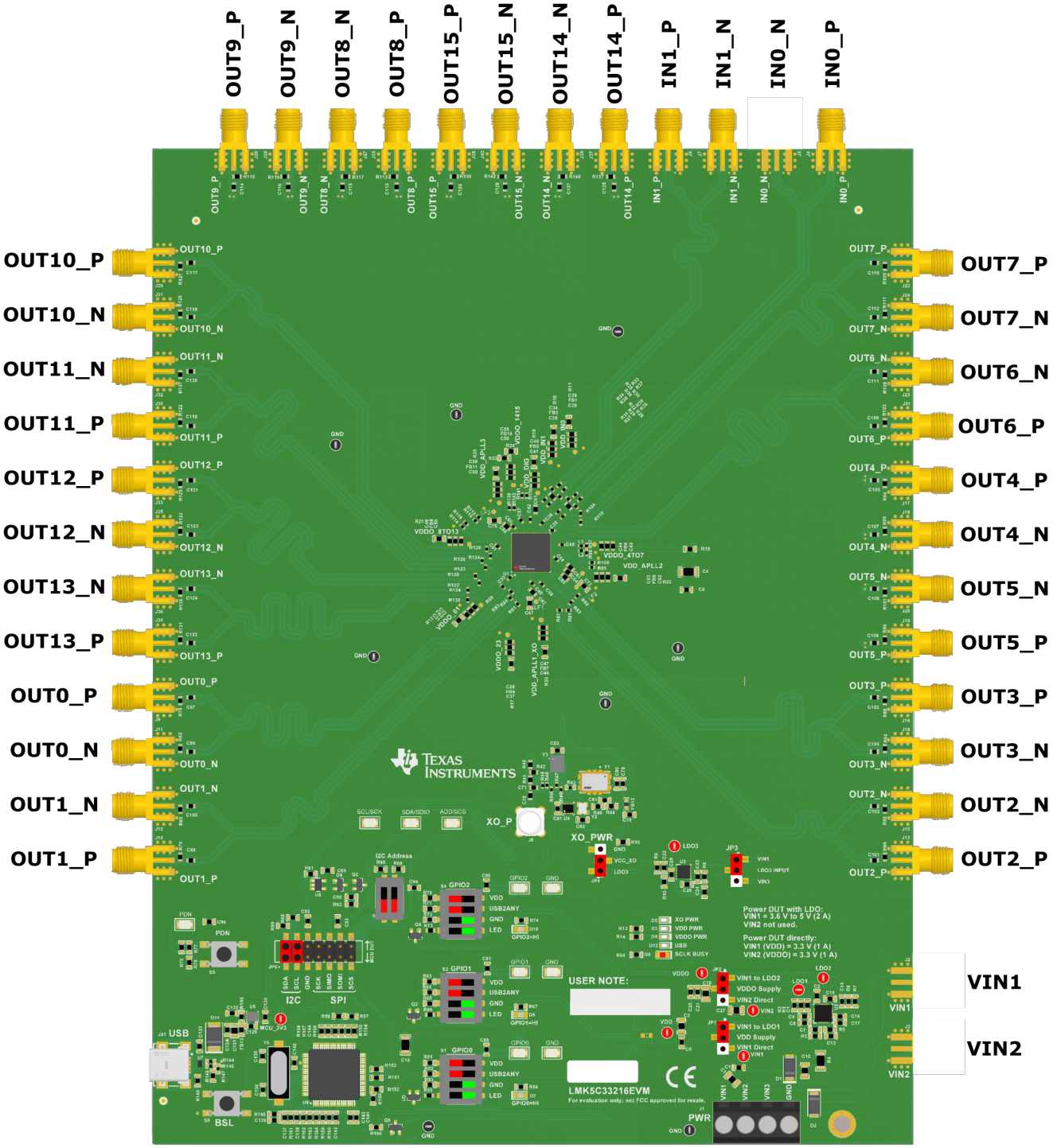

Figure 1-1. LMK5C33216EVM Default Setting of Jumpers and Dip Switches

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2 EVM Quick Start

Table 2-1 describes the default jumper positions for the EVM to power the device from a single 4.5 V supply provided to VIN1. In positional information about jumpers, *adj des* means jumper is placed adjacent to designator. *Opp des* means jumper is placed opposite designator.

Table 2-1. Default Jumper and DIP Switch Settings

CATEGORY	REF DES	POSITION	DESCRIPTION
Power	JP1	1-2 (adj des)	DUT VDD = 3.3 V from LDO1 provided by U3.
	JP2	1-2 (adj des)	DUT VDDO = 3.3 V from LDO2 rail provided by U3.
	JP3	1-2 (adj des)	LDO3 IN powered from VIN1 external supply.
	JP4	1-2 (adj des)	XO VCC = 3.3 V from LDO3.
Communication	JP5	1-2, 3-4	Connect I2C from onboard USB2ANY to DUT
LMK5C33216 Control Pins	S3	S5[1:2] = OFF	SCS_ADD = no pull-up or pull-down.
	S1, S2, S4	Sx[1,2] = OFF Sx[3,4] = ON	Enable 3.9k pull-down on GPIO0, GPIO1, and GPIO2

To begin using the LMK5C33216, follow the steps below.

Hardware Setup

1. Verify the EVM default jumper and DIP switch settings shown in Table 3-1.
2. Connect Power, +4.5 V from an external DC power supply (2-A limit), see Figure 3-2.
   a. To VIN1 & GND terminals on header J1 (pins 1 and 4), or
   b. To VIN1 SMA connector J2.
3. Connect references.
   a. 156.25 MHz reference clock to IN0_P/N and/or,
   b. 10 MHz reference clock to IN1_P/N
4. Connect USB cable to USB port at J41.

Software Setup

1. If not already installed, install TICS Pro software from TI website:
2. If the MATLAB R2015b (9.0)* 64-bit runtime is not already installed, download and install from MathWorks website. While optional for programming and evaluating the default profile settings, the Matlab Runtime is necessary for any application that needs to modify the DPLL loop filter settings. See
3. Start TICS Pro software
4. Select the LMK5C33216 profile from *Select Device → Network Synchronizer Clock (Digital PLLs) → LMK5C33216*
5. Confirm communications with board by
   a. From the menu bar, click *USB communications*.
   b. Click *Interface*
   c. In Communication Setup pop-up window.
      i. Ensure USB2ANY is selected as the interface.
      ii. In case of multiple USB2ANY, select desired interface. If a USB2ANY is currently in use in another TICS Pro, you must release that interface by changing its interface setting to *DemoMode*
      iii. Click identify to blink LED illustrated in Figure 2-1. This confirms you are connected to the board you expect.

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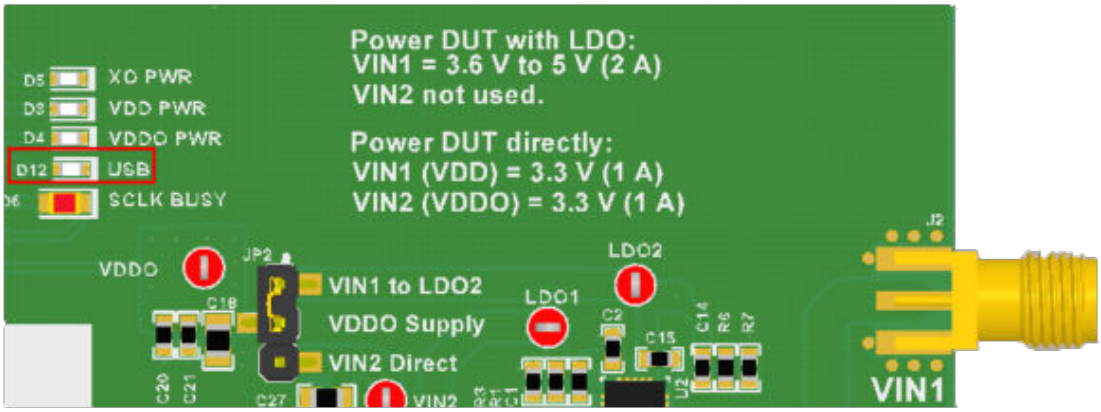

Figure 2-1. USB LED

Program LMK5C33216

1. Toggle switch S5 (PDN/RESET).
2. Program all the registers by…
   a. Pressing Write All Regs button in toolbar
   b. From the menu bar click *USB Communications* then click *Write All Registers*, or
   c. Pressing Ctrl + L.
3. Current consumption should be approximately 1.15 A.
4. Check LMK5C33216 Status
   a. Status Page of GUI
   b. Click Read Status Bits
   c. To clear latched bits.
      i. Press *Clear Latched Bits* button
      ii. Read Status Bits
   d. It may take some time for the DPLL status bits to reflect lock.

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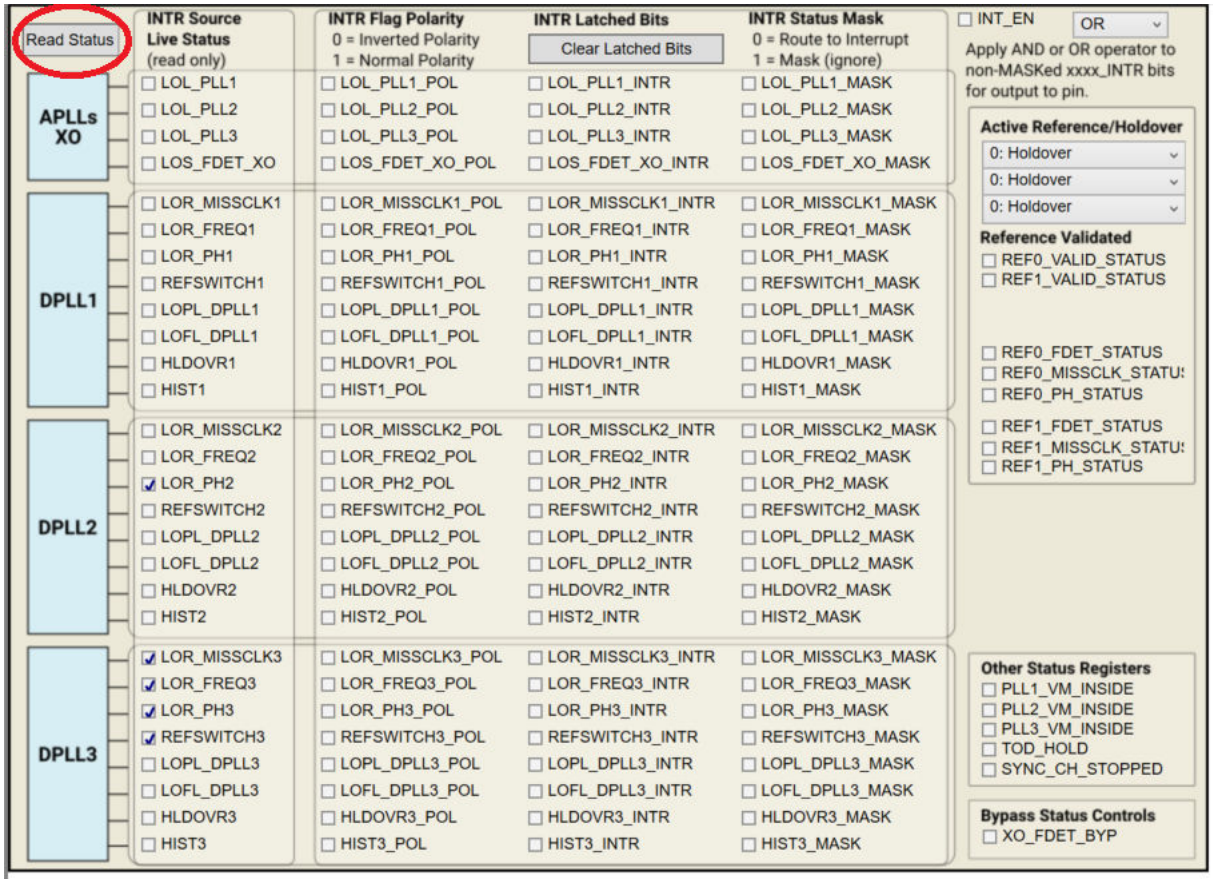

Figure 2-2. Read Status Bits

Measure

Measurements may now be made at the clock outputs.

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3 EVM Configuration

The LMK5C33216 is a highly configurable clock chip with multiple power domains, PLL domains, and clock input and output domains. To support a wide range of LMK5C33216 use cases, the EVM was designed with more flexibility and functionality than needed to implement the chip in a customer system application.

This section describes the power, logic, and clock input and output interfaces on the EVM, as well as how to connect, set up, and operate the EVM. Refer to Figure 4-1.

Table 3-1. Key Components REF DES and Descriptions

ITEM NO.		REF DES	DESCRIPTION
1		U1	LMK5C33216 DUT
2	A	J1 (VIN1 terminal block header), or	External Supply, +5 V using default configuration.
	B	J2 (VIN1 SMA) Not populated by default	
3	A	Y1, or	
	B	J8	
4		J4/5, J6/7	SMA Ports for DUT Clock Inputs (IN0_P/N and IN1_P/N)
5		J9/11, J10/12, J13/15, J14/16, J17/19, J18/20, J21/J23, J22/24, J25/27, J26/28, J29/31, J30/32, J33/35, J34/36, J37/39, J38/40	SMA Ports for DUT Clock Outputs
6		S5	Normally open. Push button for DUT power down (PDN pin). Connect R76 to enable control of the PDN pin through the GUI
7		JP5	Jumper Header for I^2C/SPI interface (MCU to DUT)
8		D6	SCL or SCK busy indication LED.
9		J41	USB Port for MCU

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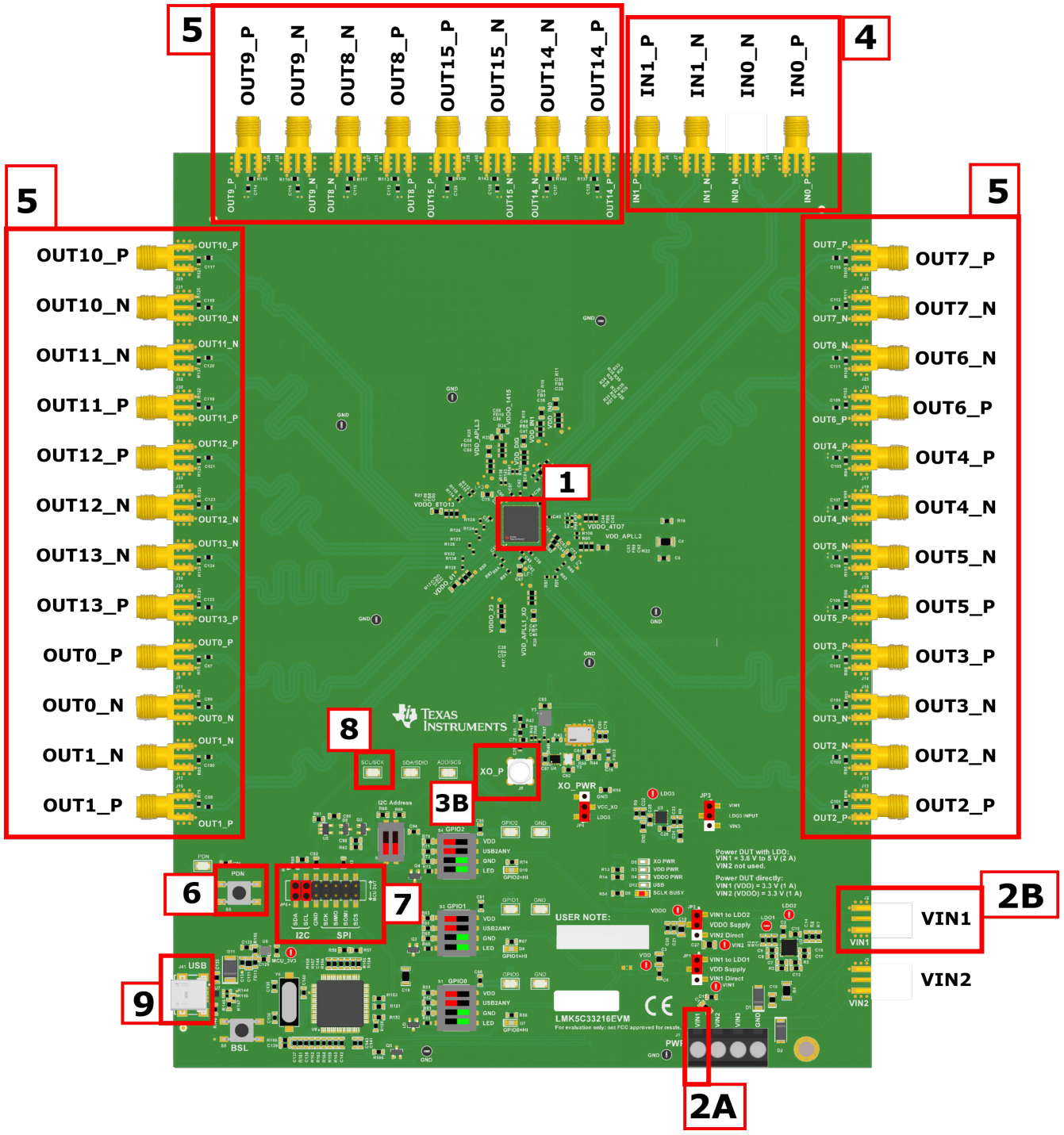

Figure 3-1. Key Components - EVM Top Side

3.1 Power Supply

The LMK5C33216 has VDD and VDDO supply pins that operate from 3.3 V ± 5%.

J1 is the main power terminal to the external power supply. Power SMA port VIN1 (J2) provides an alternative connector style to apply power through coax cable. By default this SMA connector is not populated.

On the EVM, the default power configuration uses the onboard LDO regulators to power all VDD and VDDO pins from an external 5-V supply input VIN1 to J1 (or J2). A Dual LDO regulator (U3) is used to power the VDD and VDDO rails of the DUT and its peripheral circuitry. A separate LDO regulator (U4),also supplied from VIN1, is used to power the onboard XO circuits.

Note

Not every power connection is used or required to operate the EVM. Other power configurations are possible. See the power schematics in Figure 4-1 and Figure 4-2.

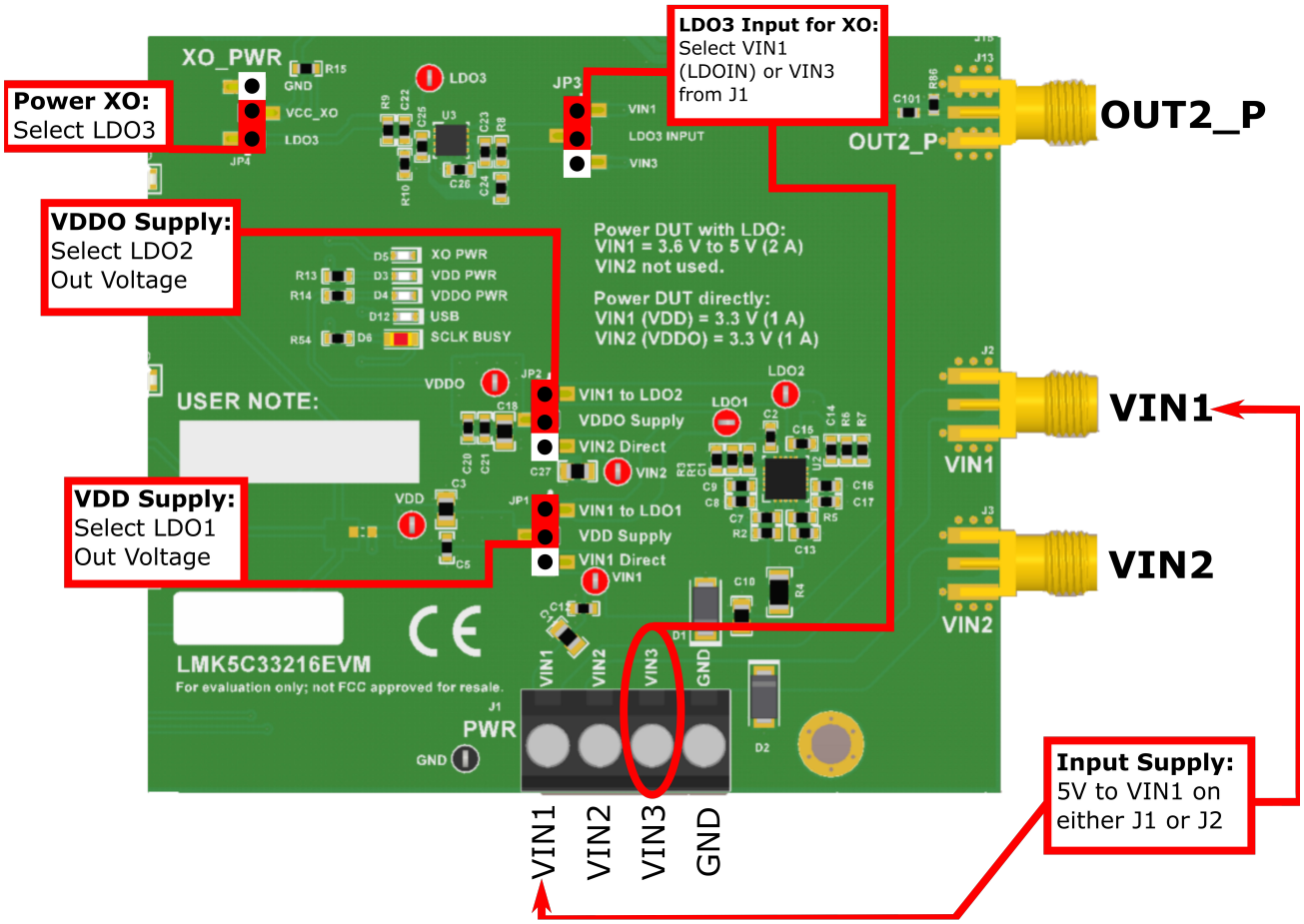

Figure 3-2. Default Power Jumper Configuration

Figure 3-2 shows the default power jumper locations and settings. Table 3-2 shows the suggested power configurations for the DUT.

Table 3-2. Suggested Power Configurations

CONNECTION	NAME	ONBOARD LDO REGULATORS (DEFAULT)	DIRECT EXTERNAL SUPPLIES
		VD = 3.3 V (LDO1) VDDO = 3.3 V (LDO2)	VDD = 3.3 V (EXT. VIN1) VDDO = 3.3 V (EXT. VIN2)
J1	PWR	Pin 1 (VIN1): Connect to external 5-V supply Pin 2 (VIN2): n/a Pin 3 (VIN3): n/a Pin 4 (GND): Connect to supply ground	Pin 1 (VIN1): Connect to external 3.3-V supply Pin 2 (VIN2): Connect to external 3.3-V supply Pin 3 (VIN3): n/a Pin 4 (GND): Connect to supply ground
JP1	VDD	Tie pins 1-2 (adjacent to designator) to select 3.3 V from LDO1 to VDD Plane	Tie pins 2-3 (opposite to designator) to select external VIN1 to VDD Plane
JP2	VDDO	Tie pins 1-2 (adjacent to designator) to select 3.3 V from LDO2 to VDDO Plane	Tie pins 2-3 (opposite to designator) to select external VIN2 to VDDO Plane

3.2 Logic Inputs and Outputs

The logic I/O pins of the DUT support different functions depending on the device start-up mode chosen by the GPIO1 input level upon POR.

The default logic input pin states are determined by onboard pullup or pulldown resistors, but some input pins can be driven to high or low state by the MCU output or DIP switch control. The MCU can be controlled from a PC running TICS Pro software to program the device registers through I2C or SPI and also drive the DUT logic inputs. To allow the MCU to control the pin input, SW[2] must be set to on.

See Table 3-3 for the logic pin mapping tables for the device start-up modes.

Table 3-3. Device Start-Up Modes

GPIO1 Input Level[1]	Start-up Mode
0	I^2C Mode
1	SPI Mode

1. The input levels on these pins are sampled only during POR.

3.3 Switching Between I2C and SPI

To switch the EVM between I2C and SPI modes, the switches and jumpers must be configured as follows:

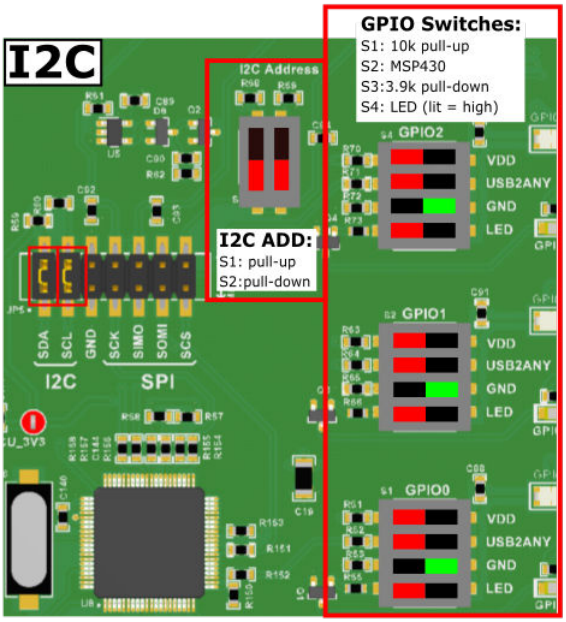

Figure 3-3. I2C Mode Jumper Configuration

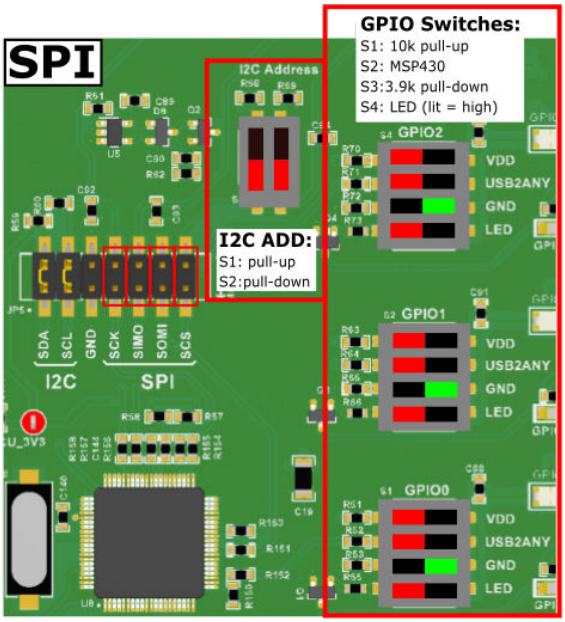

Figure 3-4. SPI Mode Jumper Configuration

In SPI mode, GPIO2 must also be configured as *STATUS or INT* and *SPI Readback Data (SDO)* to support SPI readback.

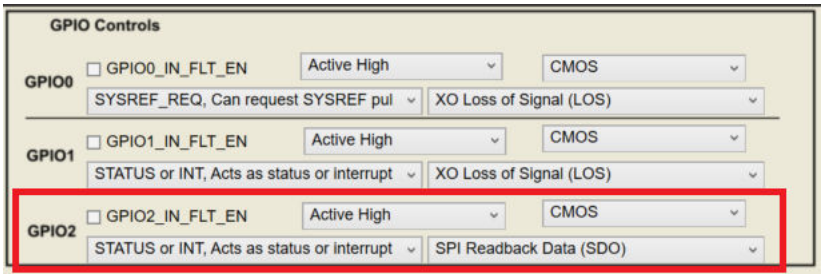

Figure 3-5. GPIO2 Setting for SPI Mode

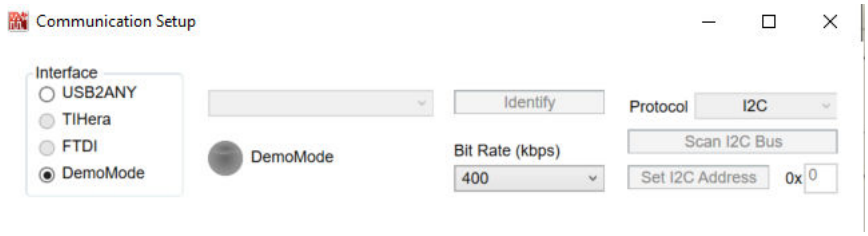

Figure 3-6. Communication Setup Window (Changing from I2C to SPI)

3.4 Generating SYSREF Request

GPIO0 and GPIO1 can be used to generate a SYSREF request. The TICS Pro software + EVM is designed to use GPIO2 for SPI readback (SDO). Accordingly, GPIO2 is not listed in the pins as it is dedicated for SPI readback. In user application, any GPIO pin may be used.

Connect the desired GPIO pin to the MCU by setting S2 as ON on the switch block for the desired GPIO. Then, make sure the GPIO pin is configured for *SYSREF_REQ* on the GPIO tab of the GUI. A SYSREF Request can now be issued by toggling the GPIO buttons in the *Pins* section of the *User Controls* tab.

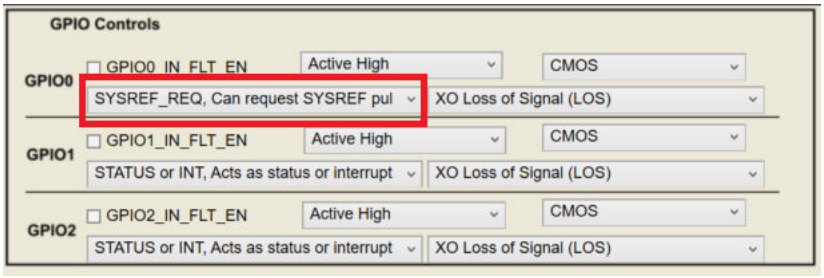

Figure 3-7. GPIO Setting for SYSREF Request

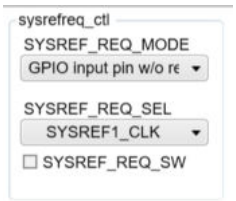

Figure 3-8. SYSREF Request Control

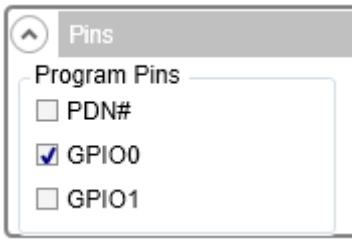

Figure 3-9. GPIO Pin Selection for SYSREF

3.5 XO Input

The LMK5C33216 has an XO input (XO_P pin) to accept a reference clock for the Fractional-N APLLs. The XO input determines the output frequency accuracy and stability in free-run or holdover modes. For synchronization applications like SyncE or IEEE 1588, the XO input would typically be driven by a low frequency TCXO, OCXO, or external traceable clock that conforms to the frequency accuracy and holdover stability requirements of the application. For DPLL mode, the XO frequency must have a non-integer frequency relationship with the VCO frequency of any APLLs which utilize XO input as their reference. For APLL only mode (DPLL not used), the XO

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frequency can have an integer relationship with the VCO to avoid fractional spurs. Any APLL may accept any other APLL as a reference instead of the XO. The BAW on APLL3 provides a good option for a high frequency cascaded referenced.

The XO input of the LMK5C33216 has programmable on-chip input termination and AC-coupled input biasing options to support any clock interface type.

For flexibility, the EVM provides the XO input options (use one at a time). C70 allows an external reference to be provided at SMA connector XO_P (J8). C71 allows one of the on board XO/TCXO/OCXO footprints to be used. By default Y1 is populated with a 38.88 MHz TCXO and selected with the populated R43. Other XO/TCXO/ OCXO may be installed and connected using the appropriate resistor. Care should be taken if more than one device is installed to remove resistors for isolation.

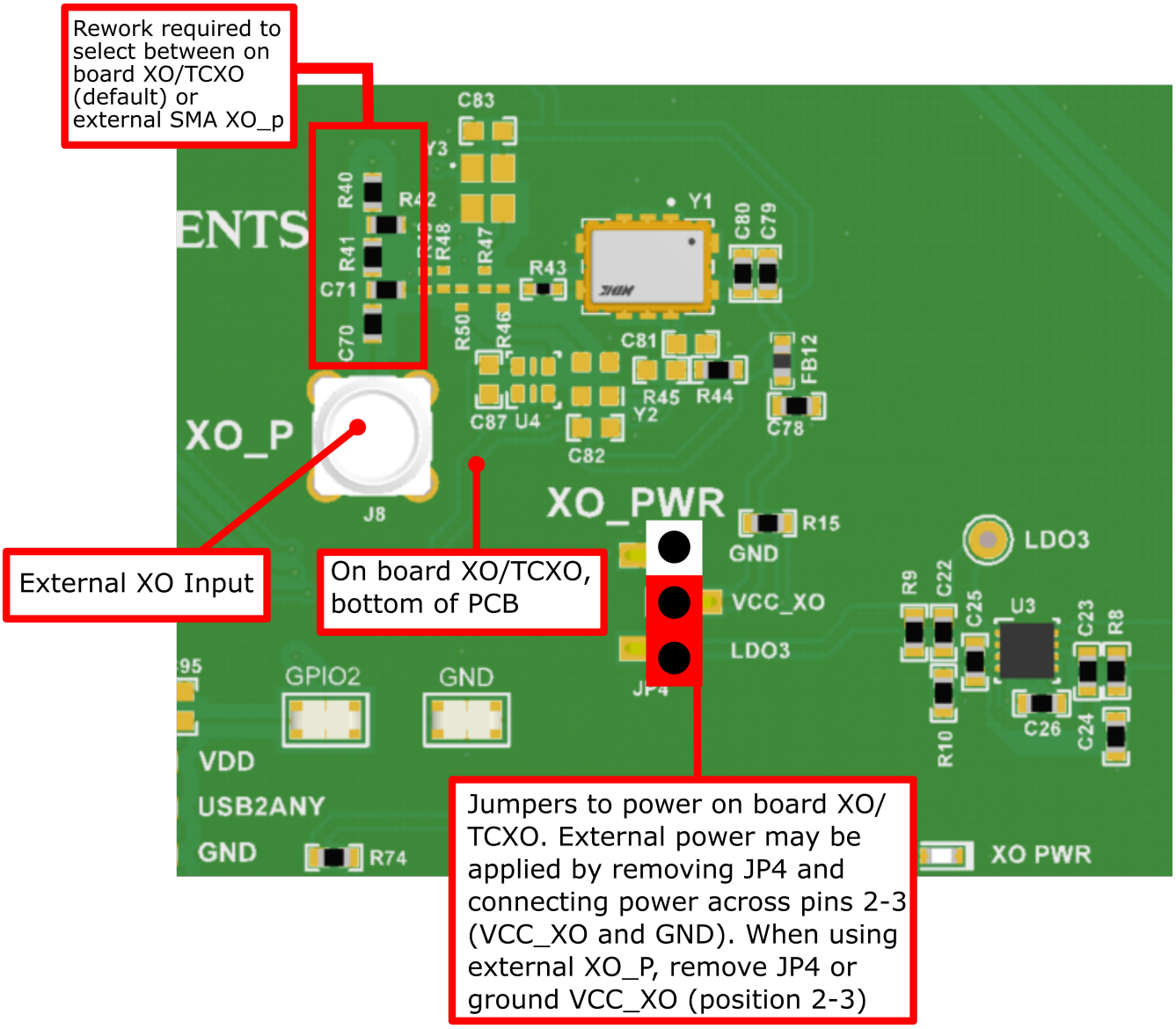

Figure 3-10. XO Input

3.5.1 38.88-MHz TCXO (Default)

By default, the EVM is populated with a 38.88-MHz, 3.3-V LVCMOS, low-jitter TCXO (Y1) to drive the XO_P input of the DUT with the onboard termination and AC coupling. See Figure 3-10. Y1 can be used to evaluate various frequency configurations.

3.5.2 External Clock Input

Another option is to feed an external clock to the SMA ports (J8) to drive the XO_P input. See Figure 3-10. This path can be connected to the XO_P input pins. Y1 should be powered down when using the external XO input path.

3.6 Reference Clock Inputs

The LMK5C33216 has two DPLL reference clock input pairs (IN0_P/N and IN1_P/N) with configurable input priority and input selection modes. The inputs have programmable input type, termination, and biasing options to support any clock interface type.

External LVCMOS or Differential reference clock inputs can be applied to the SMA ports, labeled IN0_P/N and IN1_P/N. All SMA inputs are routed through 50-Ω single-ended traces and DC coupled to the corresponding IN0_P/N and IN1_P/N pins of the DUT. Single ended singles should be connected to the non-inverting input, IN0_P or IN1_P.

3.7 Clock Outputs

The LMK5C33216 has 16 clock output pairs (OUT[0:15]_P/N).

Output clocks are AC-coupled to the SMA ports labeled OUT[0:15]_P/N.

3.8 Status Outputs and LEDS

Status outputs signals can be configured on the GPIO0, GPIO1, and GPIO2 pins. The status output signal, output type (3.3-V LVCMOS or NMOS open-drain).

3.9 Requirements for Making Measurements

When performing measurements with the LMK5C33216EVM, the following procedures must be completed:

1. Ensure all required outputs have proper termination components installed to match the desired output types. Recommended output terminations for each output type are shown in Figure 3-11.

Driver	R_B (Ω)
LVDS	open
CML*	open
LVPECL	120
HCSL	50

*CML driver has 50-Ω pull-up

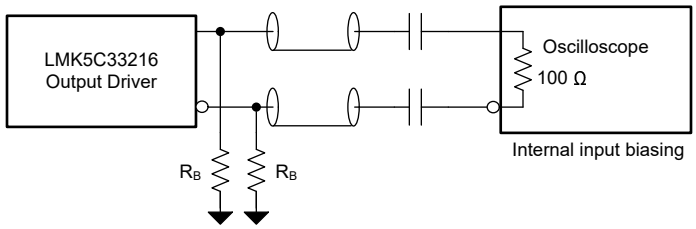

Figure 3-11. Output Termination Recommendations

2. Ensure all enabled outputs that are not connected to any test equipment have a 50 Ω SMA termination. An example of a 50 Ω SMA termination is shown in Figure 3-12.

Figure 3-12. 50 Ω SMA Termination

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4 EVM Schematics

4.1 Power Supply Schematic

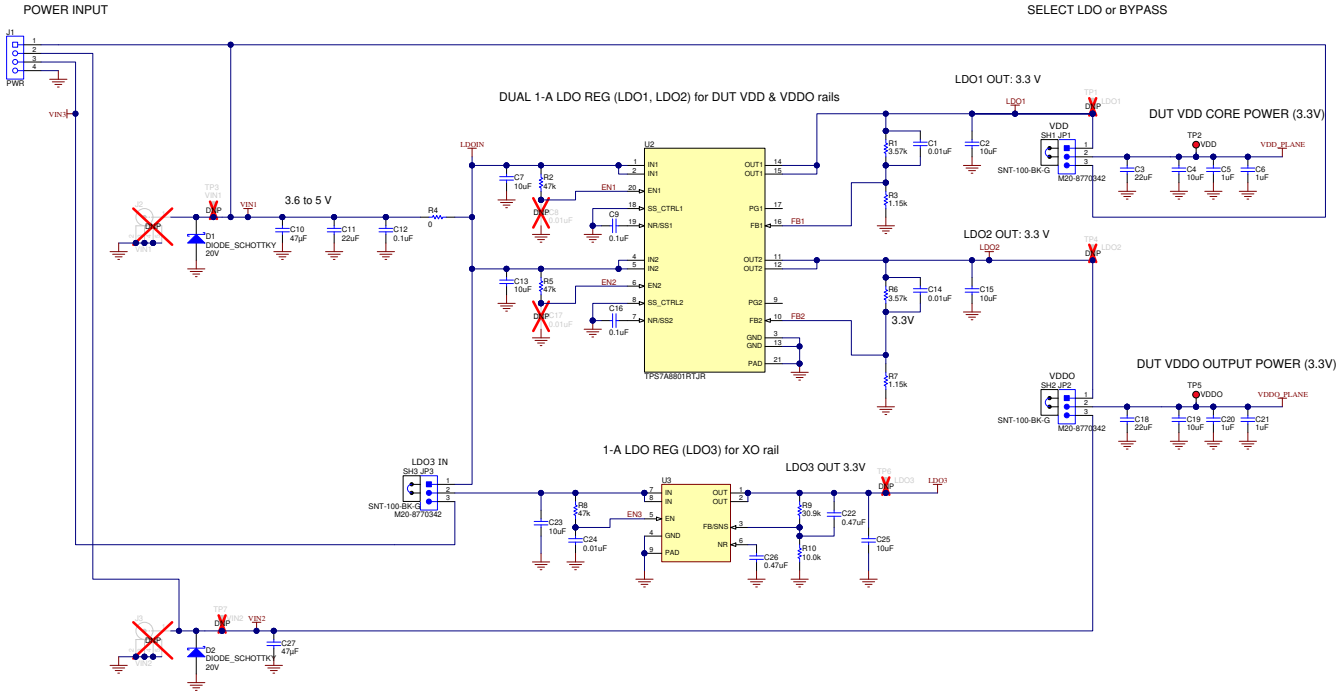

Figure 4-1. Power Supplies

4.2 Power Distribution Schematic

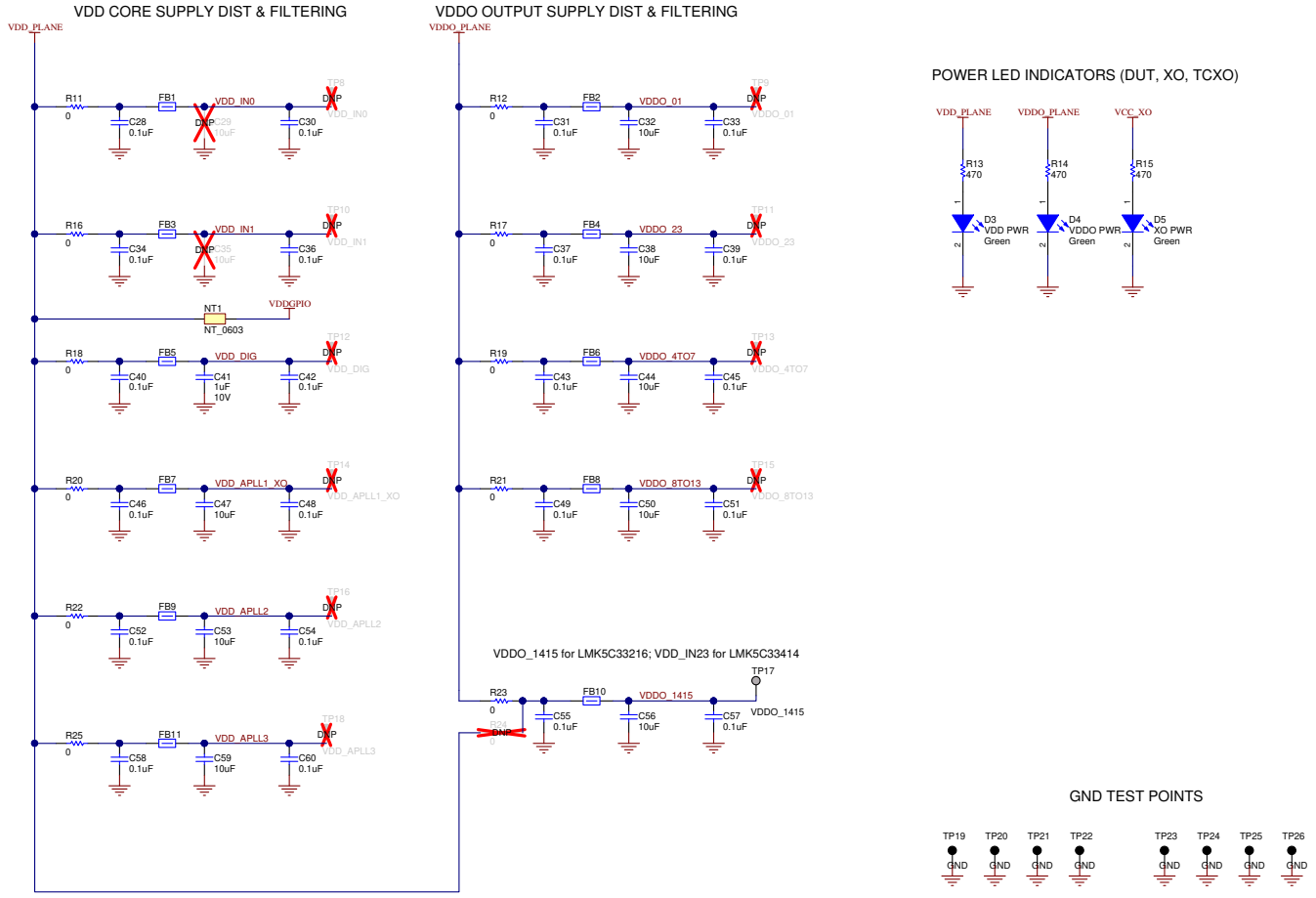

Figure 4-2. Power Distribution

4.3 LMK5C33216 and Input Reference Inputs IN0 to IN1 Schematic

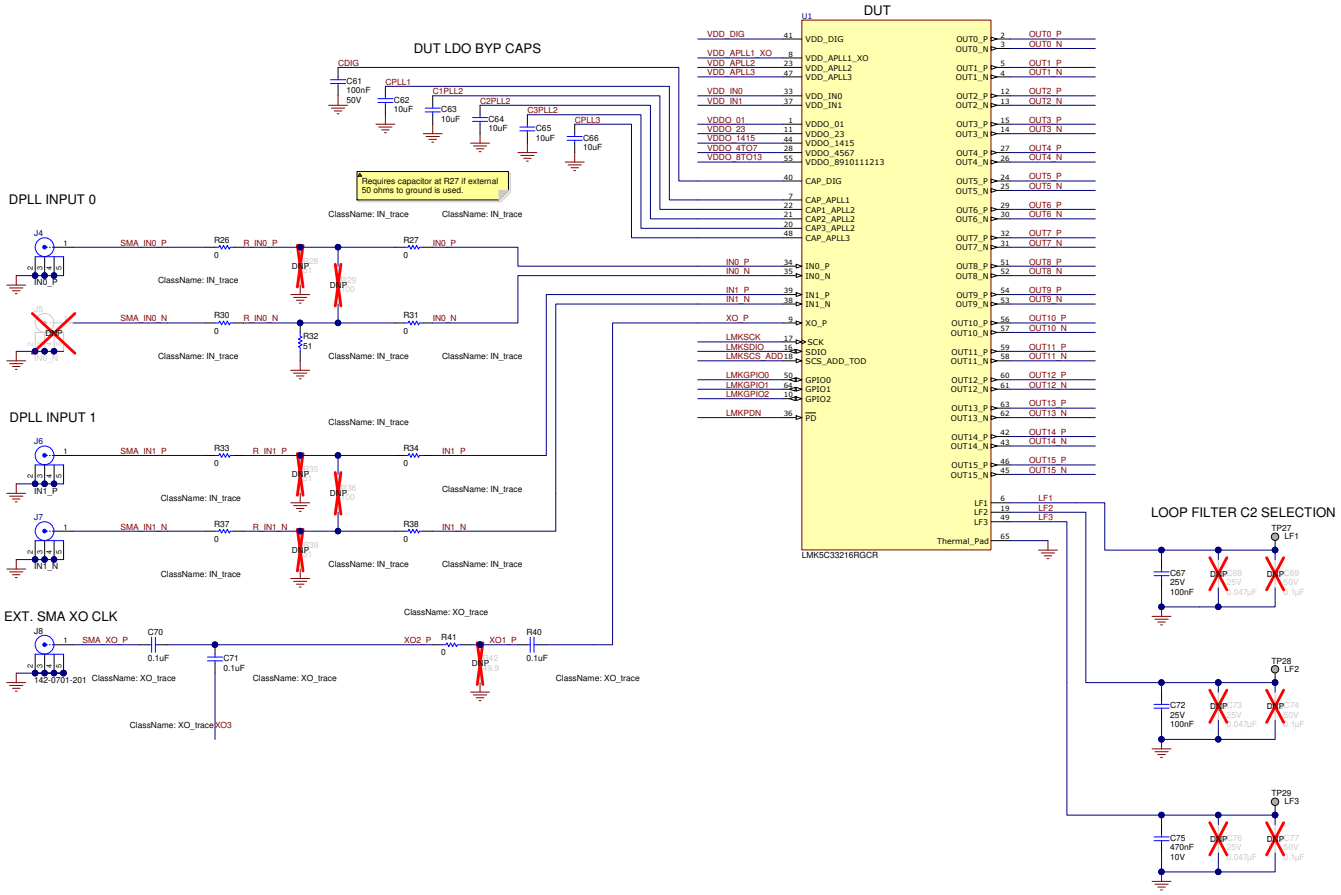

Figure 4-3. LMK5C33216 and Input Reference Inputs IN0 to IN1

4.4 Clock Outputs OUT0 to OUT3 Schematic

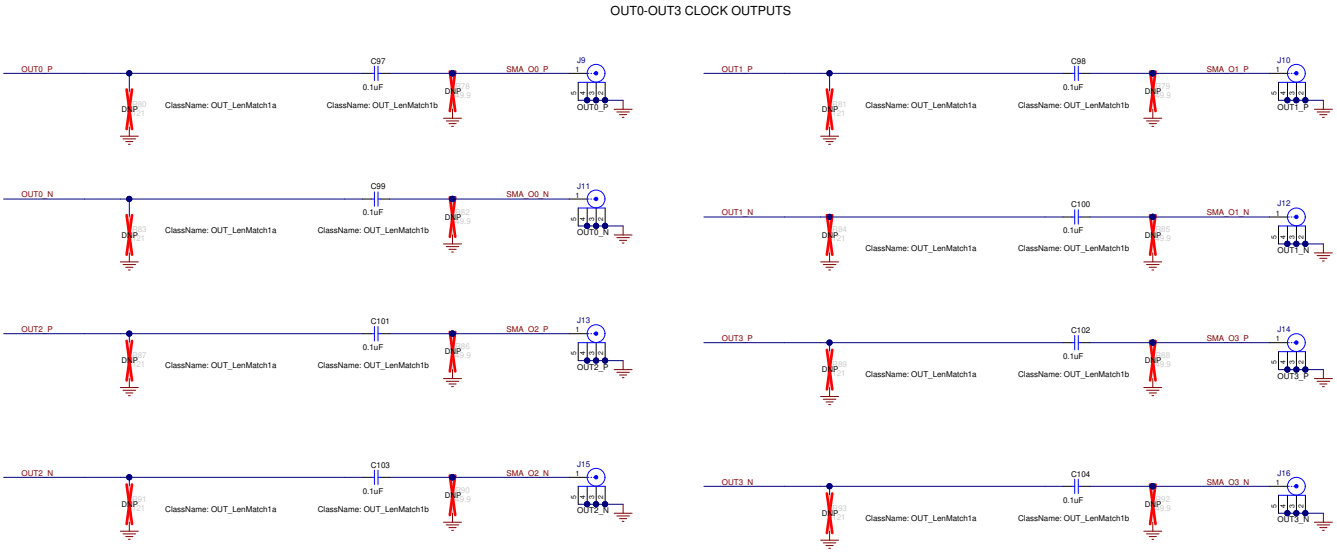

Figure 4-4. Clock Outputs OUT0 to OUT3

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4.5 Clock Outputs OUT4 to OUT9 Schematic

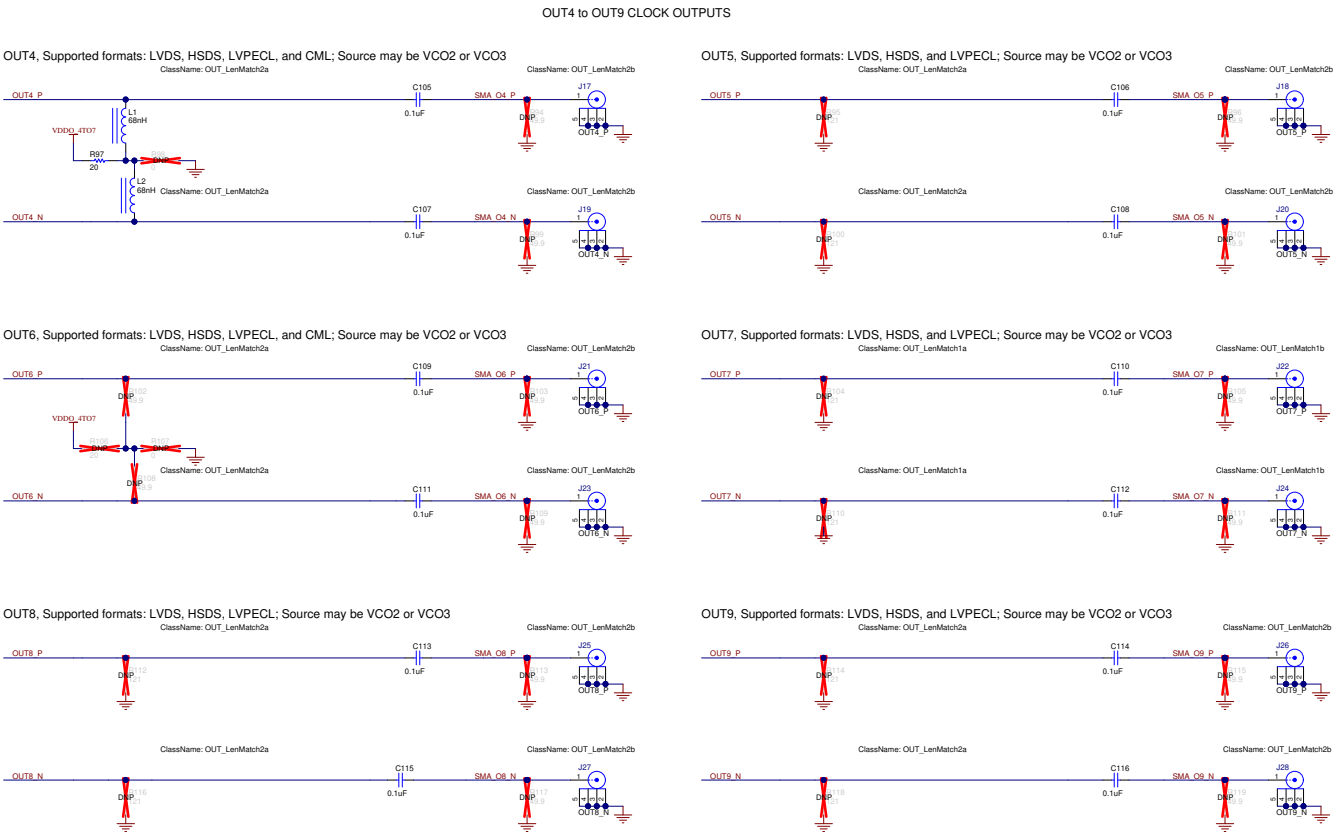

Figure 4-5. Clock Outputs OUT4 to OUT9

4.6 Clock Outputs OUT10 to OUT15 Schematic

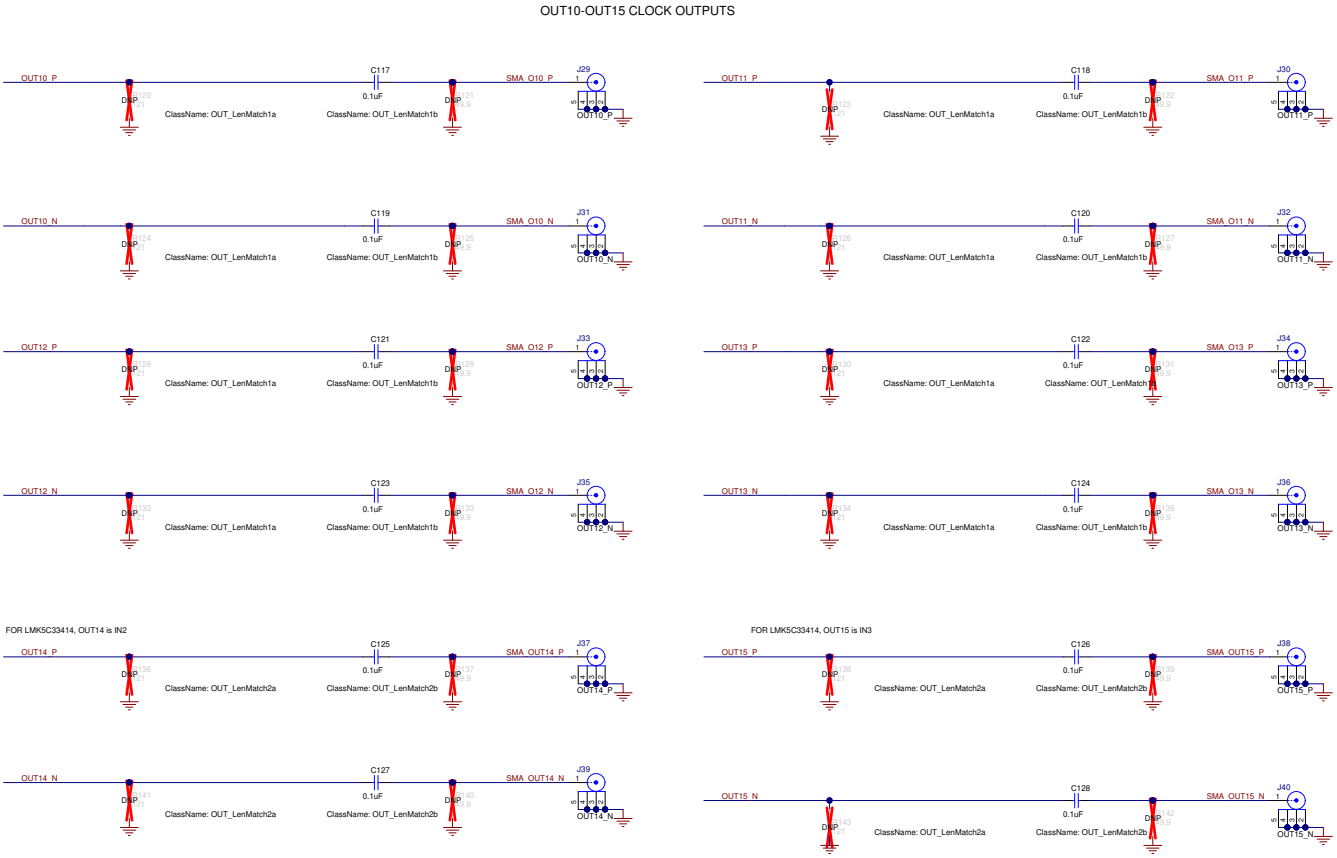

Figure 4-6. Clock Outputs OUT10 to OUT15

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4.7 XO Schematic

3.3V LVCMOS XO (multiple footprints)

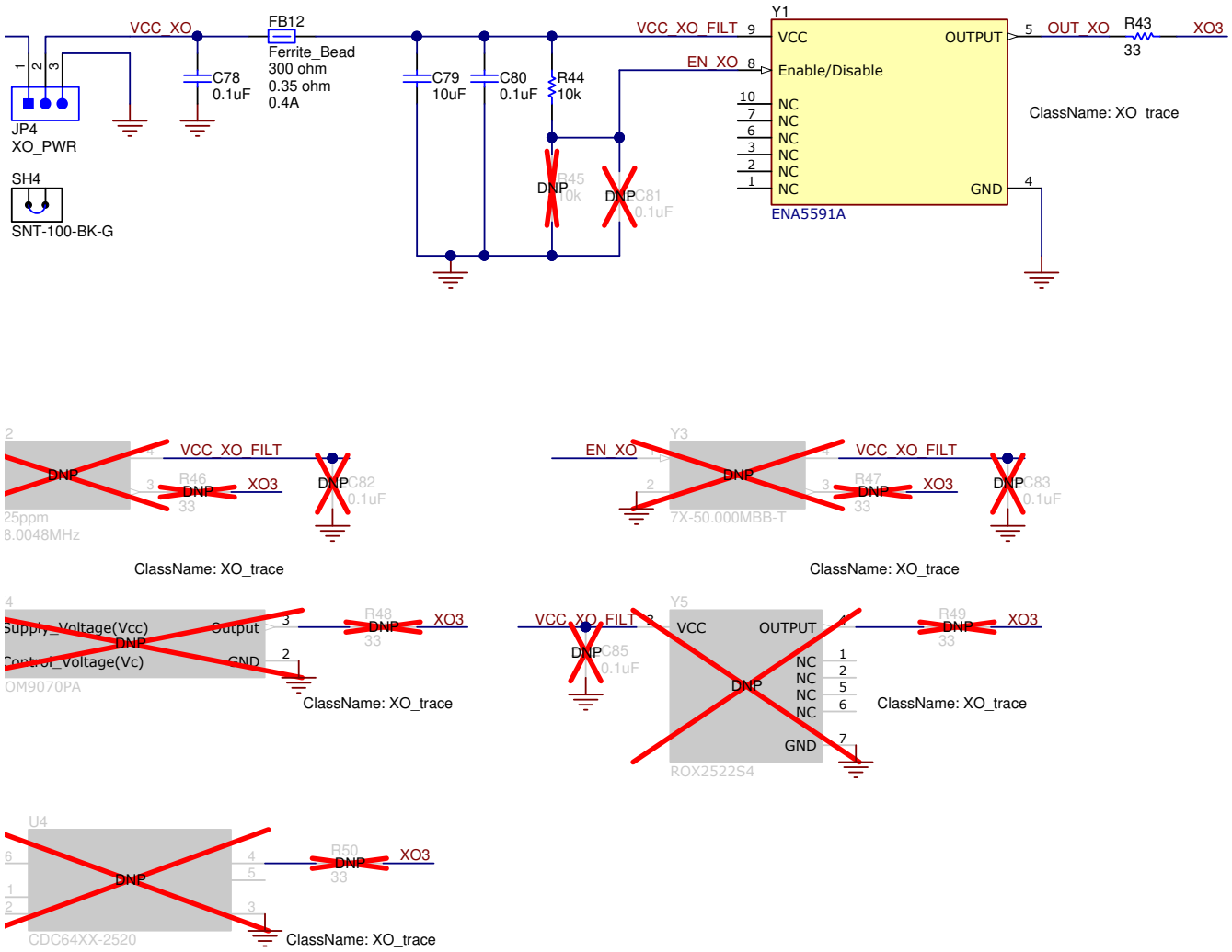

Figure 4-7. XO

4.8 Logic I/O Interfaces Schematic

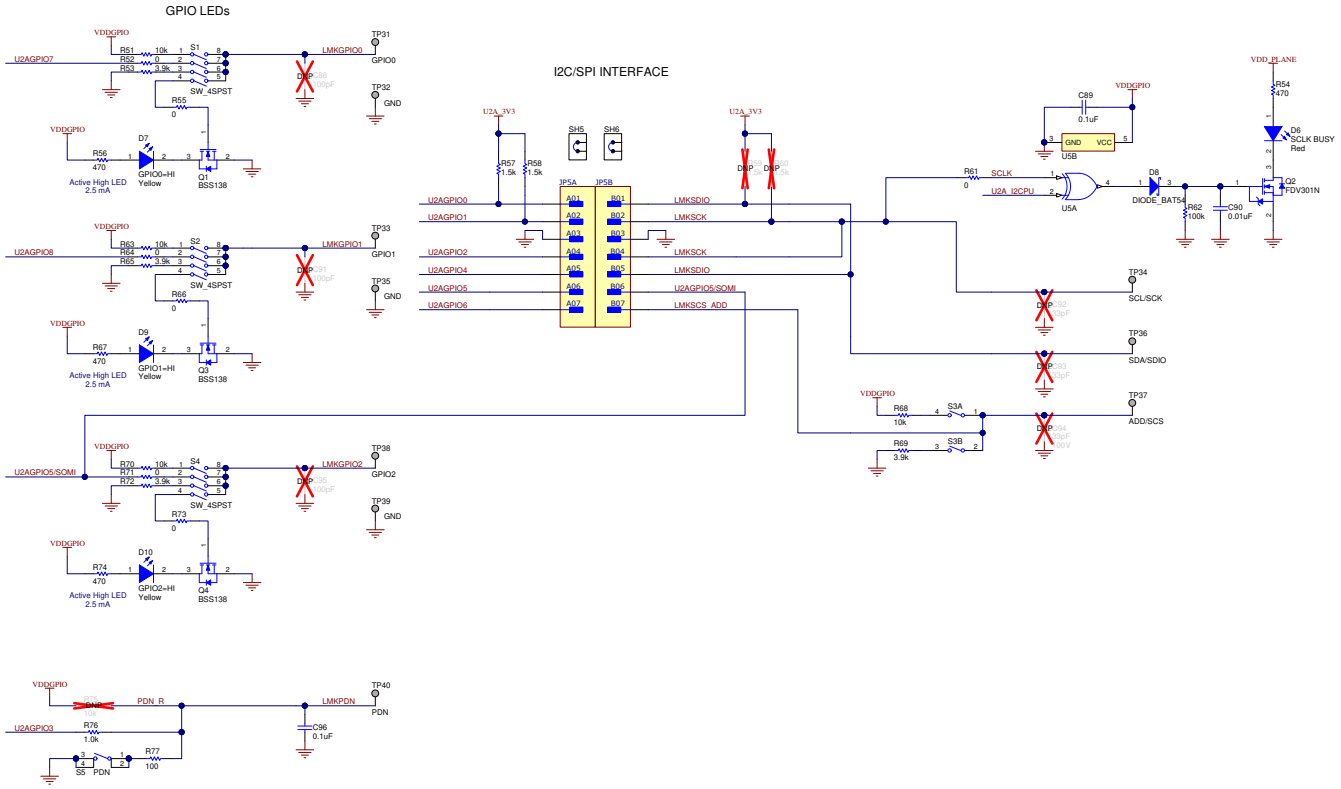

Figure 4-8. Logic I/O Interfaces

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4.9 USB2ANY Schematic

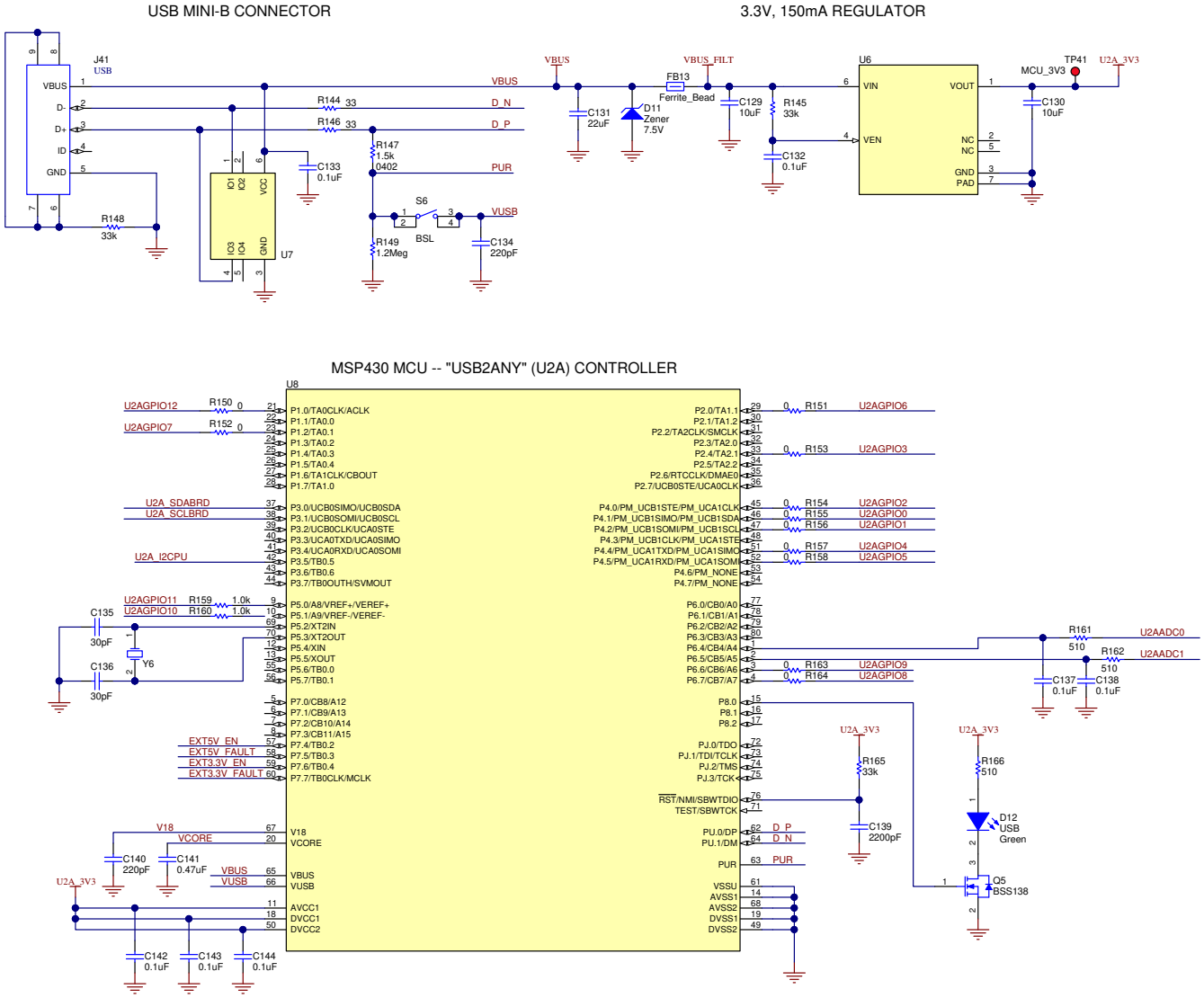

Figure 4-9. USB MCU

5 EVM Bill of Materials

Table 5-1. EVM BOM

Designator	QTY	Value	Description	PartNumber	Manufacturer
!PCB1	1		Printed Circuit Board	HSDC102	Any
C1, C14, C24, C90	4	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0603	C0603C103J5RACTU	Kemet
C2, C7, C13, C15, C23, C25, C32, C38, C44, C47, C50, C53, C56, C59, C62, C63, C64, C65, C66, C79, C129, C130	22	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0603	C1608X5R1A106M080AC	TDK
C3, C11, C18, C131	4	22uF	CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0805	LMK212BJ226MG-T	Taiyo Yuden
C4, C19	2	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X7R, 1206	C3216X7R1A106M160AC	TDK
C5, C6, C20, C21, C41	5	1uF	CAP, CERM, 1 uF, 10 V, +/- 10%, X5R, 0603	C0603C105K8PACTU	Kemet
C9, C16, C28, C31, C34, C37, C40, C43, C46, C49, C52, C55, C58, C67, C70, C71, C72, C78, C80, C96, C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, R40	53	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	C0603C104J3RACTU	Kemet
C10, C27	2	47uF	CAP, CERM, 47 µF, 10 V,+/- 20%, X5R, 0805	GRM21BR61A476ME15L	MuRata
C12, C89, C132, C133, C137, C138, C142, C143, C144	9	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 5%, X7R, 0603	C0603C104J4RACTU	Kemet
C22, C26	2	0.47uF	CAP, CERM, 0.47 uF, 10 V, +/- 10%, X7R, 0603	C0603C474K8RACTU	Kemet
C30, C33, C36, C39, C42, C45, C48, C51, C54, C57, C60	11	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402	C1005X5R1A104K050BA	TDK
C61	1	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	C1608X7R1H104K080AA	TDK
C75, C141	2	0.47uF	CAP, CERM, 0.47 uF, 10 V, +/- 10%, X7R, 0603	GRM188R71A474KA61D	MuRata
C134, C140	2	220pF	CAP, CERM, 220 pF, 50 V, +/- 1%, C0G/NP0, 0603	06035A221FAT2A	AVX
C135, C136	2	30pF	CAP, CERM, 30 pF, 100 V, +/- 5%, C0G/NP0, 0603	GRM1885C2A300JA01D	MuRata
C139	1	2200pF	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603	C0603C222K5RACTU	Kemet
D1, D2	2	20V	Diode, Schottky, 20 V, 2 A, SMA	B220A-13-F	Diodes Inc.
D3, D4, D5, D12	4	Green	LED, Green, SMD	LTST-C190GKT	Lite-On
D6	1	Red	LED, Red, SMD	LTST-C170KRKT	Lite-On
D7, D9, D10	3	Yellow	LED, Yellow , SMD	LTST-C170KSKT	Lite-On
D8	1	30V	Diode, Schottky, 30 V, 0.2 A, SOT-23	BAT54-7-F	Diodes Inc.
D11	1	7.5V	Diode, Zener, 7.5 V, 550 mW, SMB	1SMB5922BT3G	ON Semiconductor

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Table 5-1. EVM BOM (continued)

Designator	QTY	Value	Description	PartNumber	Manufacturer
FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9, FB10, FB11	11	220 ohm	Ferrite Bead, 220 ohm @ 100 MHz, 2.5 A, 0603	BLM18SG221TN1D	MuRata
FB12	1	300 ohm	Ferrite Bead, 300 ohm @ 100 MHz, 0.4 A, 1.6x0.8x0.95mm	LI0603D301R-10	Laird-Signal Integrity Products
FB13	1	60 ohm	Ferrite Bead, 60 ohm @ 100 MHz, 3.5 A, 0603	MPZ1608S600ATAH0	TDK
FID1, FID2, FID3, FID4, FID5, FID6	6		Fiducial mark. There is nothing to buy or mount.	N/A	N/A
H1, H2, H3, H4, H5, H6	6		BUMPER CYLIN 0.312" DIA	SJ61A6	3M
J1	1		Terminal Block, 4x1, 5.08mm, TH	39544-3004	Molex
J4, J6, J7, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40	35		CONN SMA JACK STR EDGE MNT	CON-SMA-EDGE-S	RF Solutions Ltd.
J8	1		Connector, SMA, TH	142-0701-201	Cinch Connectivity
J41	1		Connector, Receptacle, Mini-USB Type B, R/A, Top Mount SMT	1734035-2	TE Connectivity
JP1, JP2, JP3, JP4	4		Header, 2.54mm, 3x1, Gold, SMT	M20-8770342	Harwin
JP5	1		Connector Header Surface Mount 14 position 0.100" (2.54mm)	54202-G0807LF	Amphenol ICC
L1, L2	2	68nH	Inductor, Multilayer, Composite, 68 nH, 0.15 A, 1.5 ohm, AEC-Q200 Grade 1, SMD	MLK1005S68NJTD25	TDK
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady
Q1, Q3, Q4, Q5	4	50V	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	BSS138	Fairchild Semiconductor
Q2	1	25V	MOSFET, N-CH, 25 V, 0.22 A, SOT-23	FDV301N	Fairchild Semiconductor
R1, R6	2	3.57k	RES, 3.57 k, 1%, 0.1 W, 0603	RC0603FR-073K57L	Yageo
R2, R5, R8	3	47k	RES, 47 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060347K0JNEA	Vishay-Dale
R3, R7	2	1.15k	RES, 1.15 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K15FKEA	Vishay-Dale
R4	1	0	RES, 0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	CRCW12060000Z0EA	Vishay-Dale
R9	1	30.9k	RES, 30.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060330K9FKEA	Vishay-Dale
R10	1	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310K0FKEA	Vishay-Dale
R11, R12, R16, R17, R18, R19, R20, R21, R22, R23, R25, R41, R52, R55, R61, R64, R66, R71, R73, R150, R151, R152, R153, R154, R155, R156, R157, R158, R163, R164	30	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06030000Z0EA	Vishay-Dale
R13, R14, R15, R54, R56, R67, R74	7	470	RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603470RJNEA	Vishay-Dale

Table 5-1. EVM BOM (continued)

Designator	QTY	Value	Description	PartNumber	Manufacturer
R26, R27, R30, R31, R33, R34, R37, R38	8	0	RES, 0, 0%, 0.2 W, AEC-Q200 Grade 0, 0402	CRCW04020000Z0EDHP	Vishay-Dale
R32	1	51	RES, 51, 5%, 0.0625 W, 0402	RC0402JR-0751RL	Yageo America
R42	1	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060349R9FKEA	Vishay-Dale
R43	1	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04020000Z0ED	Vishay-Dale
R44, R51, R63, R68, R70	5	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310K0JNEA	Vishay-Dale
R53, R65, R69, R72	4	3.9k	RES, 3.9 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06033K90JNEA	Vishay-Dale
R57, R58	2	1.5k	RES, 1.5 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K50JNEA	Vishay-Dale
R62	1	100k	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100KJNEA	Vishay-Dale
R76, R159, R160	3	1.0k	RES, 1.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K00JNEA	Vishay-Dale
R77	1	100	RES, 100, 5%, 0.25 W, AEC-Q200 Grade 0, 0603	ESR03EZPJ101	Rohm
R97	1	20	RES, 20, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040220R0JNED	Vishay-Dale
R144, R146	2	33	RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040233R0JNED	Vishay-Dale
R145, R148, R165	3	33k	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060333K0JNEA	Vishay-Dale
R147	1	1.5k	RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04021K50JNED	Vishay-Dale
R149	1	1.2Meg	RES, 1.2 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031M20JNEA	Vishay-Dale
R161, R162, R166	3	510	RES, 510, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603510RJNEA	Vishay-Dale
S1, S2, S4	3		Switch, SPST 4 Pos, Top Actuated, SMT	219-4LPST	CTS Electrocomponents
S3	1		Switch, Slide, SPST 2 poles, SMT	219-2LPST	CTS Electrocomponents
S5, S6	2		Switch, Tactile, SPST-NO, 0.05A, 12V, SMT	FSM4JSMA	TE Connectivity
SH1, SH2, SH3, SH4, SH5, SH6	6	1x2	Shunt, 100mil, Gold plated, Black	SNT-100-BK-G	Samtec
TP2, TP5, TP41	3		Test Point, Miniature, Red, TH	5000	Keystone
TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26	8		Test Point, Miniature, Black, TH	5001	Keystone
TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40	10		Test Point, Miniature, SMT	5019	Keystone
U1	1		Ultra-Low Jitter Clock Synchronizer with JESD204B for Wireless Communications	LMK5C33216RGCR	Texas Instruments
U2	1		Dual 1A Low-Noise (3.8µVRMS) LDO Voltage Regulator, RTJ0020D (WQFN-20)	TPS7A8801RTJR	Texas Instruments
U3	1		Low-Noise, High-Bandwidth PSRR, Low-Dropout 1-A Linear Regulator, DRB0008A (VSON-8)	TPS7A8101DRBR	Texas Instruments
U5	1		Single 2-Input Exclusive-OR Gate, DBV0005A (SOT-23-5)	SN74LVC1G86DBVR	Texas Instruments

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Table 5-1. EVM BOM (continued)

Designator	QTY	Value	Description	PartNumber	Manufacturer
U6	1		150-mA Ultra-Low Noise LDO for RF and Analog Circuits Requires No Bypass Capacitor, NGF0006A (WSON-6)	LP5900SD-3.3/NOPB	Texas Instruments
U7	1		4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	TPD4E004DRYR	Texas Instruments
U8	1		25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	MSP430F5529IPN	Texas Instruments
Y1	1		Quartz Crystal Controlled Oscillators	ENA5591A	NDK
Y6	1		Crystal, 24.000 MHz, 20pF, SMD	ECS-240-20-5PX-TR	ECS Inc.

5.1 Loop Filter and Vibration Nonsensitive Capacitors

The capacitors used on the EVM use are X7R which are ferromagnetic and therefore sensitive to vibration due to the piezoelectric effect. It is recommended to use non-ferromagnetic capacitors such as NP0, C0G, or Tantalum for applications in which optimal performance is required in the presence of vibration.

At and below 47 nF, C0G/NP0 capacitors are available in 0805 sized packages. For values 0.1 uF and above Tantalum capacitors may be considered for vibration immune loop filter components.

Table 5-2. Examples of Substitute Capacitors Which are Vibration Immune

CAPACITOR VALUE	VIBRATION SENSITIVE, X7R	VIBRATION IMMUNE
3.3 nF	C0603C332K5RACTU, 0603	GRM1885C1H332JA01D, C0G/NP0, 0603
33 nF	C0603C333J3RACTU, 0603	C2012C0G1H333J125AA, C0G/NP0, 0805
47 nF	06035C473JAT2A, 0603	C0805X473G3GEC7800, C0G/NP0, 0805 C0805C473J3GACTU, C0G/NP0, 0805
0.1 uF	C0603C104J3RACTU, 0603	GRM31C5C1E104JA01L, C0G/NP0, 1206 TAJR104K020RNJ, Tantalum, 0805
0.47 uF	GRM188R71A474KA61D, 0603	F921C474MPA, Tantalum, 0805

6 Appendix A - TICS Pro LMK5C33216 Software

6.1 Using the Start Page

The Start Page can be used to configure the PLLs for specific VCO frequencies and DPLL operation.

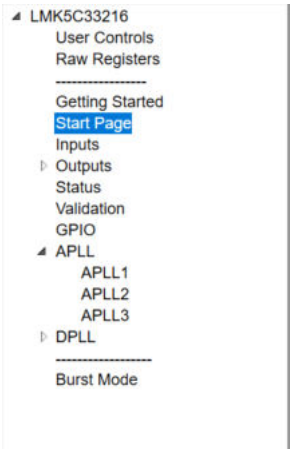

Figure 6-1. Start Page Location

6.1.1 Step 1

Setup the XO_P input frequency and interface type. Setup the input to the APLL by specifying the reference to each PLL and associated settings for PLL phase detector frequency.

6.1.2 Step 2

In Step 2, setup the clock input frequencies and the interface type. Cascaded APLLs can also be assigned from this page using the PLL R-divider and phase detector preview to the right.

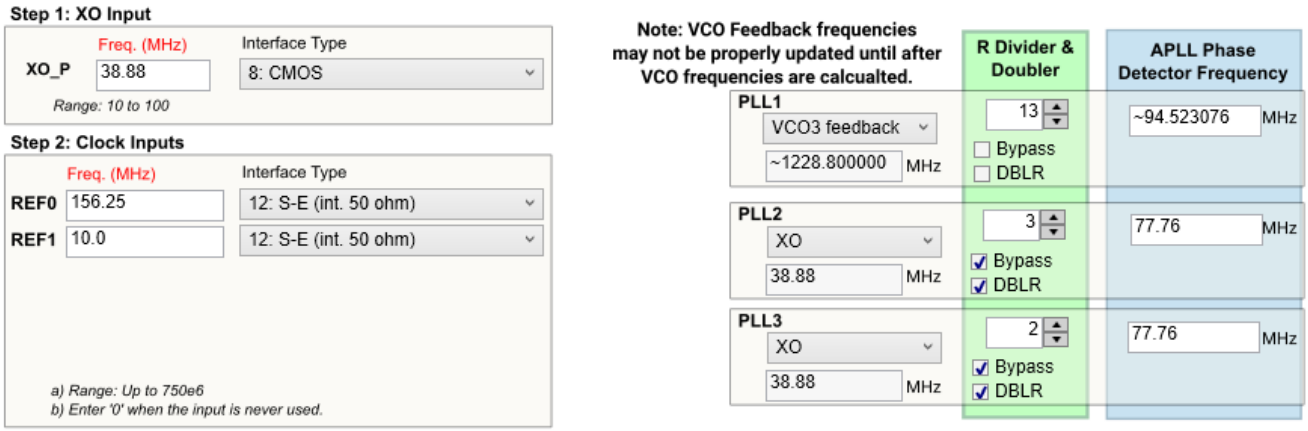

Figure 6-2. Step 1 and 2: XO Input and Clock Inputs

6.1.3 Step 3

Set the clock input select mode for the DPLLs, input priority, and maximum TDC frequency.

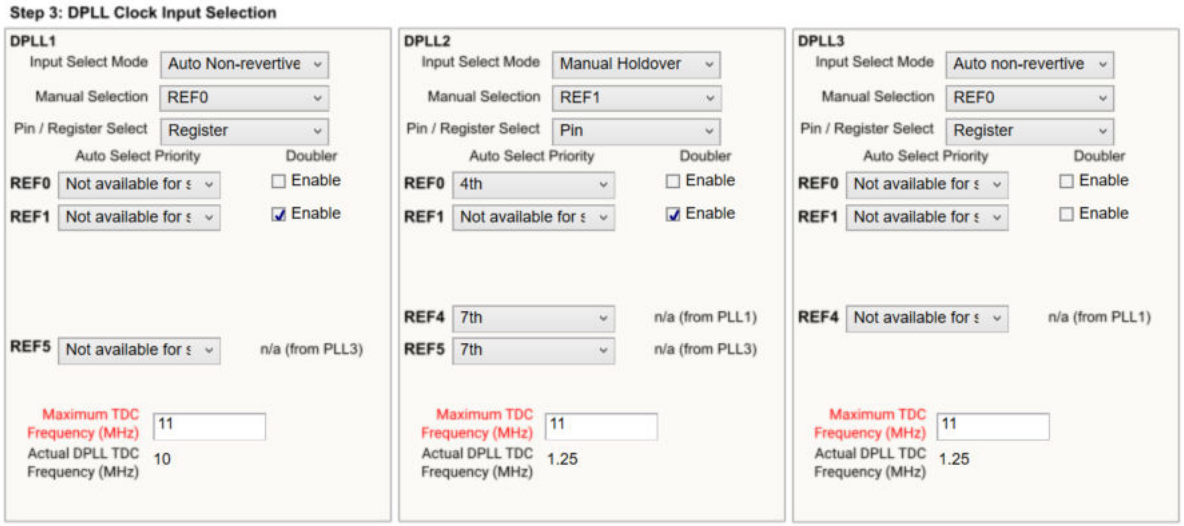

Figure 6-3. Step 3: DPLL Clock Input Selection

6.1.4 Step 4

Step 4 is currently not implemented for 0-Delay setup.

6.1.5 Step 5

Enter desired target frequencies for each of the outputs as well as desired output format, output source, whether the output is SYSREF, and whether the output is being used or not.

Press the *Calculate VCO Frequency Options* to generate a list of possible VCO frequency combinations.

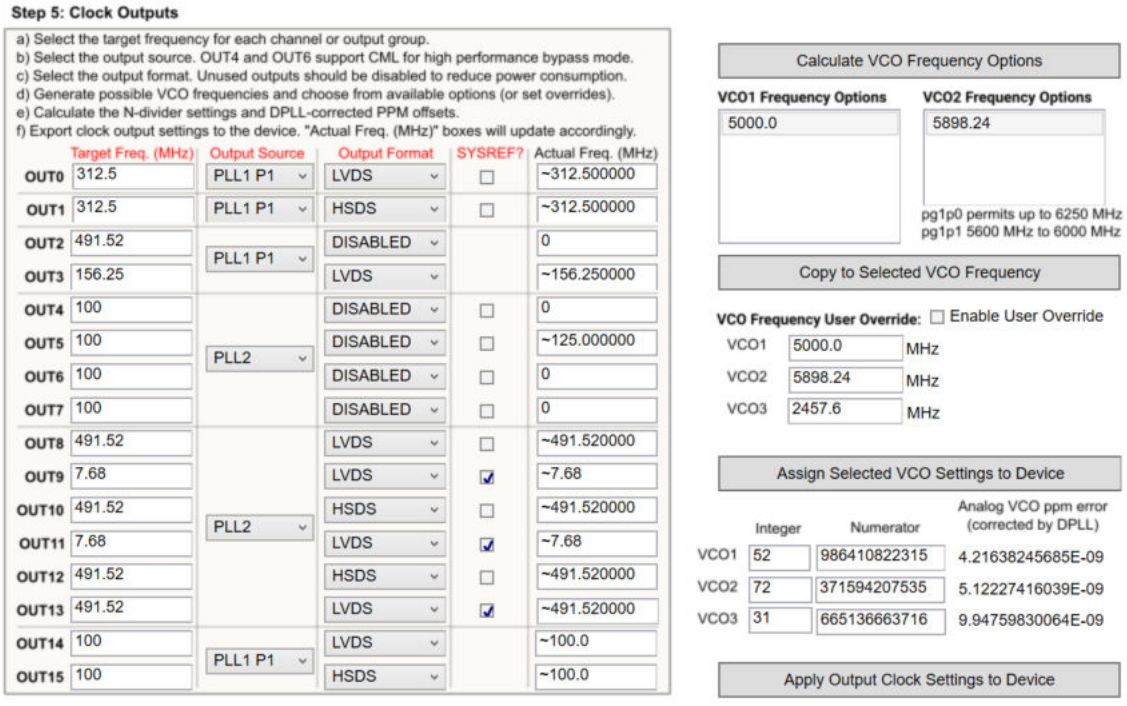

Figure 6-4. Step 5: Clock Outputs

Select a desired combination of VCO frequencies from the list of calculated values. If a specific VCO frequency is not in this list, a manual override can occur by selecting the *Enable User Override* check box and typing in the desired VCO frequencies. The *Copy to Selected VCO Frequency* box can also be used to copy the VCO frequency in the list selections to the VCO overrides.

Press the *Assign Selected VCO Settings to Device* to update the VCO frequencies. Press the *Apply Output Clock Settings to Device* button. By default, the analog PLL frequencies are shown; however the DPLL calculated frequency from step 6 will result in exact output frequencies.

6.1.6 Step 6

For step 6, enter the desired DPLL loop bandwidth.

Note: Any time an approximate symbol is shown, a tool tip will allow exact output frequency to be seen by mousing over the control.

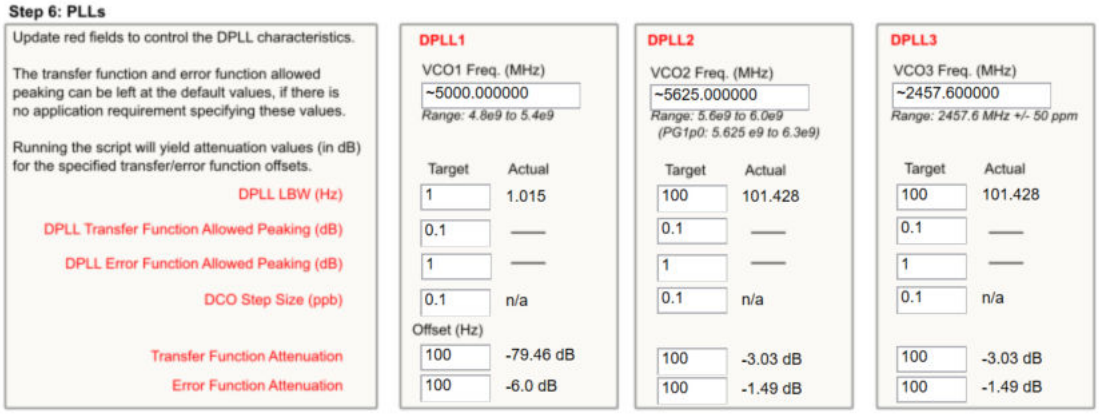

Figure 6-5. Step 6: PLLs

6.1.7 Step 7

To calculate the DPLL divider settings, select which DPLL loop filters and dividers to calculate and press the Run Script button. The software will now run and calculate the necessary settings.

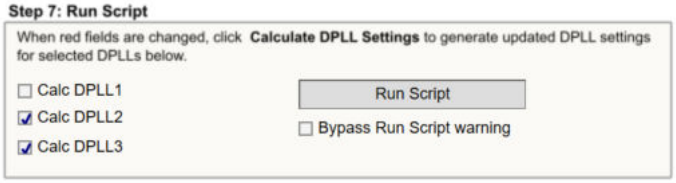

Figure 6-6. Step 7: Run Script

6.2 Using the Status Page

The status page shows fields pertaining to the current status of the device. The update these fields click the *Read Status Bits* button or the *Read RO Regs* button in the tool bar. The Read RO Regs button will read all read only registers which provides more information on other pages including the status fields but can take longer to read back. The read status bits just reads the status bits for this page.

For the DPLL to lock, a reference must be validated and selected as shown in the Active Reference/Holdover and Reference Validated portion of the window, as seen in the circled portion of Figure 6-7.

As the DPLL locks, it is expected to see the LOPL_DPLLx as the last bit to become clear when the phase lock is acquired.

When INT_EN = 1, any live status flag which occurs will latch to the INTR Latched bit columns. These will remain asserted until the *Clear Latched Bits* button is selected. This gives additional insight into the behavior of the device.

Pressing the Soft-chip reset button in the toolbar will cause the device to reset and re-start lock.

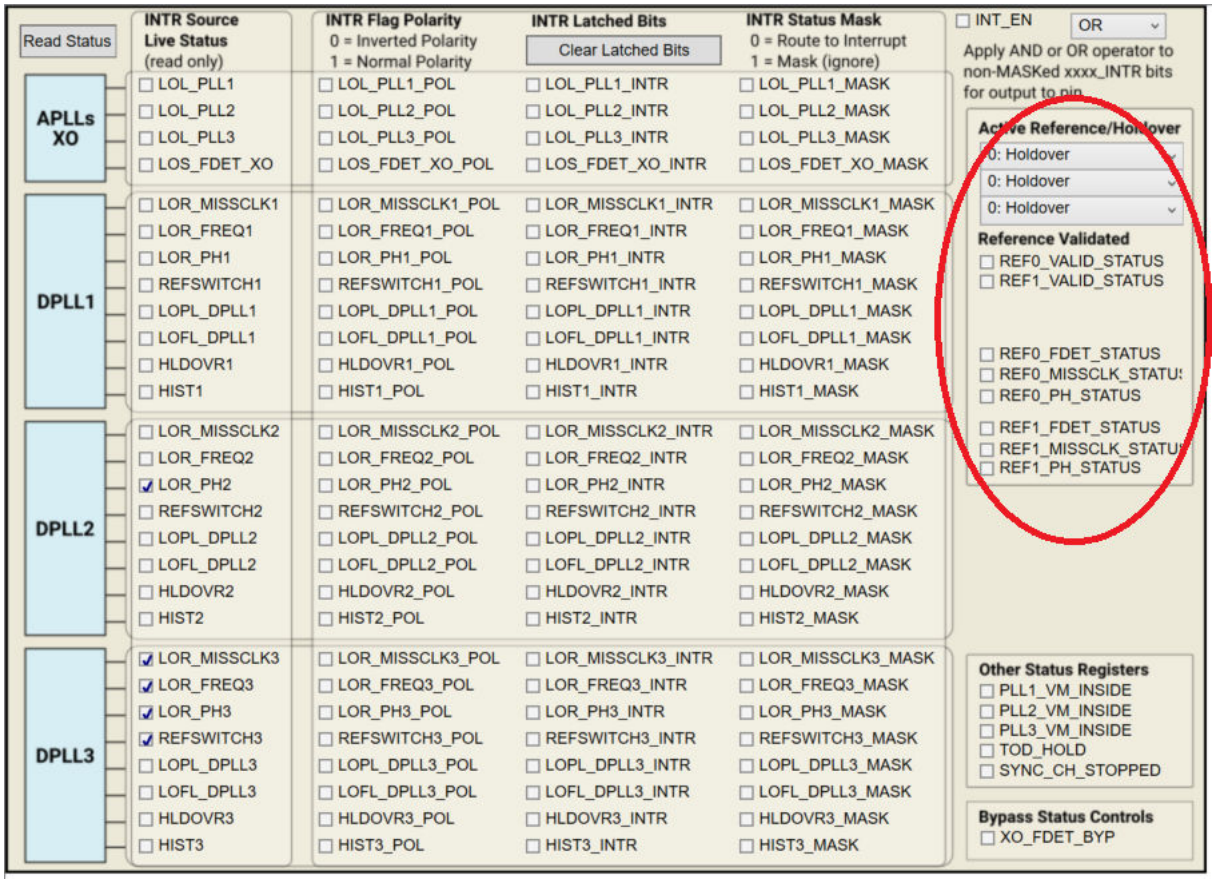

Figure 6-7. Status Page

6.3 Using the Input Page

The Input Page provides a high level view of all the inputs for the device, the APLL frequency, and DPLL frequency of the device.

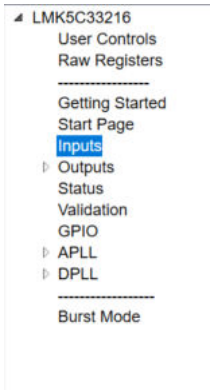

Figure 6-8. Inputs Location

Once the DPLL dividers and loop filter have been calculated by running the script in step 7 on the start page, this page displays the DPLL divider values which set the DPLL frequency. Here it is shown that the DPLL frequency is the exact desired frequency.

Each DPLL supports two sets of DPLL dividers which can be selected. At this time, the tool calculates the divider for FB Config 1 only. Div #1 settings may be copied into Div #2 settings and selected for use by the DPLL Div Select control.

On this page, it is possible to select the APLL frequency or DPLL frequency to propagate through to the outputs by changing APLL frequency to DPLL frequency.

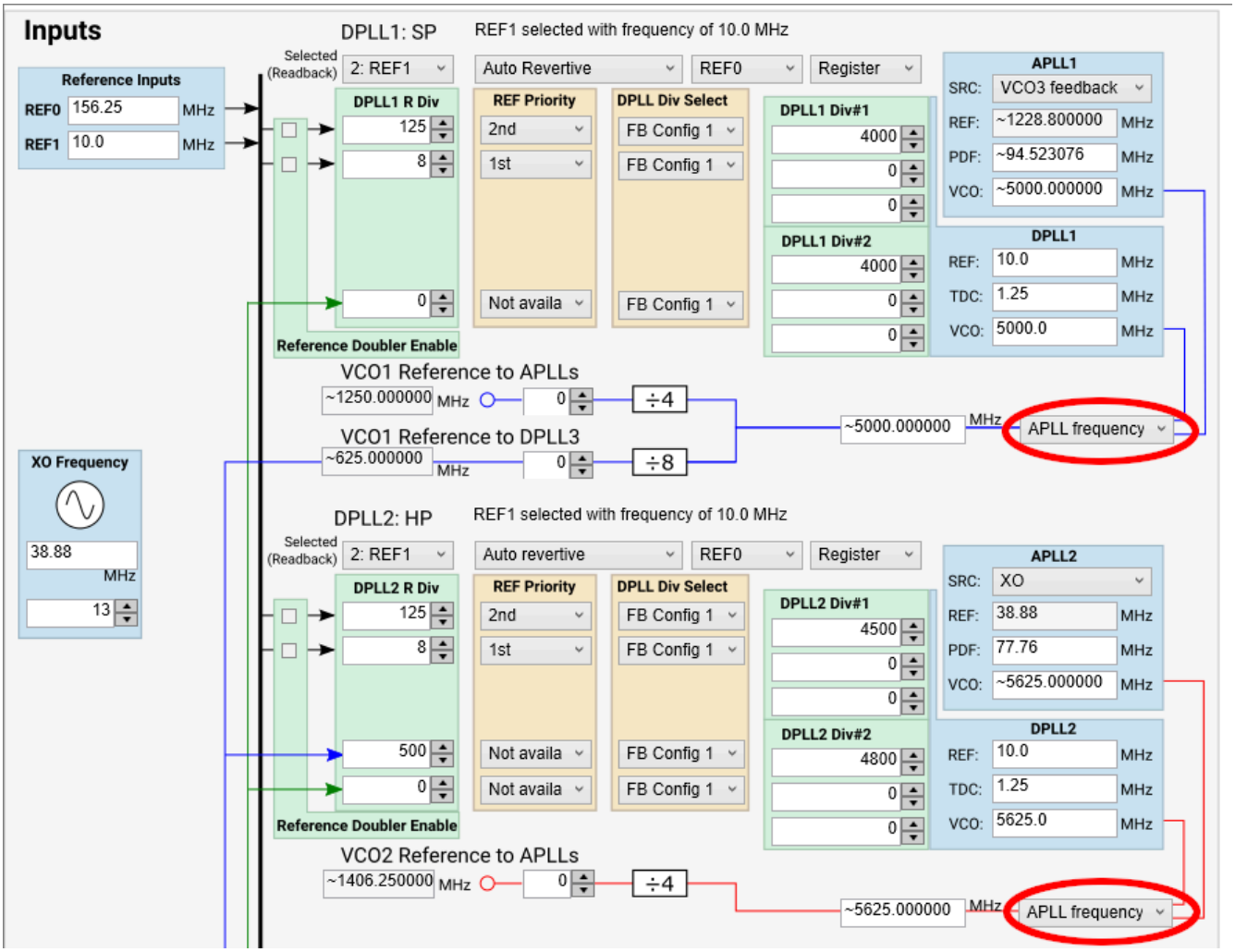

Figure 6-9. APLL or DPLL Frequency Selection

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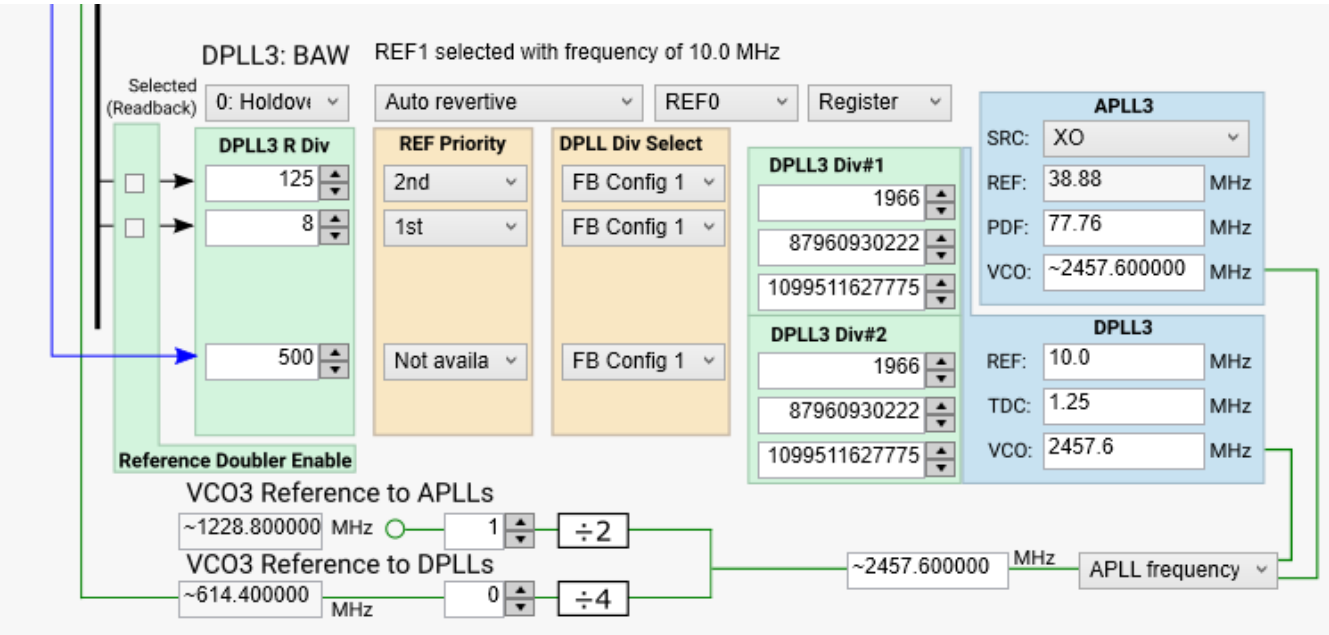

Figure 6-10. PLL3 Input

6.3.1 Cascaded Configurations

Cascaded configurations can be created using the input page, where the relevant VCO buffers and dividers will automatically be enabled by inferring the state of source selection registers.

At least one PLL must always be active and set to XO reference source for cascaded configurations to be valid. APLL start-up priority will automatically choose XO-source APLLs to start up before all other PLLs whenever possible. If in pin-selection mode, since start-up priority cannot be properly inferred, users must set this priority themselves in the User Controls page. In the example image below, APLL2 and APLL3 are referenced to XO input and APLL1 reference is from APLL3. Priority is controlled in ascending order, with 0 first and 2 last. APLLs can share priorities; if all APLL priorities are set to 0, all APLLs will startup simultaneously.

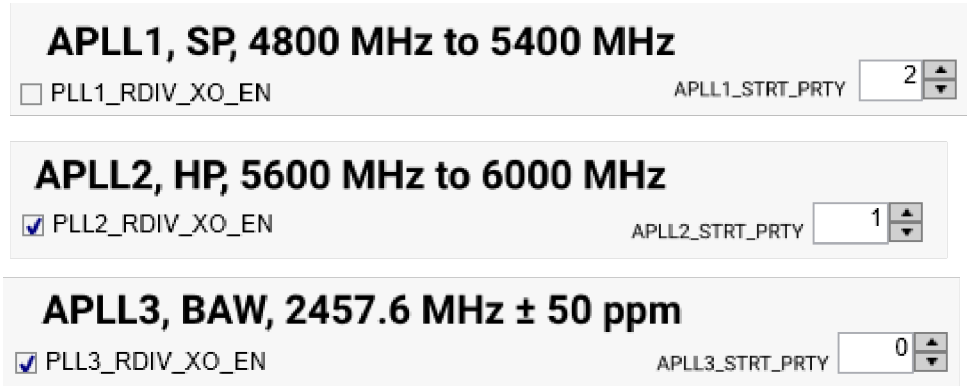

Figure 6-11. Cascade APLL Start Priorities

6.3.1.1 Cascade VCO to APLL Reference

Cascading APLLs is controlled by the APLL source box, circled in Figure 6-12. This box is programmed bitwise and is automatically set when generating a frequency plan. The XO_OUT_BUF_EN register in the *Input Control* section of the *User Controls* tab is automatically set to enable or disable the XO Output Buffer. The PLLx_RDIV_XO_EN is automatically checked/unchecked in each APLLx tab depending on whether each APLL is using the XO input.

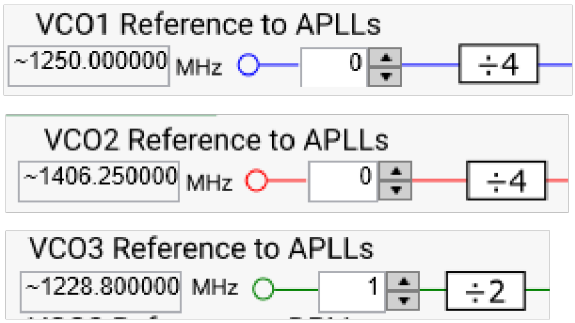

Figure 6-12. APLL Source Box

6.4 Using APLL1, 2, and 3 Pages

The APLL pages can be used to see detailed information on APLL behavior including the output dividers. It is possible to select between APLL frequency and DPLL frequency from this page to cascade to the output frequency boxes. By leaving **APLL frequency** (as shown in blue circle) selected, it is possible to type a VCO frequency into the PLL1 VCO frequency box (as shown in red circle) to have the fractional N value re-calculated.

When the DPLL is not used, the APLLs support an APLL only mode with a programmable 24-bit denominator. Support for this mode is currently not implemented in the TICS Pro software.

ADVANCE INFORMATION

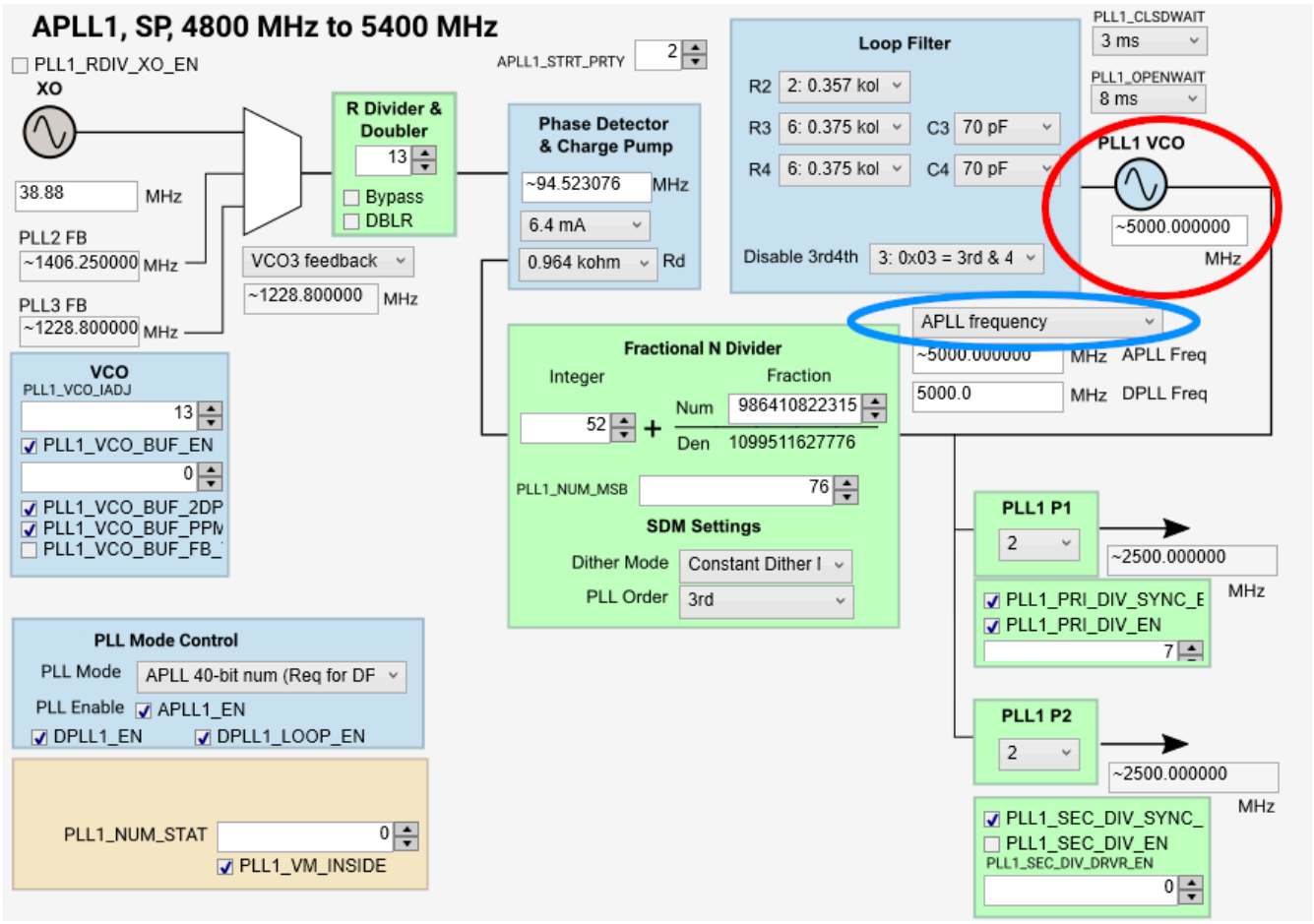

Figure 6-13. APLL1 Page

Figure 6-14 below shows the post dividers for PLL2 which includes PLL2 P2 for high speed open collector CML output, and below right shows the post dividers for PLL3 which includes PLL3 P1 with a CML MUX for bypassing BAW frequency directly to CML outputs or to be used with the PLL3 P1 divider for other outputs.

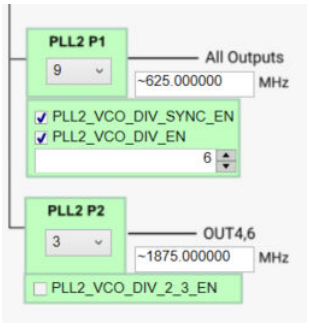

Figure 6-14. PLL2 Post Divider

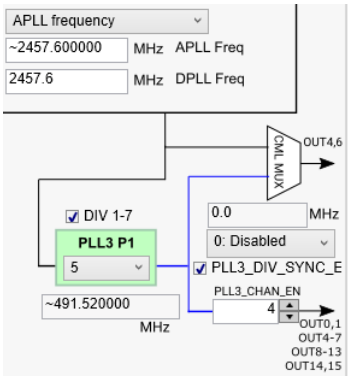

Figure 6-15. PLL3 Dividers

6.5 Using the DPLL1, 2, and 3 Pages

The DPLL pages contain many advanced controls that are normally set during the *Run Script* calculation. They also contain the DCO Shift control in the top left.

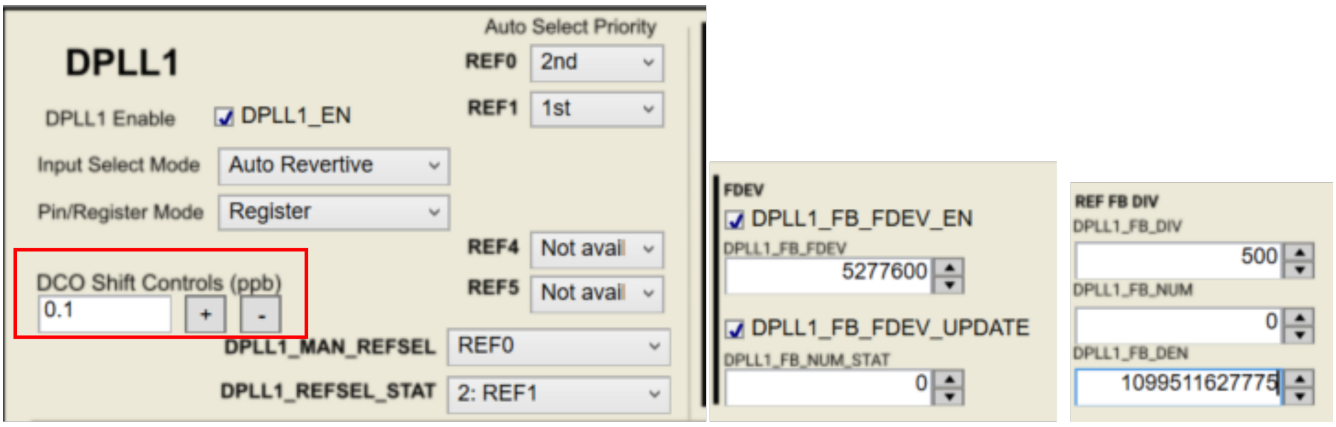

Figure 6-16. Primary DPLL Controls

6.5.1 DPLL DCO

To use the DCO shift controls on a given DPLL, enter the DCO ppb step value into the *DCO Shift Controls (ppb)* box shown above.

6.6 Using the Validation Page

The validation page allows the user to enable/disable different detectors for reference validation along with DPLL frequency and phase lock requirements.

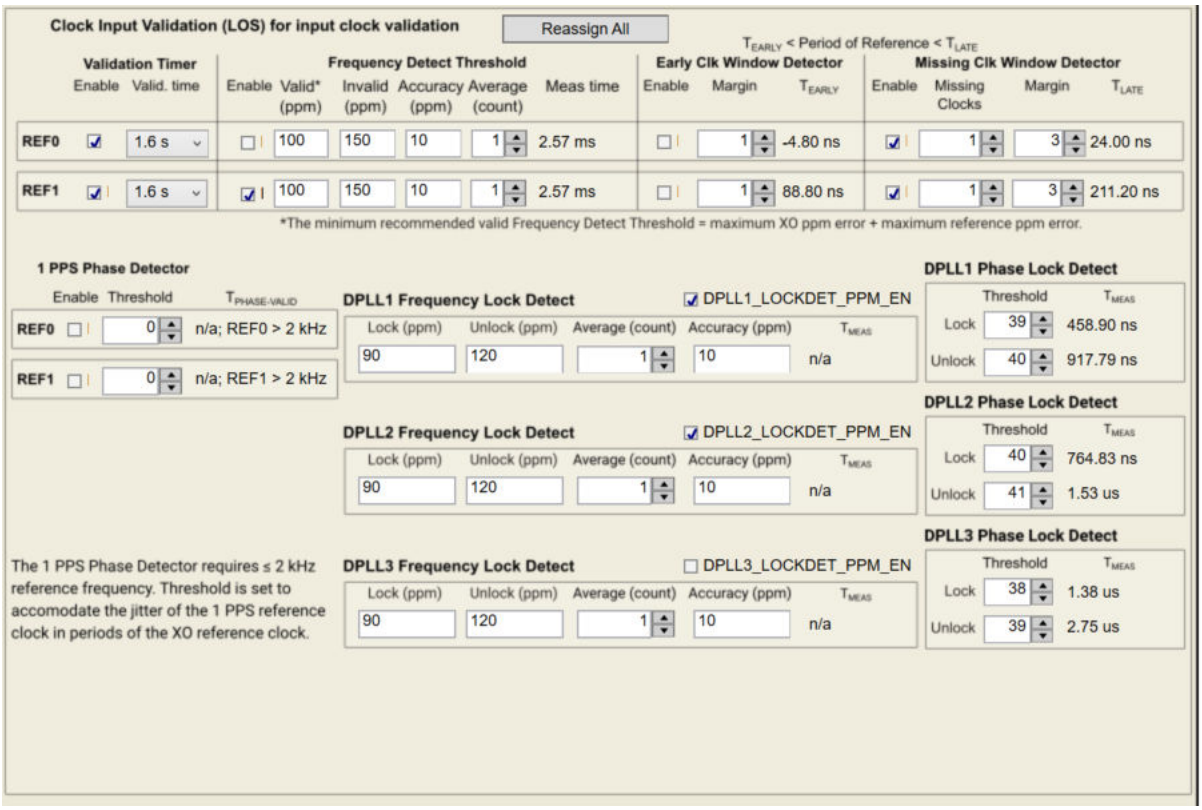

Figure 6-17. Validation Page

6.7 Using the GPIO Page

Allows configuring GPIO0, 1, and 2.

When using SPI readback on the EVM, GPIO2 must be configured as *STATUS or INT…* and *SDO output.* Refer to Section 3.3.

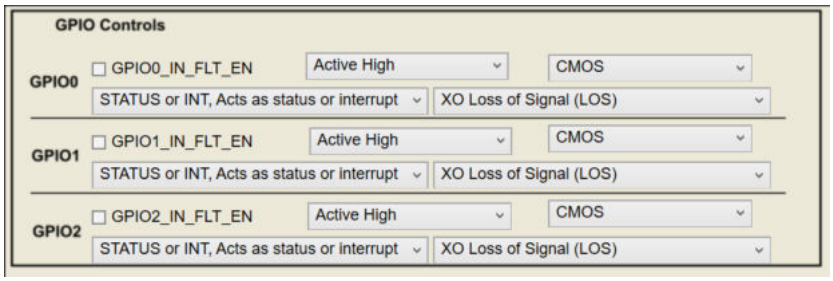

Figure 6-18. GPIO Page

6.8 Using the Outputs Page

The outputs page shows all the possible source frequencies to the output channels. To simplify settings fields necessary to providing an output frequency, a source mux lists all possible sources for each output. Be sure to enable/disable desired outputs at right hand side.

There are many detailed output pages beneath the Outputs page illustrated below showing individual controls for each set of outputs.

The black line between OUT2 to OUT3, OUT4 to OUT7,OUT8 to OUT13, and OUT14 to OUT15 signifies that all these outputs should source from the same VCO.

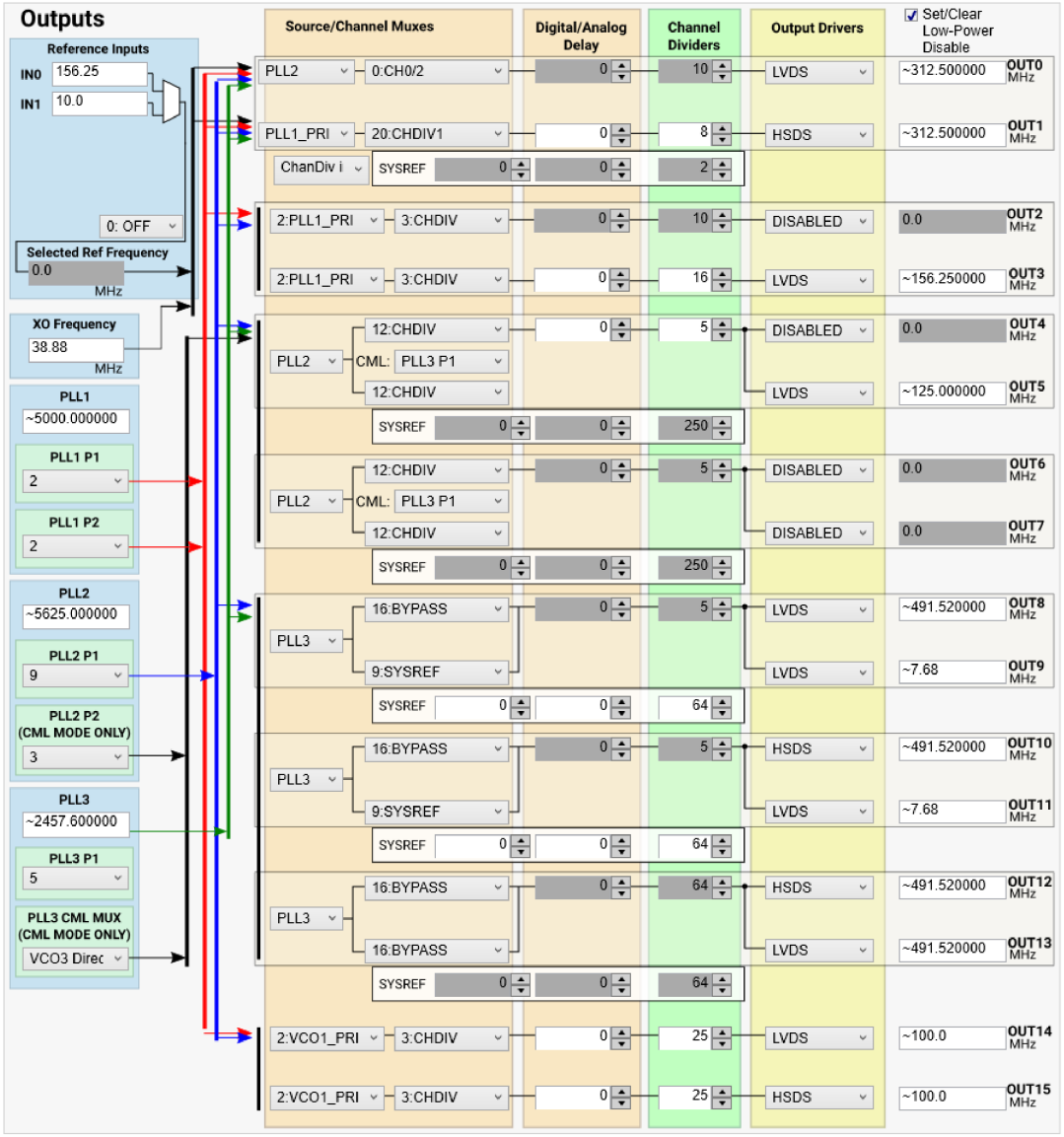

Figure 6-19. Outputs Page

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2020) to Revision A (February 2021)	Page
• Updated Power Supplies image	14
• Updated Power Distribution image	15
• Updated LMK5C33216 and Input Reference Inputs IN0 to IN1 image	16
• Updated Clock Outputs OUT0 to OUT3 image	17
• Updated Clock Outputs OUT4 to OUT9 image	18
• Updated Clock Outputs OUT10 to OUT15 image	19
• Updated XO Schematic image	20
• Updated Logic I/O Interfaces image	21
• Updated USB MCU image	22

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