

LMK04616 Evaluation Module

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Overview

The LMK04616EVM features LMK04616 ultra-low noise and low power JESD204B compliant Dual Loop Jitter Cleaner. With a power consumption of only 1200 mW with all outputs running, LMK04616 supports 65-fs jitter (12 kHz to 20 MHz) using a low-noise VCXO module. Integrated LDOs provide high PSRR that enables the use of DC-DC converters.

The dual loop architecture consists of two high-performance phase-locked loops (PLL), a low-noise crystal oscillator circuit, and a high-performance voltage controlled oscillator (VCO). The first PLL (PLL1) provides a low-noise jitter cleaner function while the second PLL (PLL2) performs the clock and SYSREF generation. PLL1 can be configured to either work with an external VCXO module or the integrated crystal oscillator with an external tunable crystal and varactor diode. When used with a very narrow loop bandwidth, PLL1 uses the superior close-in phase noise (offsets below 50 kHz) of the VCXO module or the tunable crystal to clean the input clock. The output of PLL1 is used as the clean input reference to PLL2 where it locks the integrated VCO. The loop bandwidth of PLL2 can be optimized to clean the far-out phase noise (offsets above 50 kHz) where the integrated VCO outperforms the VCXO module or tunable crystal used in PLL1.

Features

- Dual Loop Architecture with typical 60-fs rms from 10 kHz to 20 MHz at 122.88-MHz output frequency
- 1.2-W typical power consumption for 16 outputs at 122.88 MHz
- JEDEC JESD204B Support
- Jumper configurable supplies with onboard LDOs and DCDC converters
- GUI platform for full access to device registers

Quick Start Guide

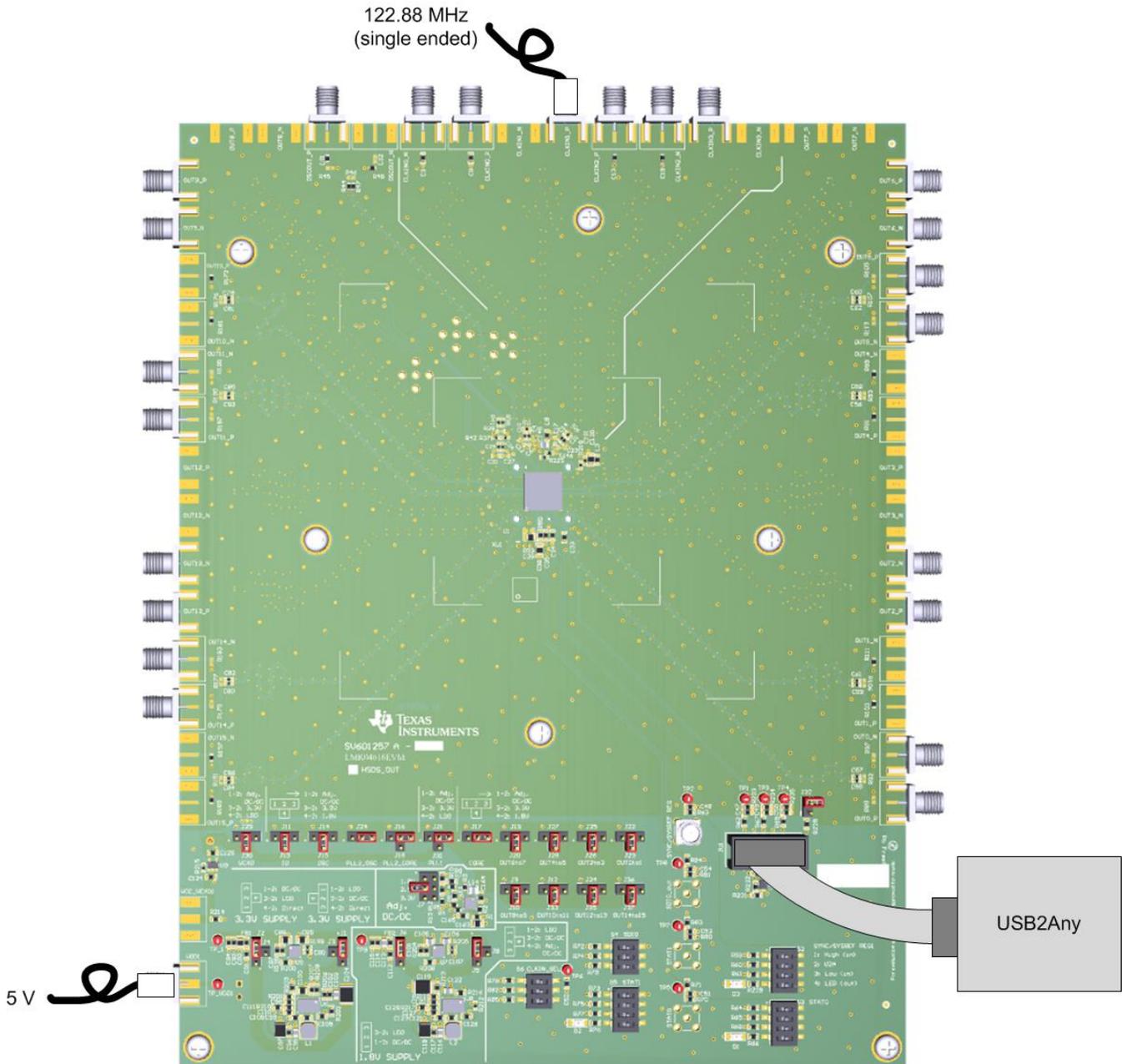


Figure 1. LMK04616 EVM Quick Start Connection

1 Quick Start Description

The LMK04616 EVM allows full verification of the device functionality and performance specification. To quickly set up and operate the board with basic equipment, refer to the quick start procedure below and test setup shown in [Figure 1](#).

1. Place Dip switches S1 to S5 into default position as shown in [Table 5](#)
2. Connect a supply voltage of 5 V to the VCC SMA.
3. Connect a reference clock to the CLKin1 port from a signal generator or other source. Use 122.88 MHz for default.
4. Connect the SPI header to a computer using USB2ANY.
5. Program the device with TICS Pro.
 - (a) Start TICS Pro
 - (b) Select LMK04616 from *Select device* → *Clock Generator/Jitter Cleaner (Dual Loop)* → *LMK0461x* Menu.
 - (c) Select from *USB Communications* → *Interface* Menu USB2ANY.
 - (d) Select default mode from the “Default Configuration” Menu. For the quick start use *Dual Loop: PLL1 BW= 40Hz REF: CLKin1 (single-ended)*
 - (e) Ctrl-L must be pressed at least once to load all registers. Alternatively click menu *Keyboard Controls* → *Load Device*.
 - (f) Click *Device Start* button in the *Generic* page or use the *Device: DEV_STARTUP* button from the Tool bar.
6. Measurements may be made at an active CLKout port through its SMA connector.

2 1.2 Device Start-Up Sequence

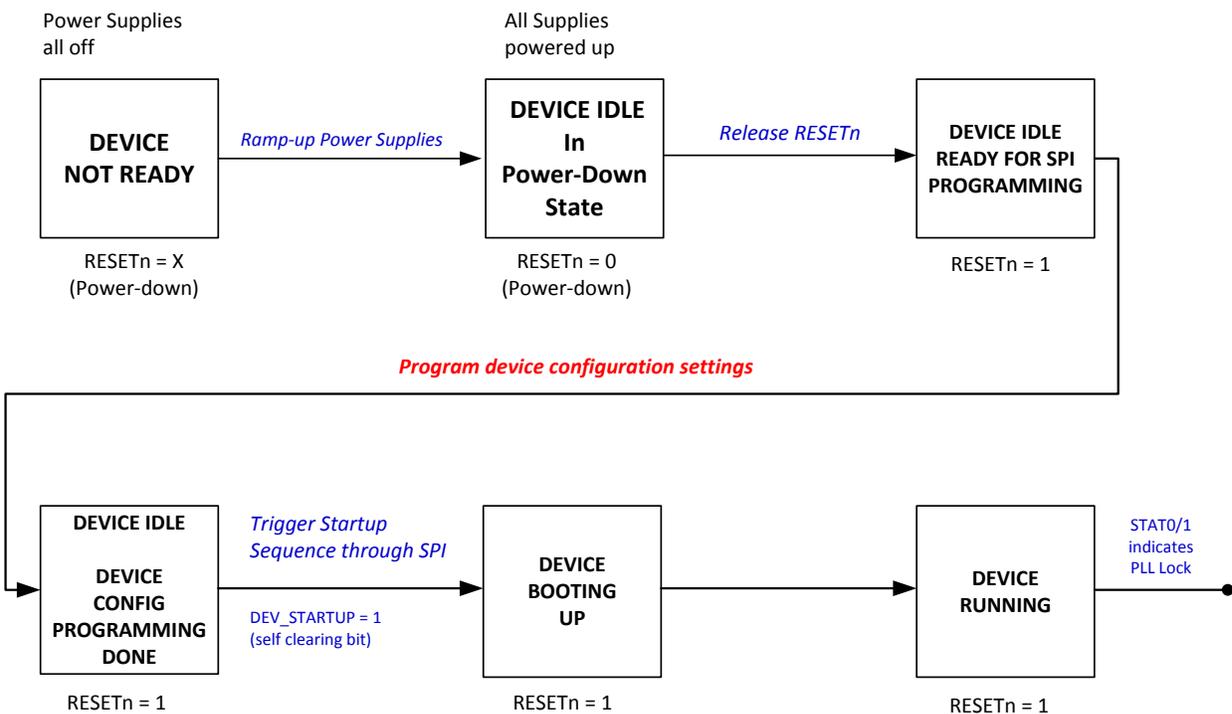


Figure 2. Device Start-Up Sequence

Installing the EVM Control Software

1. Install latest TICS Pro software from web: <http://www.ti.com/tool/ticspro-sw>
2. Start TICS Pro.
3. Select Device → Clock Generator/Jitter Cleaner (Dual Loop) → LMK0461x → LMK04616

Using the EVM Control Software

- 1 **Keyboard Shortcuts**
CTRL + L => write all registers
- 2 **TICS Pro Overview**

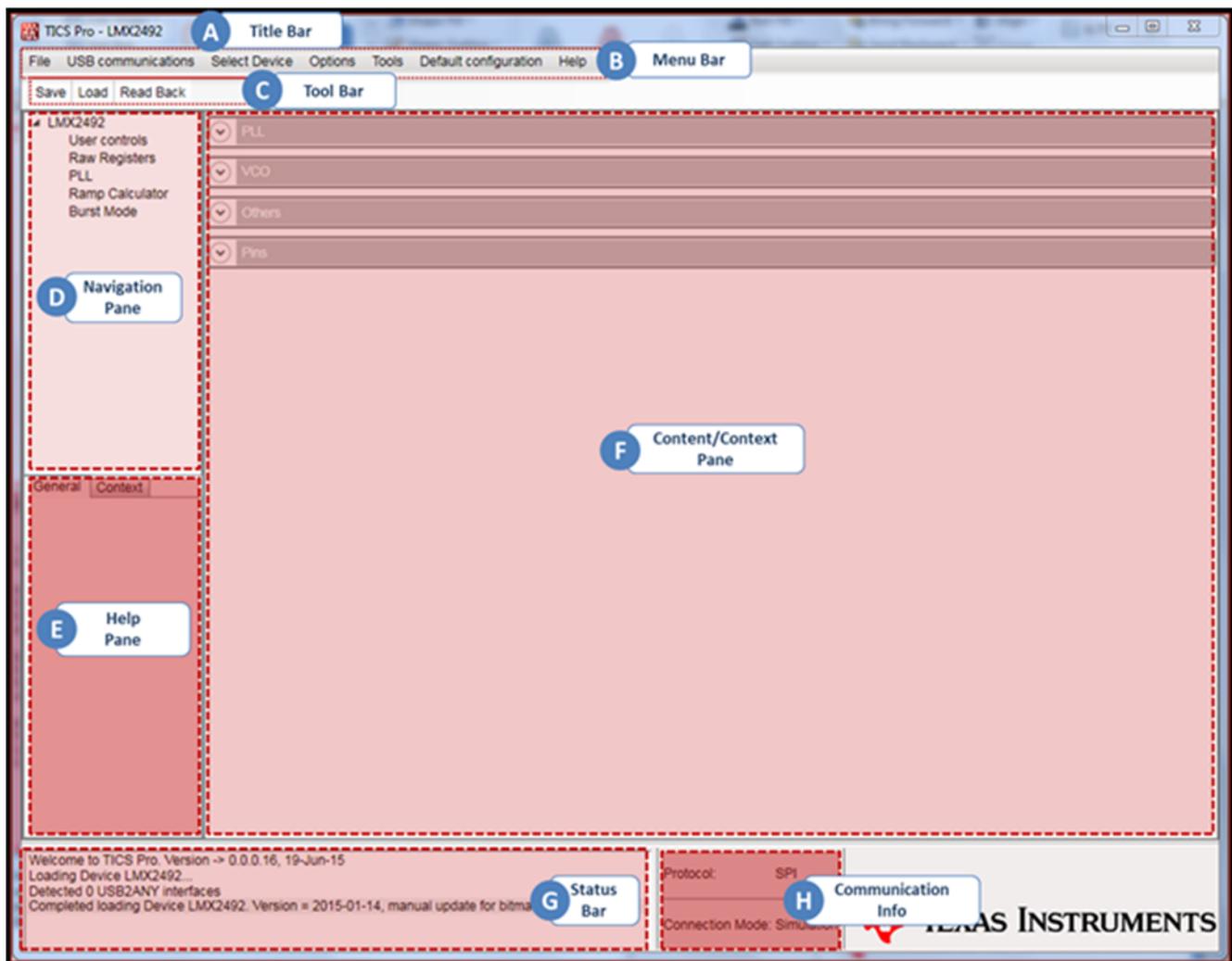


Figure 3. TICS Pro Overview

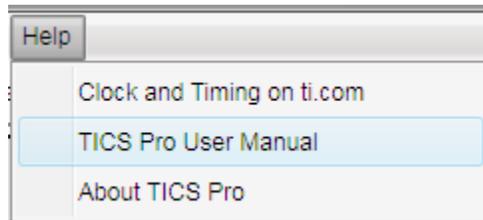


Figure 4. TICS Pro User Manual

Further information at Help → TICS Pro User Manual

3 TICS Pro With LMK04616 GUI Loaded

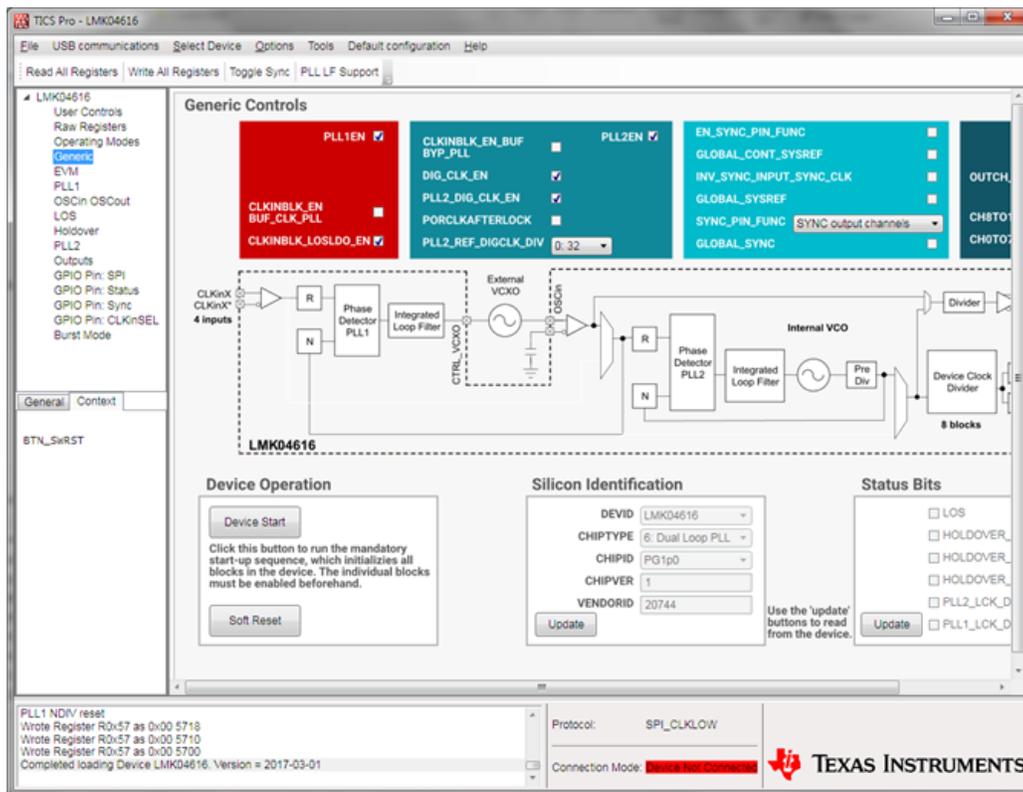


Figure 5. TICS Pro With LMK04616 GUI Loaded

4 GUI: Generic Control

Generic Controls

PLL1EN <input checked="" type="checkbox"/> CLKINBLK_EN_BUF_CLK_PLL <input type="checkbox"/> CLKINBLK_LOSLDO_EN <input checked="" type="checkbox"/>	CLKINBLK_EN_BUF_BYP_PLL <input type="checkbox"/> DIG_CLK_EN <input checked="" type="checkbox"/> PLL2_DIG_CLK_EN <input checked="" type="checkbox"/> PORCLKAFTERLOCK <input type="checkbox"/> PLL2_REF_DIGCLK_DIV <input type="text" value="0.32"/>	PLL2EN <input checked="" type="checkbox"/> EN_SYNC_PIN_FUNC <input type="checkbox"/> GLOBAL_CONT_SYSREF <input type="checkbox"/> INV_SYNC_INPUT_SYNC_CLK <input type="checkbox"/> GLOBAL_SYSREF <input type="checkbox"/> SYNC_PIN_FUNC <input type="text" value="SYNC output channels"/> GLOBAL_SYNC <input type="checkbox"/>	OUTCH_MUTE <input type="checkbox"/> CH8T015EN <input checked="" type="checkbox"/> CH0T07EN <input checked="" type="checkbox"/>
--	--	---	--

LMK04616

Device Operation

Click this button to run the mandatory start-up sequence, which initializes all blocks in the device. The individual blocks must be enabled beforehand.

Silicon Identification

DEVID:

CHIPTYPE:

CHIPID:

CHIPVER:

VENDORID:

Use the 'update' buttons to read from the device.

Status Bits

LOS

HOLDOVER_DLD

HOLDOVER_LOL

HOLDOVER_LOS

PLL2_LCK_DET

PLL1_LCK_DET

Figure 6. GUI: Generic Control

5 GUI: Operating Modes

Operating Modes Each of the buttons next to a block diagram ensures that the internal paths are enabled as illustrated with the color coding.

Please ensure that the PLL loop can be closed by setting the reference and feedback dividers appropriately on the 'PLL1' and 'PLL2' pages. By default CLKIn1 is selected.

<p>Dual Loop</p> <p>Normal Dual Loop OscOut = OscIn</p>	<p>Dual Loop</p> <p>Normal Dual Loop OscOut = PLL2 Output</p>	
<p>Single Loop PLL1</p> <p>PLL1 Single Loop OscOut = OscIn</p>	<p>Single Loop PLL1</p> <p>PLL1 Single Loop OscOut = PLL1 Output</p>	
<p>Single Loop PLL2</p> <p>PLL2 Single Loop Ref=CLKInX OscOut = OscIn</p>	<p>Single Loop PLL2</p> <p>PLL2 Single Loop Ref=OscIn OscOut = PLL Output</p>	
<p>Single Loop PLL2</p> <p>PLL2 Single Loop Ref=OscIn OscOut = OscIn</p>	<p>Single Loop PLL2</p> <p>PLL2 Single Loop Ref=CLKInX OscOut = PLL Output</p>	
<p>Bypass 2A</p> <p>Mode 2A Bypass OSCIn- > CLKOutX OscOut = PLL bypass</p>	<p>Bypass 1</p> <p>Mode 1 Bypass CLKInX- > CLKOutX OscOut = PLL bypass</p>	<p>Bypass 2B</p> <p>Mode 2B Bypass OSCIn- > CLKOutX OscOut = OscIn</p>

Figure 7. GUI: Operating Modes

6 GUI: OSCin and OSCout

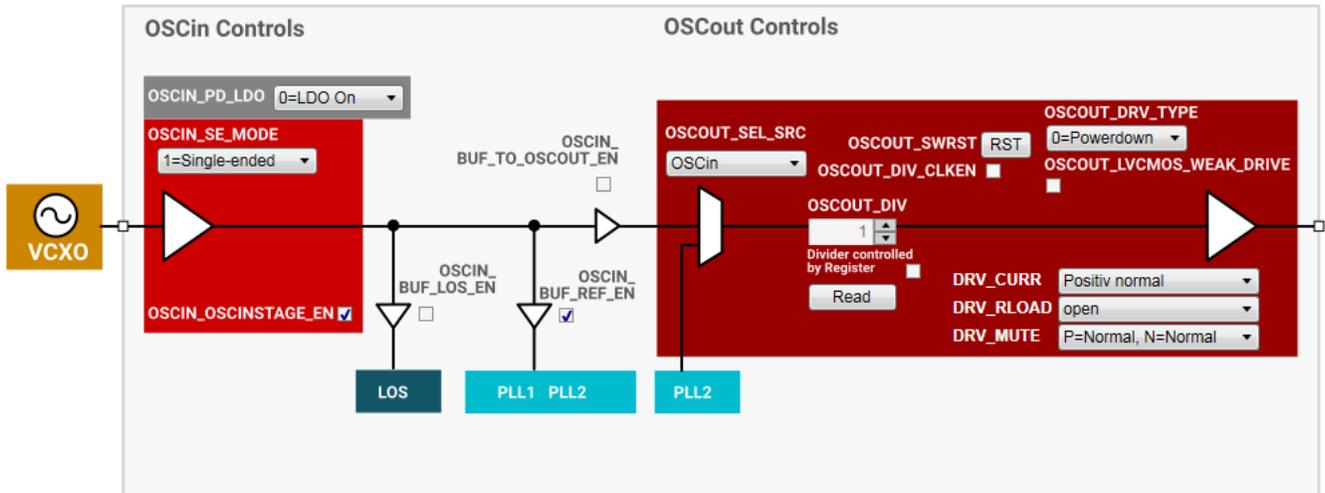


Figure 8. GUI: OSCin and OSCout

7 GUI: LOS Control

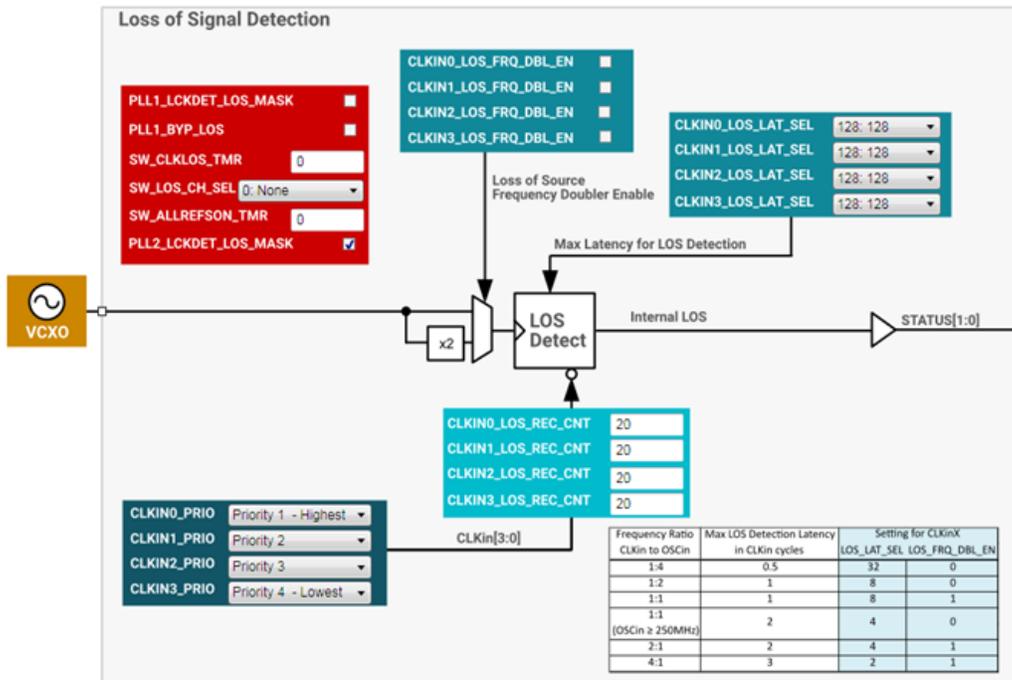


Figure 9. GUI: LOS Control

8 GUI: Holdover Control

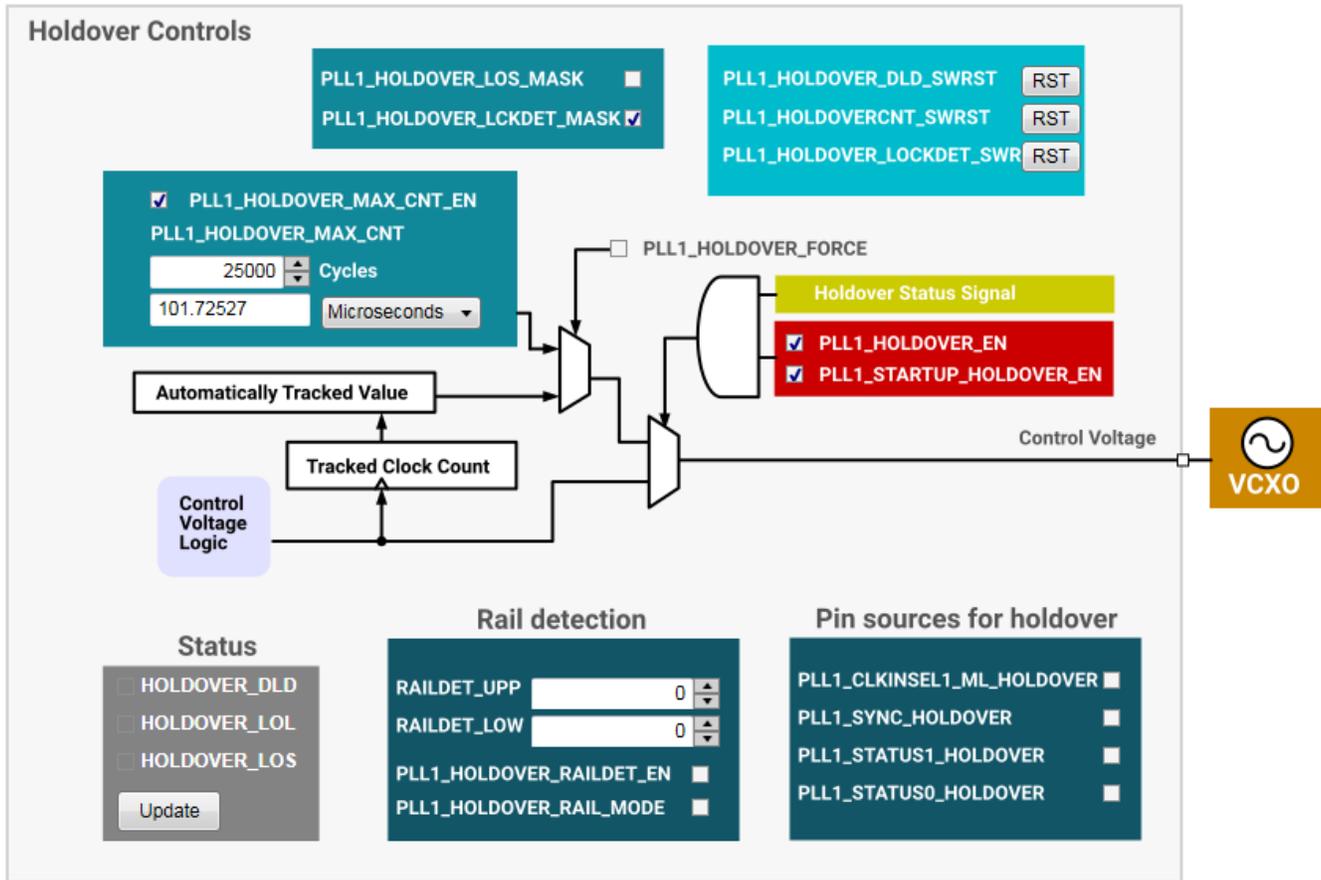


Figure 10. GUI: Holdover Control

9 GUI: Inputs and PLL1

PLL1 Control

MHz Input Buffers Dividers Inversion MHz Reference Mux

122.88 CLKIN0_EN CLKIN0_PLL1_RDIV CLKIN0_INVERSION 1.92 CLKINBLK_ALL_EN

122.88 CLKIN1_EN CLKIN1_PLL1_RDIV CLKIN1_INVERSION 1.92 CLKINSEL1_MODE

122.88 CLKIN2_EN CLKIN2_PLL1_RDIV CLKIN2_INVERSION 1.92 SW_REFINSEL

122.88 CLKIN3_EN CLKIN3_PLL1_RDIV CLKIN3_INVERSION 1.92 CLKINSEL1_INV

122.88 CLKIN3_EN CLKIN3_PLL1_RDIV CLKIN3_INVERSION 1.92 CLKMUX

PLL1_STORAGE_CELL: 0
Read storage cell

The read back storage cell value provides an indication of the level of the analog tuning voltage for the external VCXO.

Charge Pumps

Integral Final: 1, Fast Lock: 1

Proportional Final: 8, Fast Lock: 255

PLL1_EN REGULATION

PLL1_DIR_POS_GAIN: 1=Negative

122.88 MHz VCXO

PLL1_RDIV_CLKEN PLL1_RDIV_SWRST RST

PLL1_NDIV: 64, FBCLK INVERSION

PLL1_NDIV_CLKEN PLL1_NDIV_SWRST RST

1.024 MHz

PLL1_SWRST RST

FN	FVOID	PLL1_RDIV	PLL1_NDIV	PROP MODE	PLL1_PROP	PLL1_INTG	C3
122.88 MHz	122.88 MHz	100	100	Low Pulse Mode	2	0	4.7 μ F
122.88 MHz	122.88 MHz	100	100	Low Pulse Mode	10	0	4.7 μ F
122.88 MHz	30.72 MHz	100	25	Low Pulse Mode	2	0	4.7 μ F
122.88 MHz	30.72 MHz	100	25	Low Pulse Mode	10	0	4.7 μ F

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Lock Detection

Window Comparator

PLL1_LD WNDW_SIZE: 63 ns

PLL1_FAST LOCK

PLL1_LCKDET_BY_32

PLL1_PD_LD

PLL1_LOCKDET CYC_CNT: 16384

CLKIN_STAGGER_EN Disable RDIV/NDIV

CLKIN_SWRST 50% Duty Cycle CLK Output

PLL1_LOL_NORESET

PLL1_RC_CLK_EN

PLL1_RC_CLK_DIV: 7

PLL1_F_30: 0=122MHz

PLL1_LDO_WAIT_TMR: 0

Figure 11. GUI: Inputs and PLL1

10 GUI: PLL2

PLL2 Controls

PLL1 BYPASS
 MHz: 122.88
 OSCin CLK
 PLL2 CLKin

PLL2_REF_CLK_EN
 x2
 DIV: 1
 Doubler, inv.

PFD + LD
 245.76 MHz
 PLL2_LD WNDW_SIZE: 2 ns
 PLL2_LOCKDET CYC_CNT: 16384
 PFD_DIS SAMPLE
 PROG_PFD_RESET
 PLL2_PD_LD
 PLL2_SWRST RST

Charge Pumps
 PLL2_PROP: 20
 VCO: 5898.24 MHz
 PLL2 INTEGRAL INIT VALUE: 511=Cell 9
 PLL2 INTEGRAL GAIN: 10

Pre-Scaler
 PLL2_PRESCALER_TOP: DIV6
 PLL2_VCO_PRESC LOW_POWER

Other PLL2 Controls:
 PLL2_FB DIV: Feedback
 OUTCH_CH6
 OUTCH_CH5
 PLL2_NBYPASS_DIV2_FB: DIV2
 PLL2_NDIV: 4
 PLL2_NDIV_SWRST
 PLL2_NDIV_CLKEN

F _{IN} PLL2	F _{VDD}	PLL2_RDIV	PLL2_NDIV	PRESCALER	INPUT MODE	PLL2_PROP	PLL2_INTG	PLL2_CPROP	R3, C3 ⁽¹⁾
122.88 MHz	5898.24 MHz	1	4	6	Doubler Invert	20	0	5.4 pF	disabled, 0 pF
122.88 MHz	5898.24 MHz	1	4	6	Doubler Invert	21	0	5.4 pF	4.7 kΩ, 96 pF
30.72 MHz	5898.24 MHz	1	16	6	Doubler Invert	20	0	5.4 pF	disabled, 0 pF
30.72 MHz	5898.24 MHz	1	16	6	Doubler Invert	7	0	5.4 pF	4.7 kΩ, 96 pF

Charge Pump

- PLL2_CFLT_64
- PLL2_CFLT_32
- PLL2_CFLT_16
- PLL2_CFLT_8
- PLL2_CFLT_4
- PLL2_EN_FILTER
- PLL2_CSAMPLE: 4.85 pF
- PLL2_RFILT
- PLL2_CP_EN_SAMPLE_BYP
- PLL2_CPROP: 3.0 pF

PLL2_LD WNDW_SIZE_INITIAL: 2 ns
PLL2_LOCKDET_CYC_CNT_INITIAL: 16384
PLL2_AC_REQ RST

Enable Bypass Buffer
 PLL2_SYNC_BOTTOM
 PLL2_SYNC_TOP
 PLL2_BYPASS
 PLL2_BOTTOM
 PLL2_TOP

E-Mail Support @ TI

Figure 12. GUI: PLL2

11 GUI: Outputs

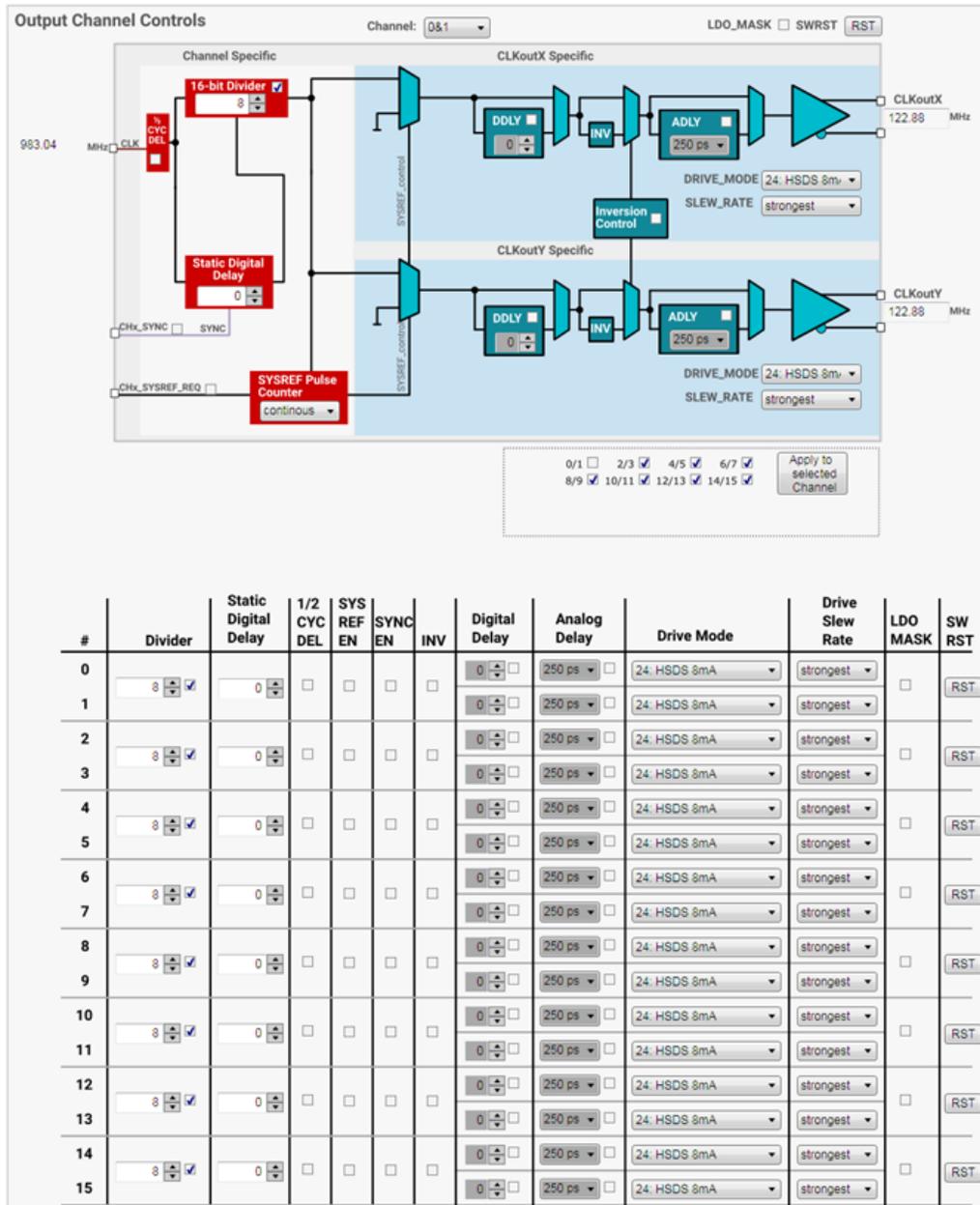


Figure 13. GUI: Outputs

12 GUI: EVM

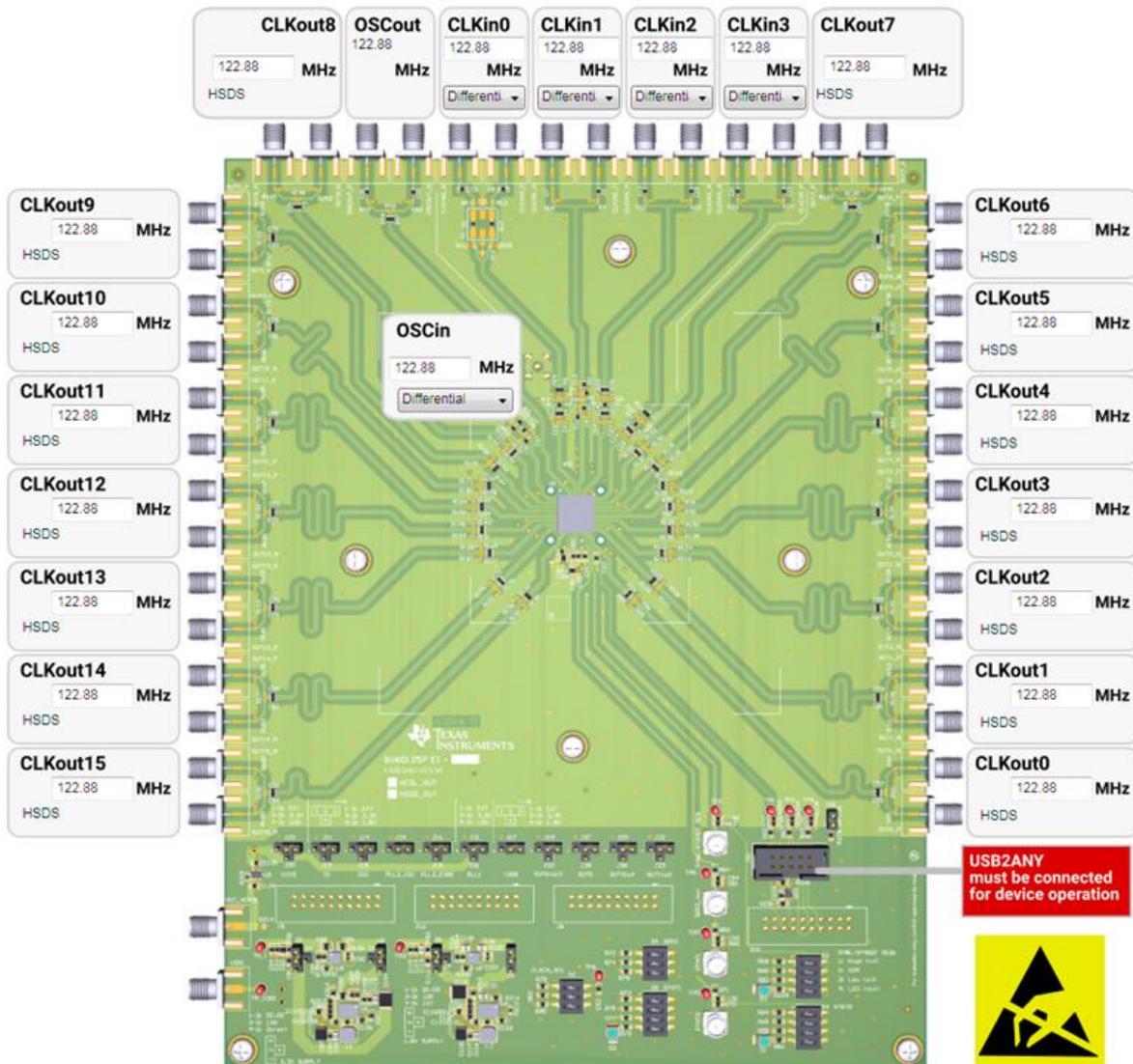


Figure 14. GUI: EVM Overview

Configuring the Board

The LMK04616 is a programmable clock jitter cleaner with many options. The EVM was designed with maximum flexibility so engineers can configure the EVM for operation at its desired mode.

Figure 15 shows the connection concept of the LMK04616EVM.

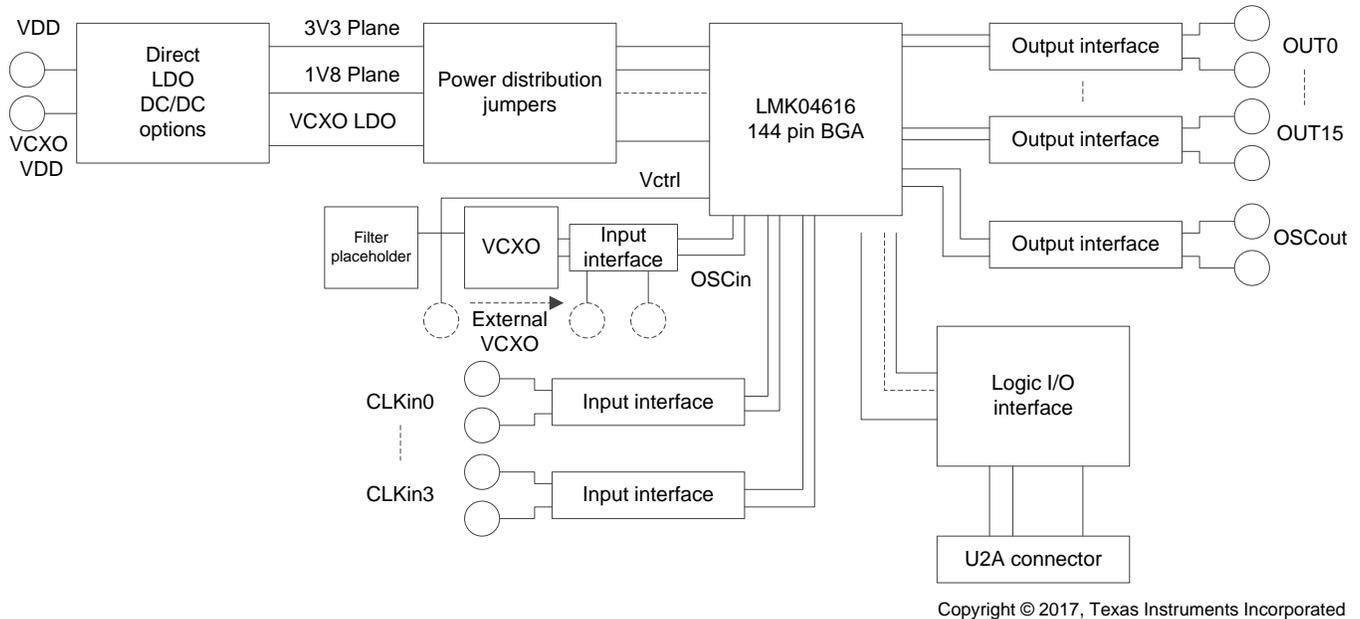


Figure 15. EVM Connection Concept

1 Configuring the Power Supply

Figure 16 shows the default jumper setting to supply 3.3 V and 1.8 V to the device.

The VDD SMA or VDD_2 terminal block (on the back side of the EVM) is connected to J1 and J5 to provide the external supply voltage for the 3.3-V and 1.8-V supply plane.

The VDD_VCXO SMA is directly connected to the VCXO LDO.

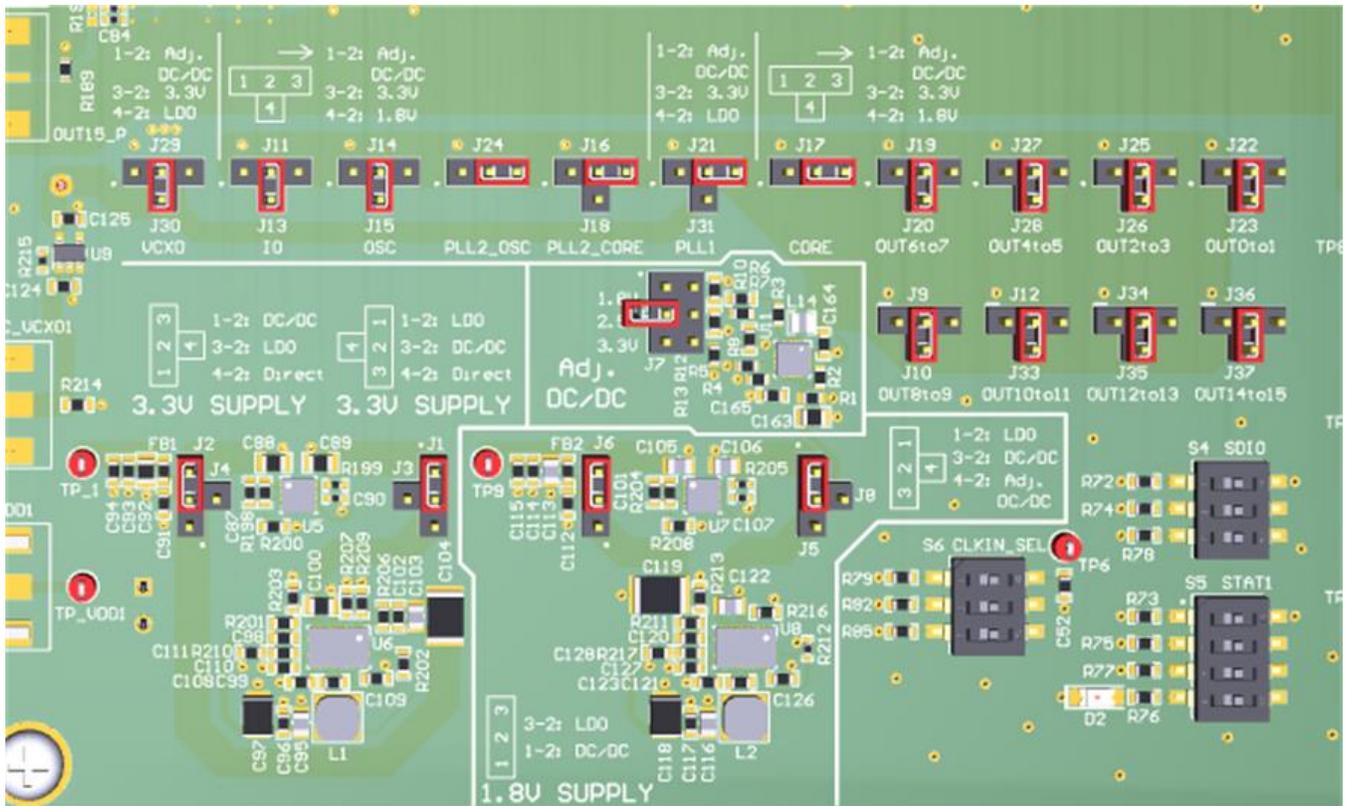


Figure 16. Default Power Supply Connection

1.1 Supply Plane Source Selection

Jumper J1 and J2 selects the Power connection for the 3.3-V plane from either the LDO, a DC-DC switcher or direct from VDD SMA Connector.

Table 1. 3.3-V Supply Plane Connections

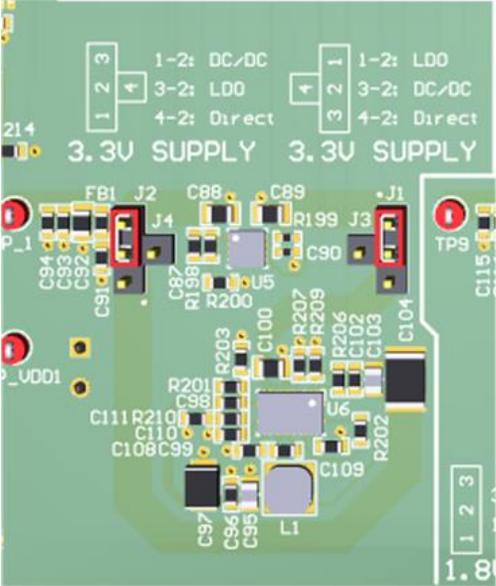
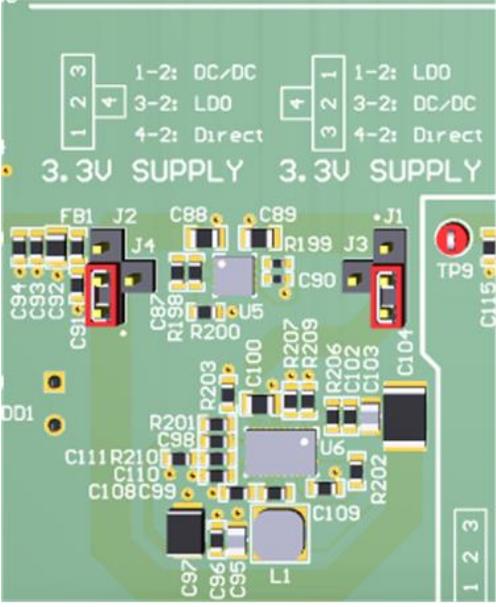
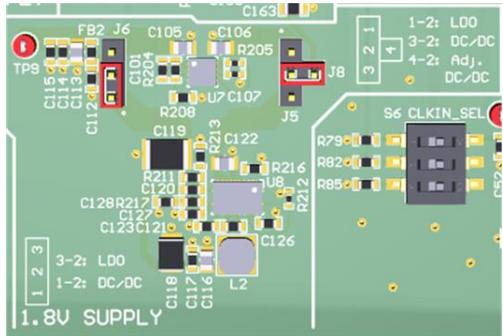
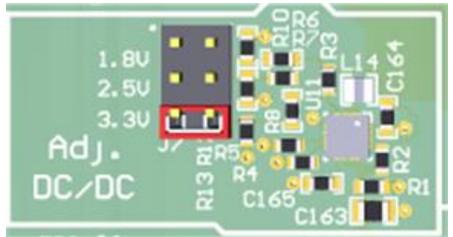
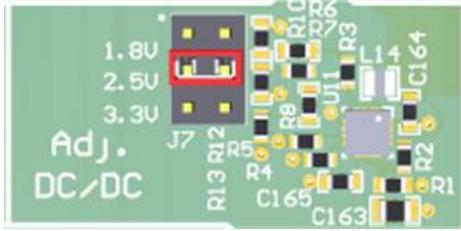
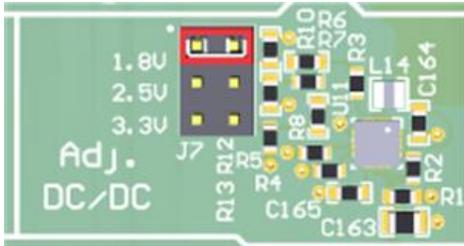
DESCRIPTION	JUMPER SETTING	PICTURE
<p>3.3-V LDO (TPS7A8101)</p>	<p>J1: 1-2 J2: 2-3</p>	
<p>3.3-V DC-DC (TPS54120)</p>	<p>J1: 2-3 J2: 1-2</p>	

Table 2. 1.8-V Supply Plane Connections (continued)

DESCRIPTION	JUMPER SETTING	PICTURE
Adjustable DC-DC (TPS62150)	J5: 2-4 J6: open	

J7 sets the output voltage for the adjustable DC-DC plane.

Table 3. Adjustable DC-DC Supply Settings

DESCRIPTION	JUMPER SETTING	PICTURE
3.3-V output voltage	J5: 2-4 J7: bottom	
2.5-V output voltage	J5: 2-4 J7: middle	
1.8-V output voltage	J5: 2-4 J7: Top	

1.2 Power Distribution

The power distribution jumpers (J9, J11, J12, J14, J16, J17, J19, J21, J22, J24, J25, J27, J29, J34 and J36) are connected to the 3.3-V and 1.8-V supply planes and individual external connections.

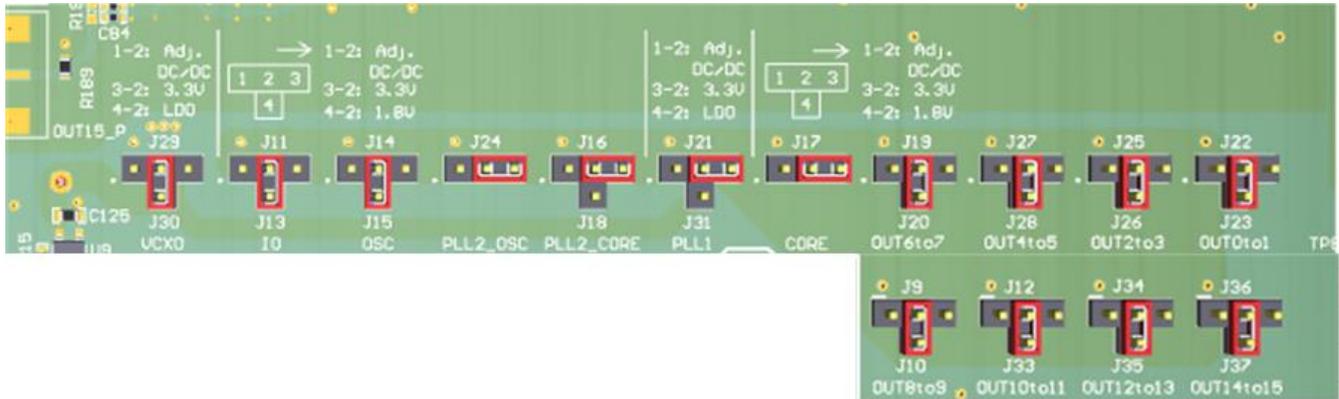


Figure 17. Power Distribution Jumpers

J17 (VDD_CORE) and J24 (VDD_PLL2_OSC) selects between 3.3-V supply plane and adjustable DC-DC connection as shown in [Figure 18](#).



Figure 18. J17, J24 Connection Description

J21 (VDD_PLL1) selects between 3.3-V supply plane, VCXO LDO and adjustable DC-DC connection as shown in [Figure 19](#).



Figure 19. J21 Connection Description

J9 (VDDO_89), J11 (VDD_IO), J12 (VDDO_1011), J14 (VDD_OSC), J16 (VDD_PLL2OSC), J19 (VDDO_67), J22 (VDDO_01), J25 (VDDO_23), J27 (VDDO_45), J34 (VDDO_1213) and J36 (VDDO_1415) selects between 3.3-V supply plane, 1.8-V supply plane and adjustable DC-DC connection as shown in [Figure 20](#).

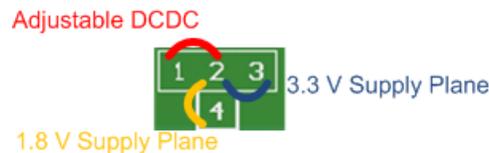
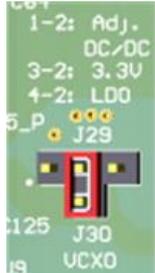
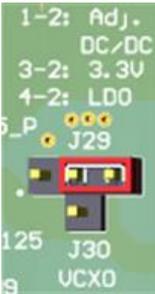
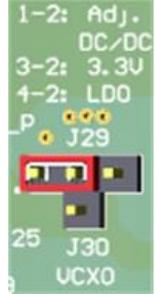


Figure 20. J9, J11, J12, J14, J16, J19, J22, J25, J27, J34, J36 Connection Description

1.3 VCXO Supply Connection

The VCXO has its own LDO (LM5907MFX-3.3). A 5-V supply needs to be connected to VCC_VCXO SMA. Jumper J29 selects between this LDO, the LMK04616 3.3-V supply plane and an adjustable DC-DC supply connection as shown in [Table 4](#).

Table 4. VCXO Supply Connections

DESCRIPTION	JUMPER SETTING	PICTURE
3.3-V LDO (LM5907MFX-3.3)	J26: 2-4	
3.3-V supply plane (TPS7A8101 or TPS54120)	J26: 2-3	
Adjustable DC-DC supply connection on Jumper J28 (TPS62150) NOTE: Apply 3.3 V only!	J26: 1-2	

2 Dip Switch Configuration

Default configuration of Dip Switches is shown in [Table 5](#) or [Figure 21](#).

Table 5. Default Dip Switch Configuration

SWITCH POSITION	S2 SYNC/SYSREF REQ	S3 STAT0	S4 SDIO	S5 STAT1	S6 CLKIn_SEL
1 – High	OFF	OFF	OFF	OFF	OFF
2 – U2A	ON	ON	ON	ON	ON
3 – Low	OFF	OFF	OFF	OFF	OFF
4 – LED	ON	ON	n/a	ON	n/a

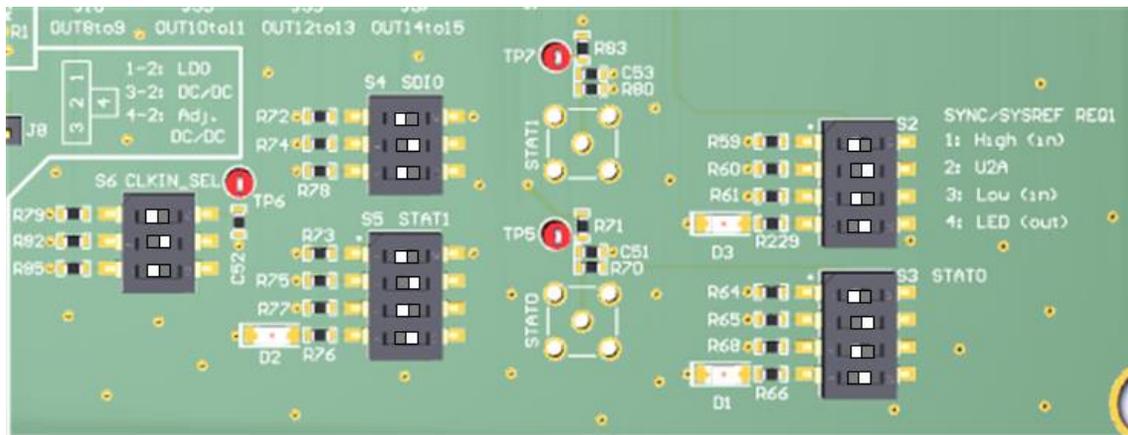
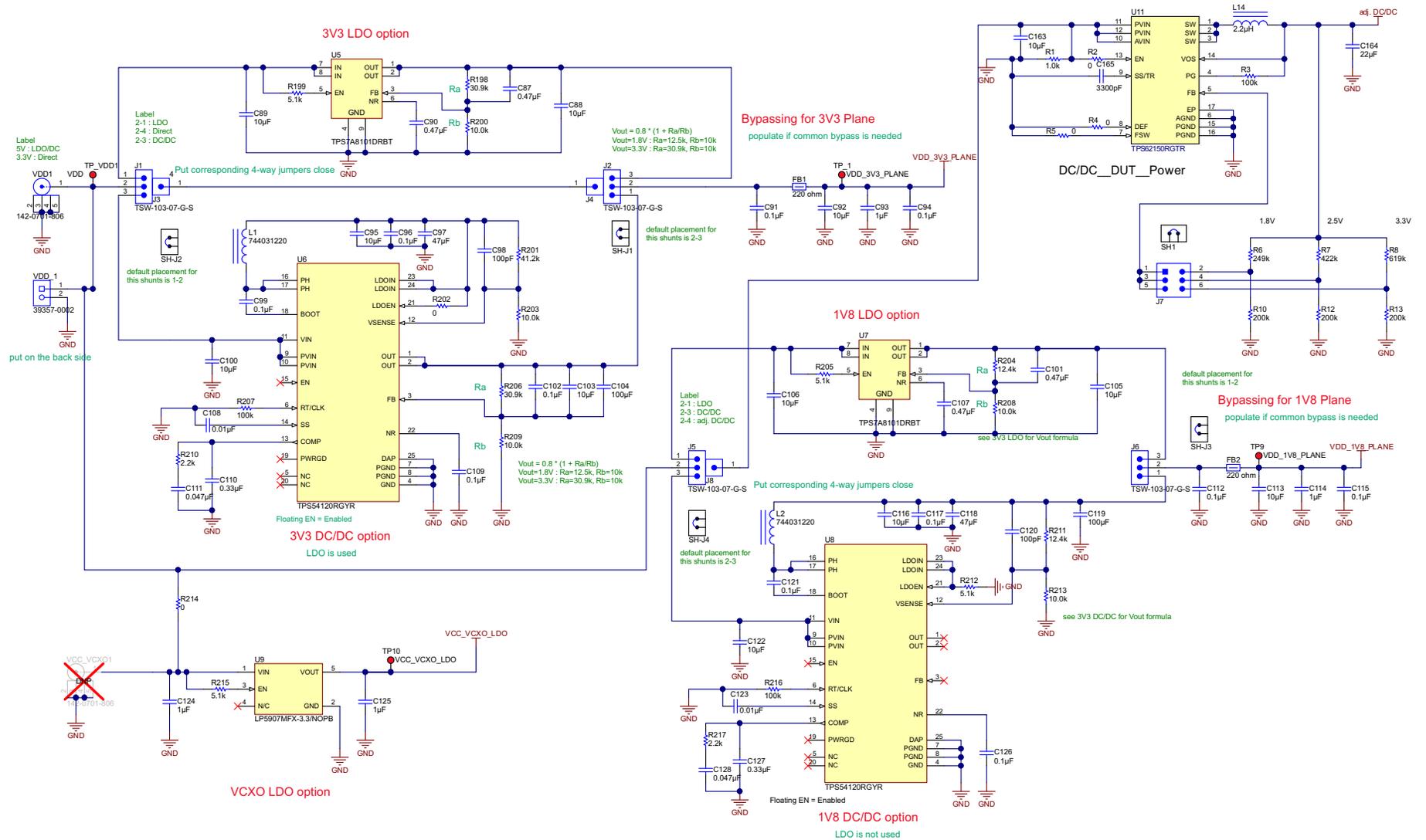


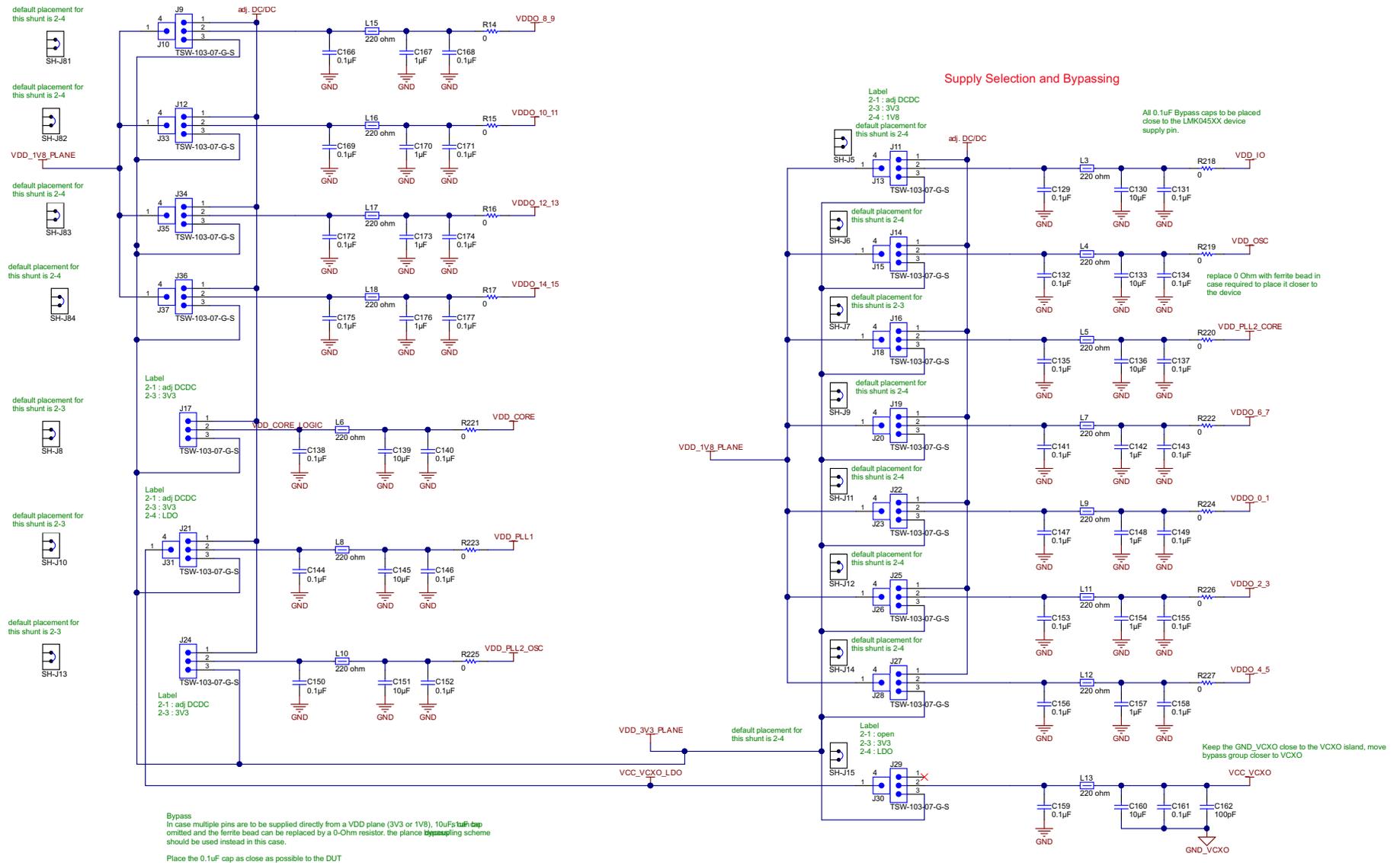
Figure 21. Default Dip Switch Setting

LMK04616 EVM Board Schematic



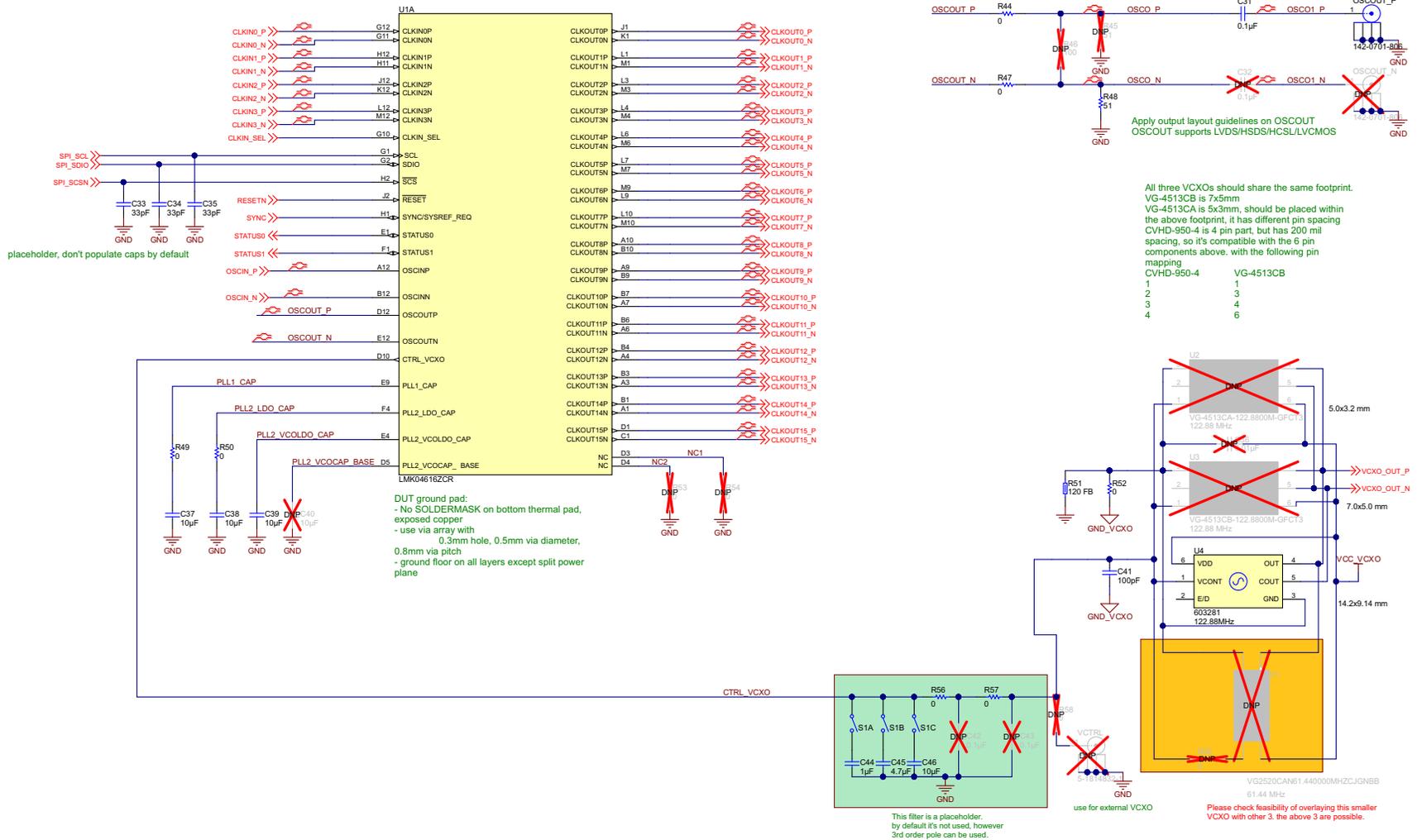
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Figure 22. Power Supply Connection



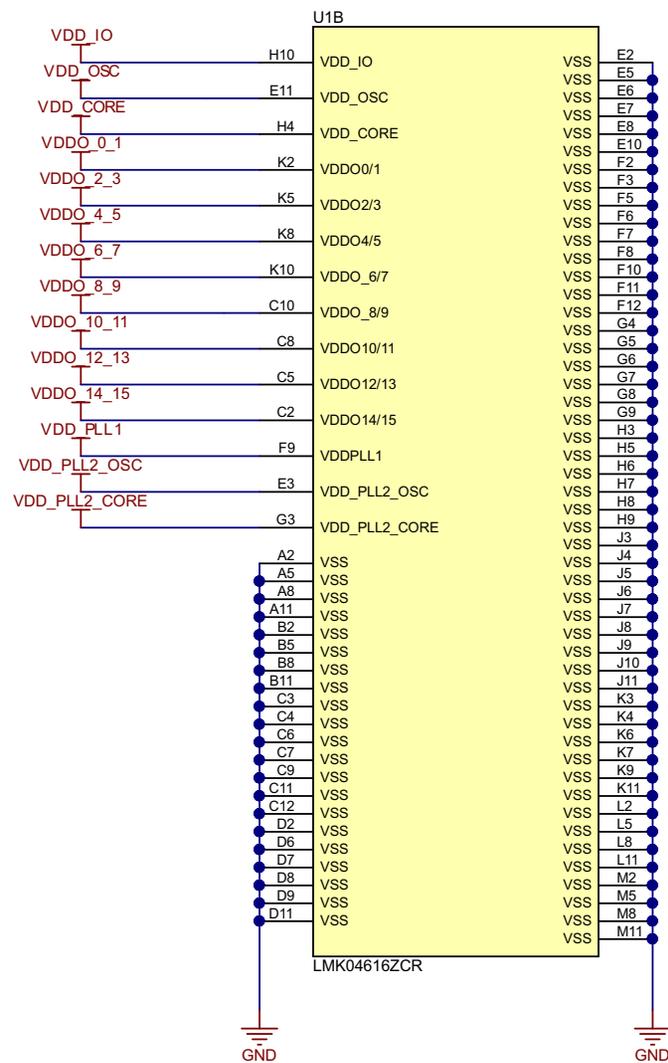
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Figure 23. Power Distribution



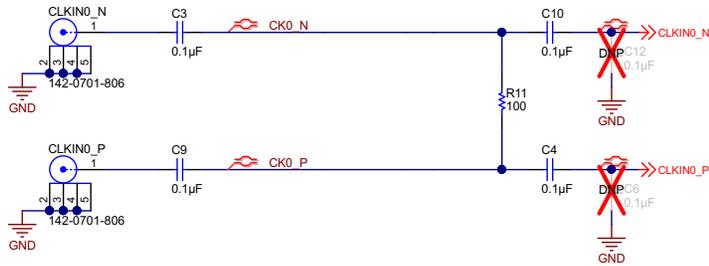
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Figure 25. LMK04616 Main Connection

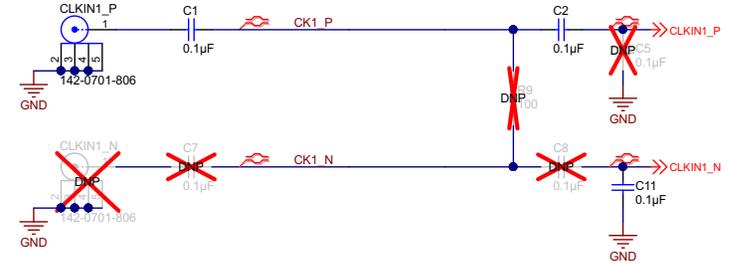


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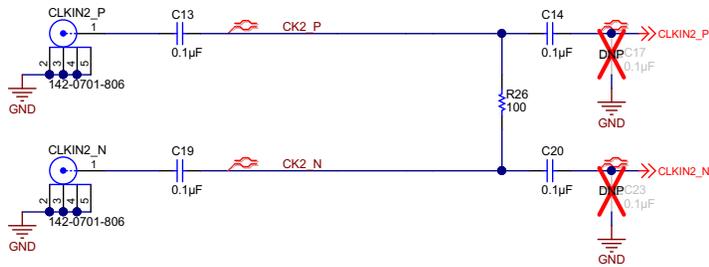
Figure 26. LMK04610 Power Connection



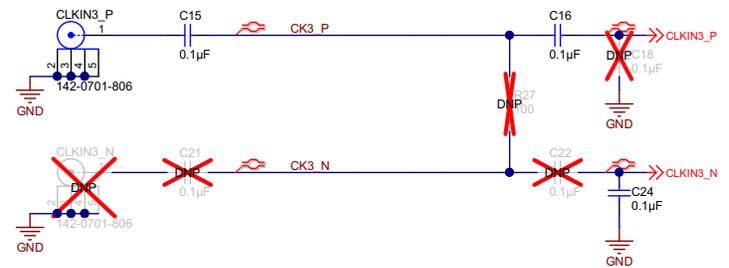
By default, CLKIN0 SMA is DC coupled to the 100 Ohm, then AC coupled to CLKIN0 input



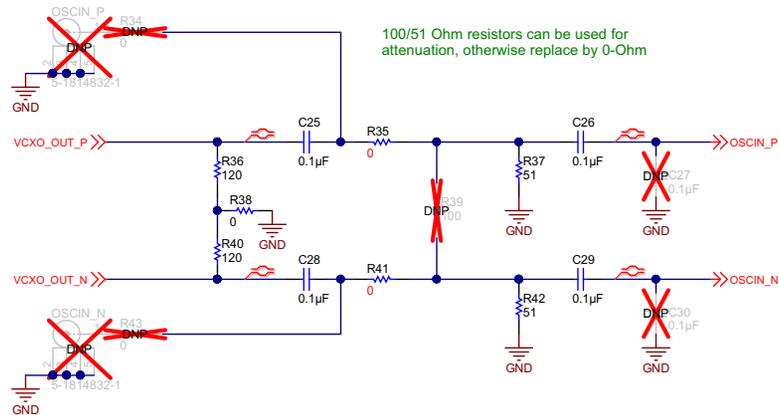
By default, CLKIN1 SMA is DC coupled to the 51 Ohm, then AC coupled to CLKIN1 input
CLKIN1 is single-ended by default (negative input is connected to 0.1µA)



By default, CLKIN2 SMA is DC coupled to the 100 Ohm, then AC coupled to CLKIN2 input



By default, CLKIN3 SMA is DC coupled to the 100 Ohm, then AC coupled to CLKIN3 input



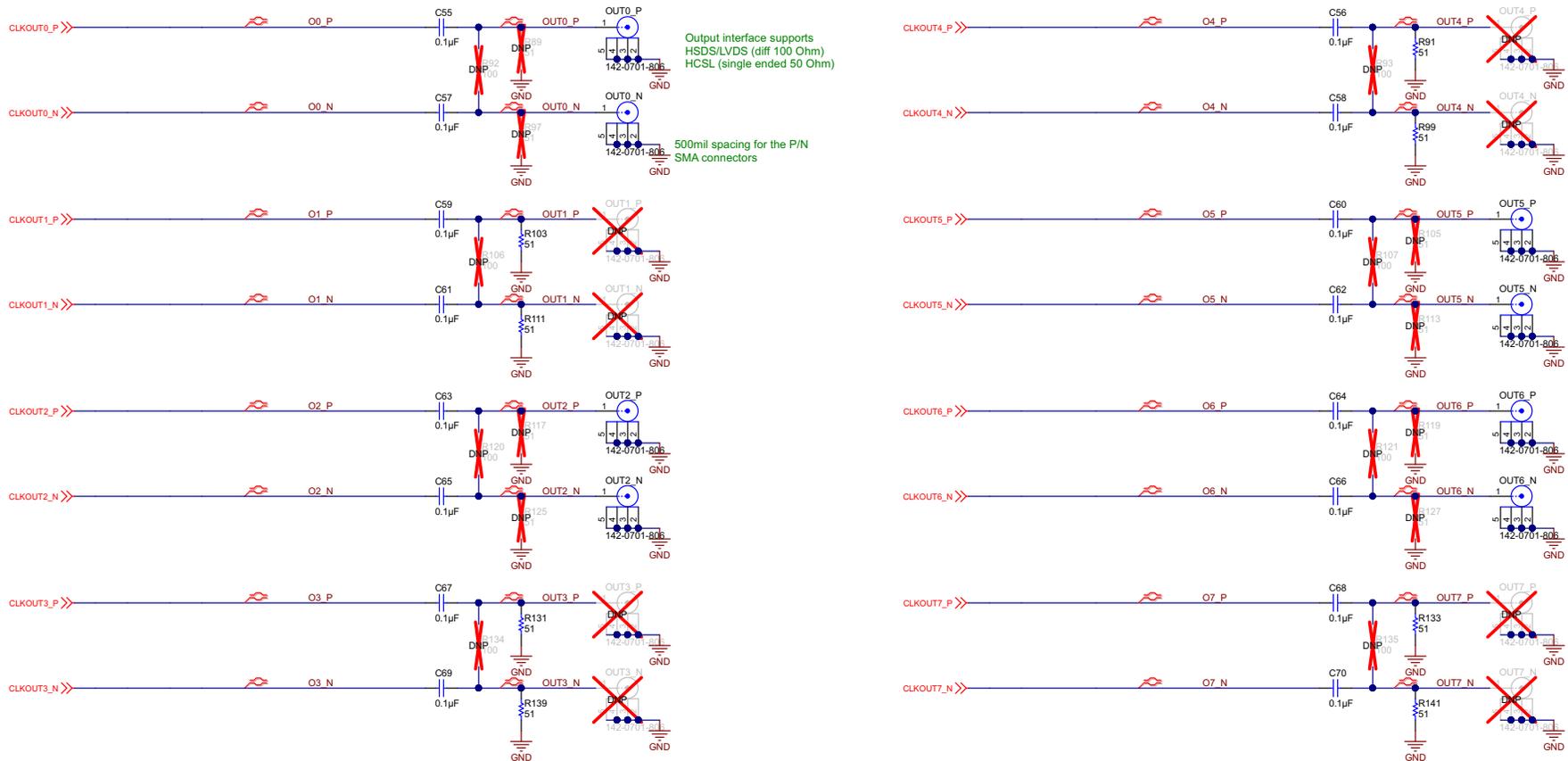
100/51 Ohm resistors can be used for attenuation, otherwise replace by 0-Ohm

Apply Clock input layout guidelines on OSCIN
By default VCXO path (single ended) is AC coupled to OCSIN_P

CLOCK INPUT CLKIN0, CLKIN1 LAYOUT REQUIREMENTS:

- *** CONTROLLED IMPEDANCE ***
- Route as 50-ohm (+/-5% tol.) controlled-impedance single-ended RF traces from SMA center pin to DUT pin
- Place component pads directly on RF traces (no stubs), match 50-ohm trace width to SMA pad, and use 50-ohm Zo via structures.
- *** LENGTH / SKEW MATCHING ***
- Equalize total path length and indiv. trace segments WITHIN pair from DUT to SMA center pin (intra-pair skew).
- There is NO requirement to match inter-pair skew between CLKIN0 path and CLKIN1 path.
- Total path length should be as short as possible. Use 45 deg. serpentine pattern on striplines only to equalize lengths within pair.
- *** SHIELDING / ISOLATION ***
- Use ground shielding on routing layers with clearance to not affect controlled impedance traces.
- Ground flood on routing layers should have clearance of more than 2.5x width from RF traces.
- Use ground stitching vias with 100 mil spacing around RF traces to connect to GND shielding on all layers.
- Avoid crossing Digital signal/return paths with REF input signal/return paths. If unavoidable, cross at a 90 deg. angle

Figure 27. Inputs



CLOCK OUTPUT (OUT#_P, OUT#_N) LAYOUT REQUIREMENTS:

- *** CONTROLLED IMPEDANCE ***
- Route as 50-ohm (+/-5% tol.) controlled-impedance single-ended RF traces from DUT pin to SMA pin
- Place component pads directly on RF traces (no stubs), match 50-ohm trace width to solder pad (30 mils wide), and use 50-ohm Zo via structures.
- *** LENGTH / SKEW MATCHING ***
- Equalize total path length and indiv. trace segments between/within all OUT#_P/_N pairs to SMA pins (NO INTER- or INTRA-pair skew).
- Use 45 deg. serpentine pattern on internal stripline only for equalizing lengths.

*** SHIELDING / ISOLATION ***

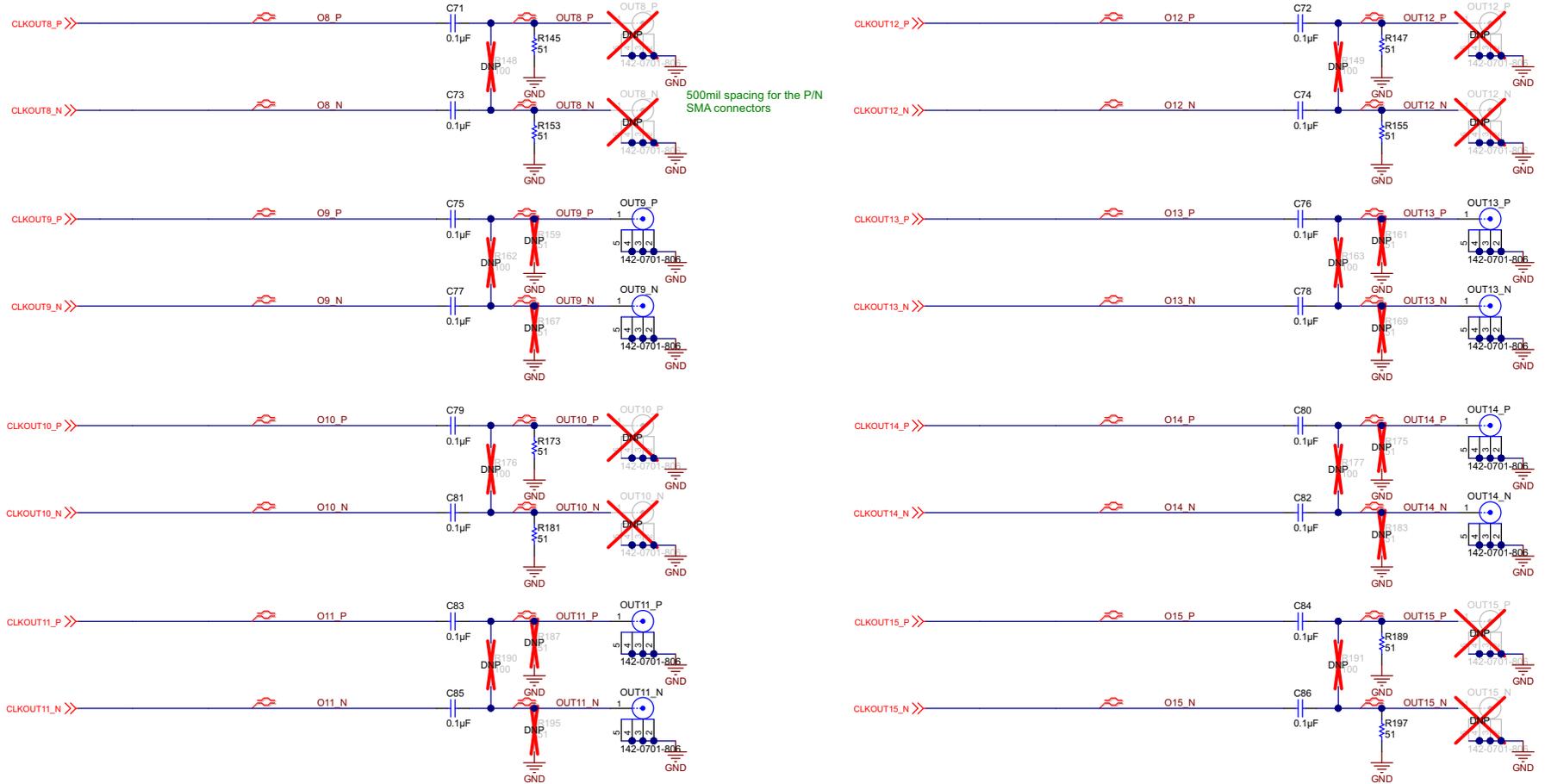
- Use ground shielding on routing layers with clearance to not affect controlled impedance traces.
- Ground flood on routing layers should have clearance of more than 2.5x width from RF traces.
- Use ground stitching vias with 100 mil spacing around RF traces to connect ground on all layers.
- Use sufficient clearance between OUT# paths, as well as from other dynamic signals.
- Avoid crossing Digital signal/return paths with clock OUT signal/return paths. If unavoidable, cross at a 90 deg. angle

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Figure 28. Outputs 0 to 7

Output interface supports
 HSDS/LVDS (diff 100 Ohm)
 HCSL (single ended 50 Ohm)

500mil spacing for the P/N SMA connectors



CLOCK OUTPUT (OUT#_P, OUT#_N) LAYOUT REQUIREMENTS:

- *** CONTROLLED IMPEDANCE ***
- Route as 50-ohm (+/-5% tol.) controlled-impedance single-ended RF traces from DUT pin to SMA pin
- Place component pads directly on RF traces (no stubs), match 50-ohm trace width to SMA pad (30 mils wide), and use 50-ohm Zo via structures.
- *** LENGTH / SKEW MATCHING ***
- Equalize total path length and indiv. trace segments between/within all OUT#_P/N pair/DUT to SMA pins (NO INTER- or INTRA-pair skew).
- Use 45 deg. serpentine pattern on internal stripline only for equalizing lengths.

*** SHIELDING / ISOLATION ***

- Use ground shielding on routing layers with clearance to not affect controlled impedance traces.
- Ground flood on routing layers should have clearance of more than 2.5x width from RF traces.
- Use ground stitching vias with 100 mil spacing around RF traces to connect ground on all layers.
- Use sufficient clearance between OUT# paths, as well as from other dynamic signals.
- Avoid crossing Digital signal/return paths with clock OUT signal/return paths; if unavoidable, cross at a 90 deg. angle

Figure 29. Outputs 8 to 15

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1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
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2. *Limited Warranty and Related Remedies/Disclaimers:*
 - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.
3. *Regulatory Notices:*
 - 3.1 *United States*
 - 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
 - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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