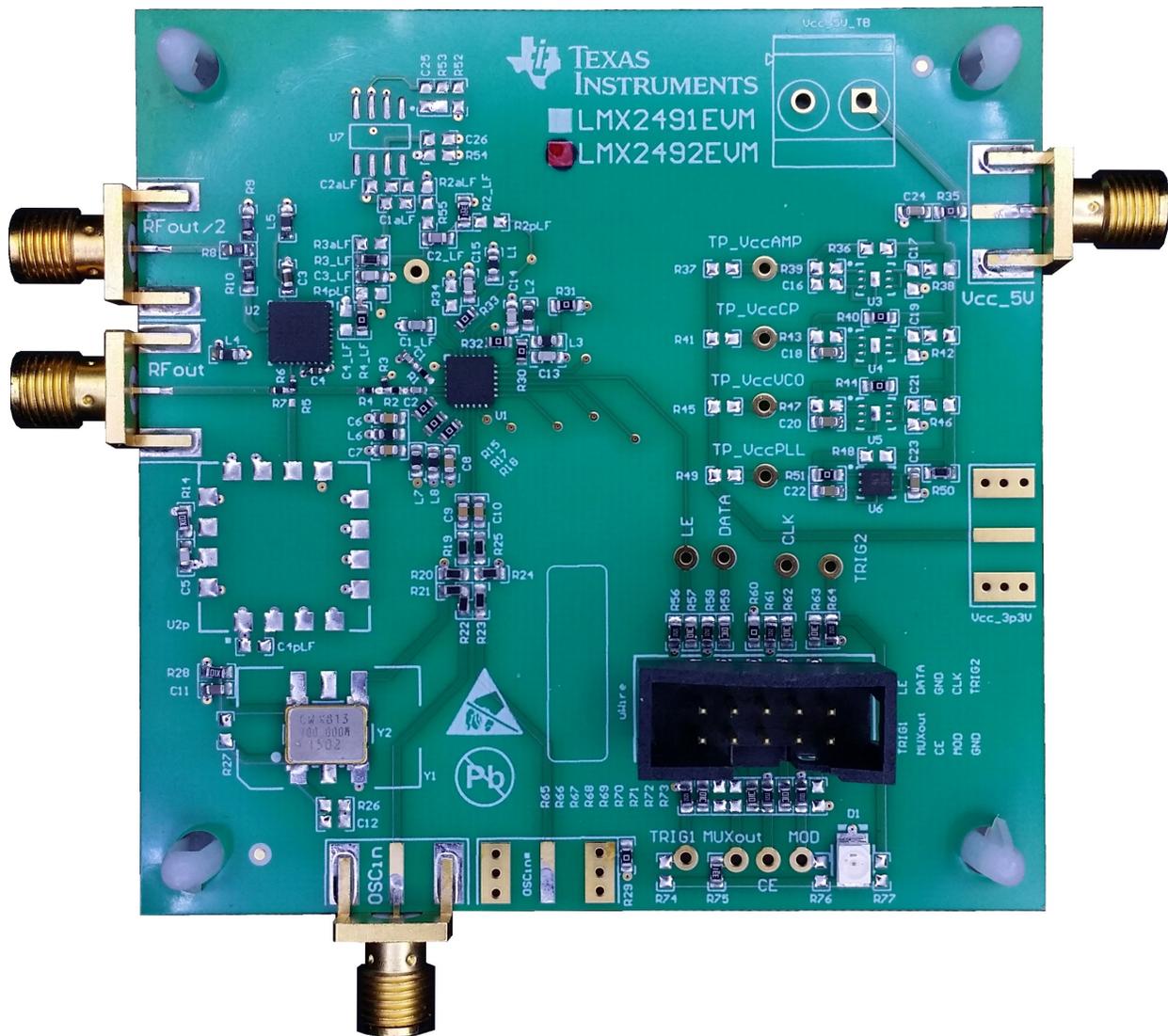


LMX2492EVM Evaluation Module

The LMX2492EVM is design to evaluate the performance of LMX2492. This board consists of a LMX2492 device, a LP5900-3.3V LDO, a 9.4 - 10.8 GHz VCO and a 100 MHz crystal oscillator.

The LMX2492 is a low noise 14 GHz wideband delta-sigma fractional N PLL with ramp and chirp generation. It consists of a phase frequency detector, programmable charge pump, and high frequency input for the external VCO. The LMX2492 supports a broad and flexible class of ramping capabilities, including FSK and configurable piecewise linear FM modulation profiles of up to 8 segments.



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Trademarks

All trademarks are the property of their respective owners.

1 LMX2492EVM Evaluation Module

1.1 Evaluation Module Contents

In the box, there are:

- One LMX2492EVM board (SV601040-002).
- One USB2ANY module (HPA665-001).
- One USB cable.
- One 10-pin ribbon cable.

1.2 Evaluation Setup Requirement

The evaluation will require the following hardware and software:

- A DC power supply
- A spectrum analyzer or a signal analyzer
- A PC running Windows 7 or more recent version
- An oscilloscope (optional)
- A high quality signal generator (optional)
- A function waveform generator (optional)
- Texas Instruments Clocks and Synthesizers TICS Pro software
- Texas Instruments PLLatinum Simulator Tool (optional)

1.3 Resources

Related evaluation and development resources are as follows:

- [LMX2492 datasheet](#)
- [LMX2491 datasheet](#)
- [TICS Pro software](#)
- [PLLatinum Simulator Tool \(PLL Sim\)](#)

2 Setup

2.1 Connection Diagram

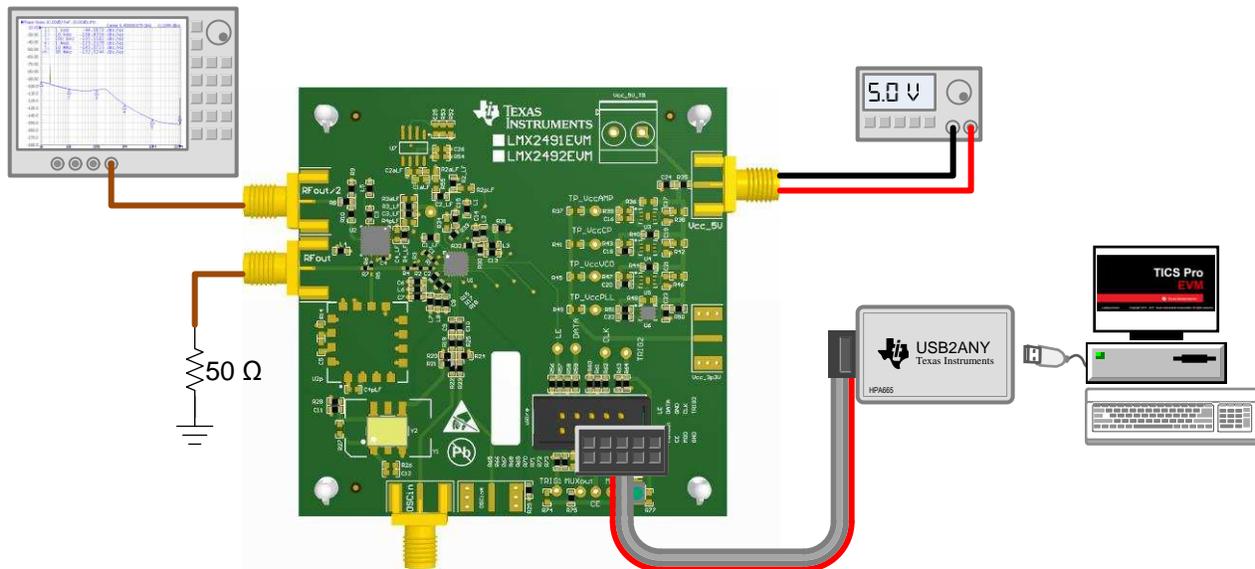


Figure 1. EVM Connection Diagram

2.2 Power Supply

Apply 5-V to Vcc_5V SMA connector. The on-board VCO and the optional op-amp require 5-V supply while the on-board XO and LMX2492 need 3.3-V supply. The on-board LDO regulates 5-V down to 3.3-V. Never apply more than 6-V to Vcc_5V SMA connector or otherwise the LDO will be damaged. The total current consumption of the board is about 240 mA.

2.3 Reference Clock

By default, the board is operated with the on-board 100-MHz CMOS XO. If required, the board can be modified to operate with an external clock source. In this case, apply a single-ended clock to the OSCin SMA connector or apply a differential clock to both OSCin and OSCin* SMA connectors. See [Appendix B](#) for details.

2.4 RF Output

Connect RFout/2 SMA connector to a spectrum analyzer or a signal analyzer. By default, the output signal frequency is 4.8 GHz and the amplitude is about -3 dBm. Because the frequency accuracy of the on-board XO is 25 ppm, RF output frequency may also be off by 25 ppm. The phase noise of the XO is not bad but not excellent, as a result, RF output phase noise may not look very good.

2.5 Programming

Connect the uWire header to a PC using the USB2ANY module. The firmware of the USB2ANY may not be up-to-date. In this case, follow the procedures outlined in [Appendix A](#) to get it updated.

2.6 Evaluation Software

Download and install TICS Pro to a PC. Run the software and follow the following steps to get started.

1. Go to "Select Device" → "PLL" → LMX2492

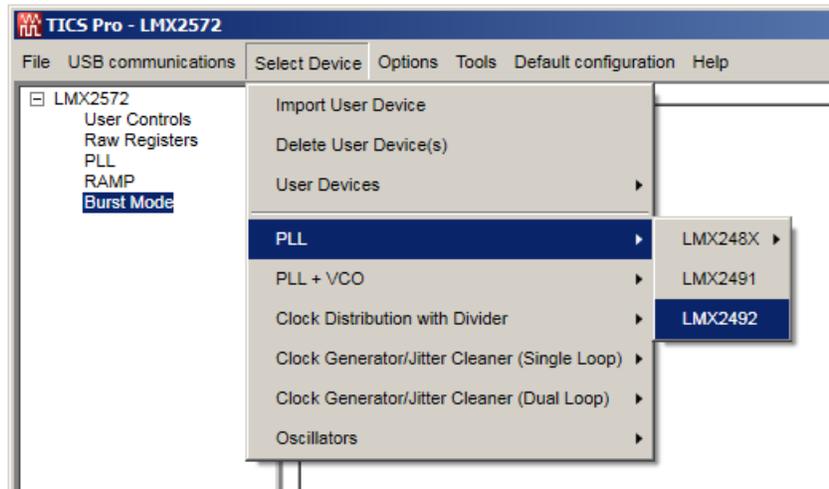


Figure 2. Select Device in TICS Pro

2. Go to "Default configuration" → "Default Mode xxxx-xx-xx"

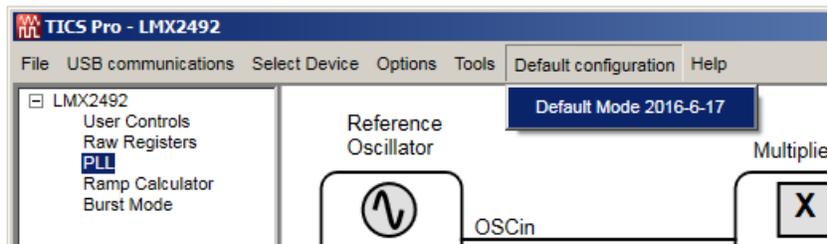


Figure 3. Default Mode

2.7 EVM Strap Options

The MUXout pin is not connected to the uWire header but is used as the lock detect indicator. Other IO pins, such as TRIG1, TRIG2 and MOD are connected to the uWire header. They could be used as the input trigger sources or output flag indicators during frequency ramping.

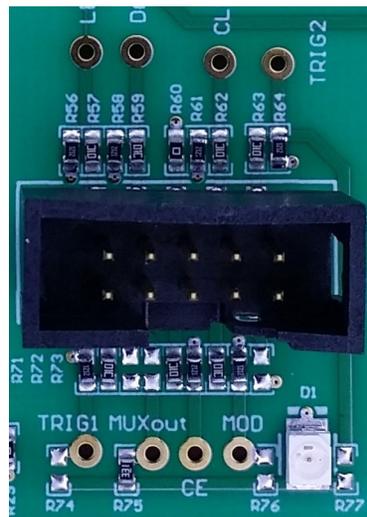


Figure 4. IO Port

3 Typical Measurement

3.1 Default Configuration

3.1.1 Loop Filter

The parameters for the loop filter are:

Table 1. Loop Filter Configuration

PARAMETER	VALUE
VCO frequency	9.4 - 10.8 GHz
VCO gain	240 MHz/V
Effective charge pump gain	3.1 mA
Phase detector frequency	100 MHz
Loop bandwidth	435 kHz
Phase margin	60.8 degrees
C1_LF	68 pF
C2_LF	3.9 nF
C3_LF	150 pF
C4_LF	Open
R2_LF	390 Ω
R3_LF	150 Ω
R4_LF	0 Ω

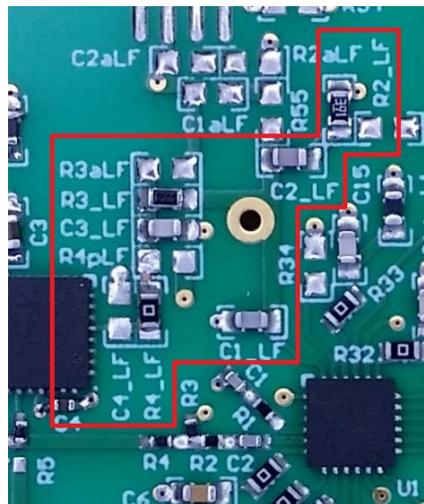


Figure 5. Loop Filter

3.1.2 Typical Output

1. Follow [Section 2](#) to setup the evaluation.
2. Go to "USB communications" → "Write All Registers" to write all the registers to LMX2492.

Default output is 4.8 GHz at RFout/2 SMA connector.

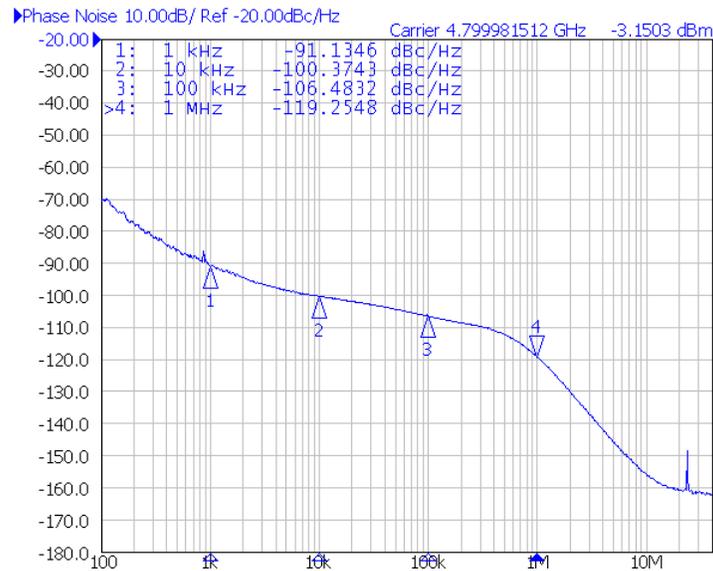


Figure 6. Default Output

3.2 Additional Tests

3.2.1 Frequency Shift Keying (FSK) Example

FSK operation requires an external input trigger signal at either MOD, TRIG1 or TRIG2 pin. In this example, MOD pin is selected as the Trigger A source. A 20 kHz square-wave clock will be applied to MOD pin to toggle the RF output to switch between 9600 MHz and 9604 MHz. That is, FSK deviation is 4 MHz.

The screenshot shows the TICS Pro configuration interface with the following settings:

- General Tab:**
 - PLL Controls: CPPOL (Positive), SWRST (unchecked), CPM_THR_HIGH (50), CPM_THR_LOW (10), PFD_DLY (860 ps), OSC_DIFFR (unchecked).
 - Readback: CPM_FLAGL, CPM_FLAGH (unchecked).
 - Lock Detect: DLD_PASS_CNT (32), DLD_TOL (1 ns), DLD_ERR_CNT (4).
 - Output Pins: MUXout_MUX (Output DLD&CPMON), TRIG2_PIN (Tristate), TRIG1_MUX (Input TRIG1), TRIG2_MUX (Input TRIG2), MOD_MUX (Input MOD), TRIG1_PIN (Tristate).
 - Speed Up Controls: FL_TOC (0), FL_CSR (Disabled), FL_CPG (Disabled).
- General Ramp Controls Tab:**
 - General Ramp Controls: RAMP_CLK (unchecked), RAMP_EN (checked), RAMP_TRIGA (MOD Rising Edge), RAMP_TRIGB (Disabled), RAMP_TRIGC (Disabled), RAMP_CNT (0), RAMP_TRIG_INC (Ramp Transition).
 - Frequency and Phase Module: RAMP_AUTO, RAMP_PM_EN (unchecked), FSK_DEV_TRIG (Trigger A), FSK_DEV (671089).
 - Ramp Comparators: RAMP_CMP0 (33554432), RAMP_CMP0_EN (0), RAMP_CMP1_EN (0).
 - Ramp Limits: RAMP_LIMIT_LOW (8489271296), RAMP_LIMIT_HIGH (402653184).

Figure 7. TICS Pro FSK Configuration

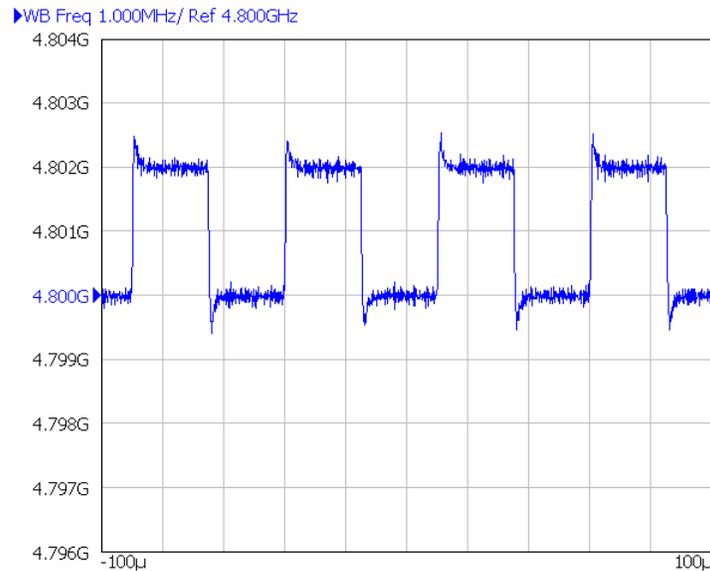


Figure 8. FSK Example

3.2.2 Continuous Sawtooth Ramp Example

This example shows how to generate a continuous sawtooth ramp. Only one ramp segment is necessary as it will loop back to itself.

Limits and Comparators

VCO Output Limit

High MHz

Low MHz

Register Programming

Sign	Decimal Value	2's Complement
High 0	402653184	402653184
Low 1	100663296	8489271296

Valid In Ramp

CMP0 MHz

CMP1 MHz

Valid In Ramp

0 1 2 3 4 5 6 7

Register Programming

Sign	Decimal Value	2's Complement
CMP0 0	33554432	33554432
CMP1 1	33554432	8556380160

This range must be greater than the ramp range

Don't care because they are not enabled

Ramps

Ramp Enable

Ramp Number	Actual Start Frequency (MHz)	Desired End Frequency (MHz)	Duration (us)	Dly	Next Ramp	Start next ramp after	RST	FL	Flags	Actual End Frequency (MHz)	Length	Increment (dec)
0	9600	9700	100	<input type="checkbox"/>	0	TOC Timeout	<input checked="" type="checkbox"/>	<input type="checkbox"/>	Disabled	9700.0165939E	10000	1678
1	-1	10500	100	<input type="checkbox"/>	0	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Disabled	-1	10000	10000
2	-1	10500	100	<input type="checkbox"/>	0	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Disabled	-1	10000	10000
3	-1	10500	100	<input type="checkbox"/>	0	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Disabled	-1	10000	10000
4	-1	10500	100	<input type="checkbox"/>	0	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Disabled	-1	10000	10000
5	-1	10500	100	<input type="checkbox"/>	0	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Disabled	-1	10000	10000
6	-1	10500	100	<input type="checkbox"/>	0	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Disabled	-1	10000	10000
7	-1	10500	100	<input type="checkbox"/>	0	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Disabled	-1	10000	10000

Ramp Count Ramp Auto RAMP_AUTO Ramp In Source

Trigger Source A

Trigger Source B

Trigger Source C

FSK Trigger

FSK Deviation

Phase Mod. En RAMP_PM_EN

Increment (2s complement)

0	1678	4	0
1	0	5	0
2	0	6	0
3	0	7	0

Figure 9. Continuous Sawtooth Ramp Configuration

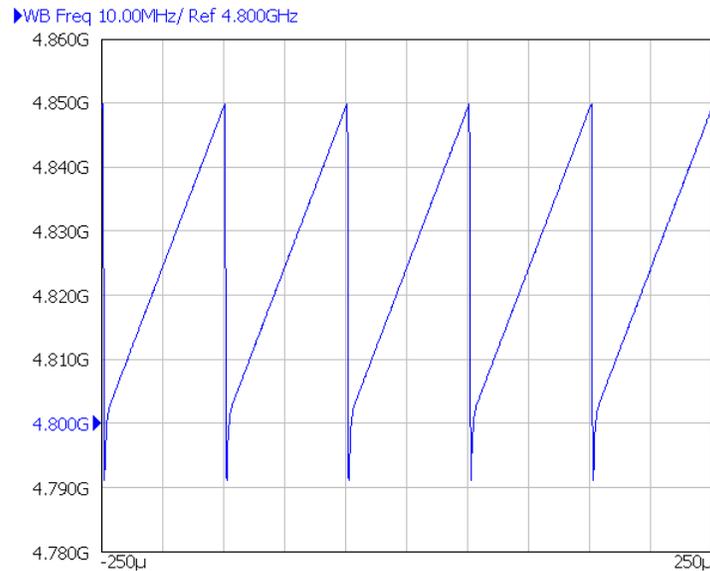


Figure 10. Continuous Sawtooth Ramp Example

3.2.3 Continuous Trapezoid Ramp Example

This is a long-ramp example, the ramp duration is 1 ms. RAMPx_DLY is enabled so that the ramp generator will ramp every 2 phase detector cycles. Output flags are turned on to indicate the start of a ramp.

Ramps Ramp Enable RAMPx_DLY

Ramp Number	Actual Start Frequency (MHz)	Desired End Frequency (MHz)	Duration (us)	Dly	Next Ramp	Start next ramp after	RST	FL	Flags	Actual End Frequency (MHz)	Length	Increment (dec)
0	9600	9600	500	<input type="checkbox"/>	1	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Disabled	9600	50000	0
1	9600	9700	1000	<input checked="" type="checkbox"/>	2	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Flag0	9700.13580322	50000	336
2	9700.13580322	9700	500	<input type="checkbox"/>	3	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Disabled	9700.13580322	50000	0
3	9700.13580322	9600	1000	<input checked="" type="checkbox"/>	0	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Flag0 & Fla	9600	50000	-336
4	-1	10500	100	<input type="checkbox"/>	0	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Disabled	-1	10000	10000
5	-1	10500	100	<input type="checkbox"/>	0	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Disabled	-1	10000	10000
6	-1	10500	100	<input type="checkbox"/>	0	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Disabled	-1	10000	10000
7	-1	10500	100	<input type="checkbox"/>	0	TOC Timeout	<input type="checkbox"/>	<input type="checkbox"/>	Disabled	-1	10000	10000

Ramp Count: 0 Ramp Auto: RAMP_AUTO Ramp In Source: Ramp Transition

Trigger Source A: Disabled Trigger Source B: Disabled Trigger Source C: Disabled

FSK Trigger: Disabled FSK Deviation: 0 Phase Mod. En: RAMP_PM_EN

Increment (2s complement)

0	0	4	0
1	336	5	0
2	0	6	0
3	1073741488	7	0

Figure 11. Continuous Trapezoid Ramp Configuration

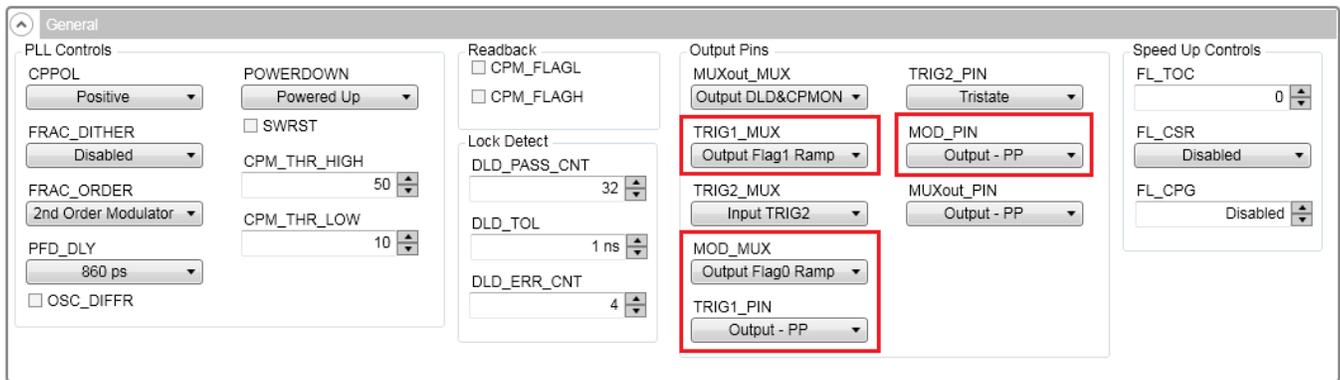


Figure 12. Flag Out Pins Configuration

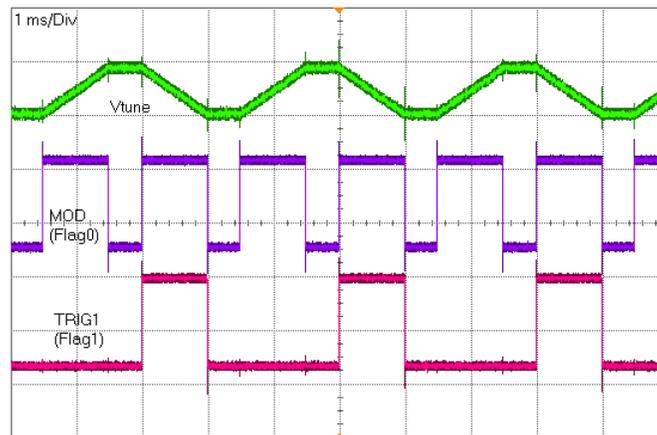


Figure 13. Flags Out Timing

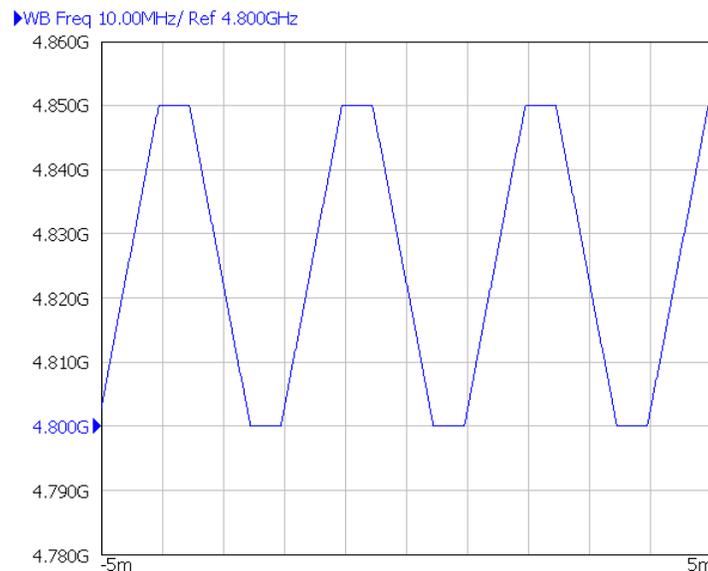


Figure 14. Continuous Trapezoid Ramp Example

3.2.4 Register Readback

To read back the written register values,

1. Remove R75 so that the MUXout pin is disconnected from the LED.
2. Populate R68 to connect MUXout pin to USB2ANY.
3. In TICS Pro, set MUXout pin to "Output Readback".

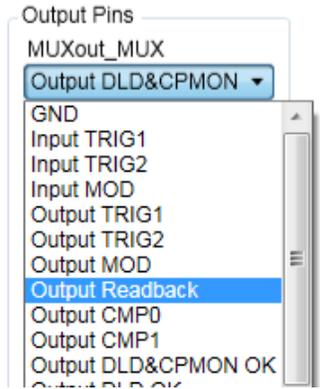


Figure 15. Readback Setting

4. Click on the Register Name that you want to read back.
5. Click the Read Register button to read back the register value.

Register Name	Address/Value	2	2	2	2	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
		3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
R38	0x002618	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	1	1	0	0	0
R37	0x002510	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	0	0
R36	0x002408	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0
R35	0x002341	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1	0	0	0	0	0	1
R34	0x002204	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0

Data: 0x002618

Write Register

Read Register

Figure 16. Register Readback

4 Schematic

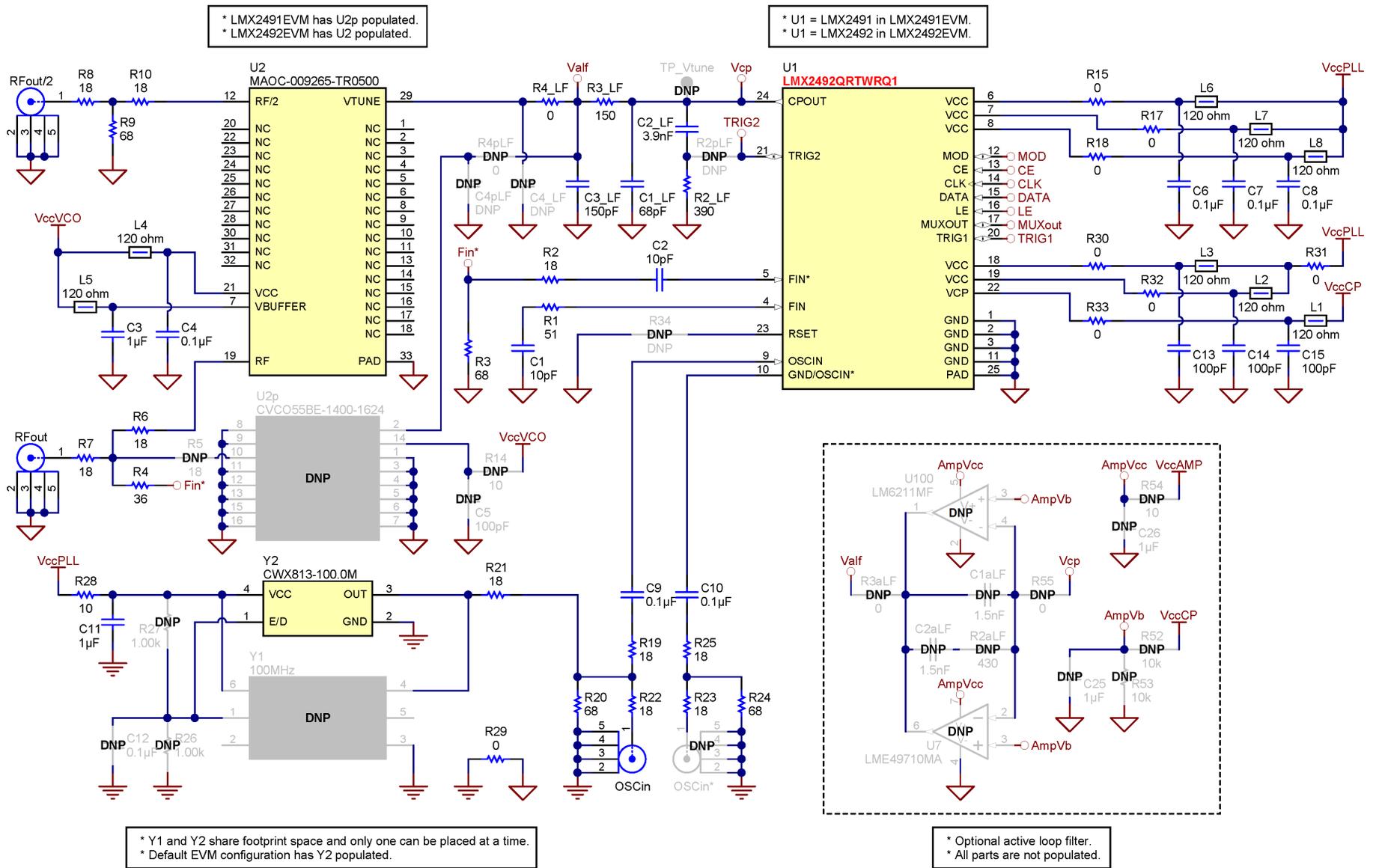


Figure 17. LMX2492EVM Schematic (Page 1)

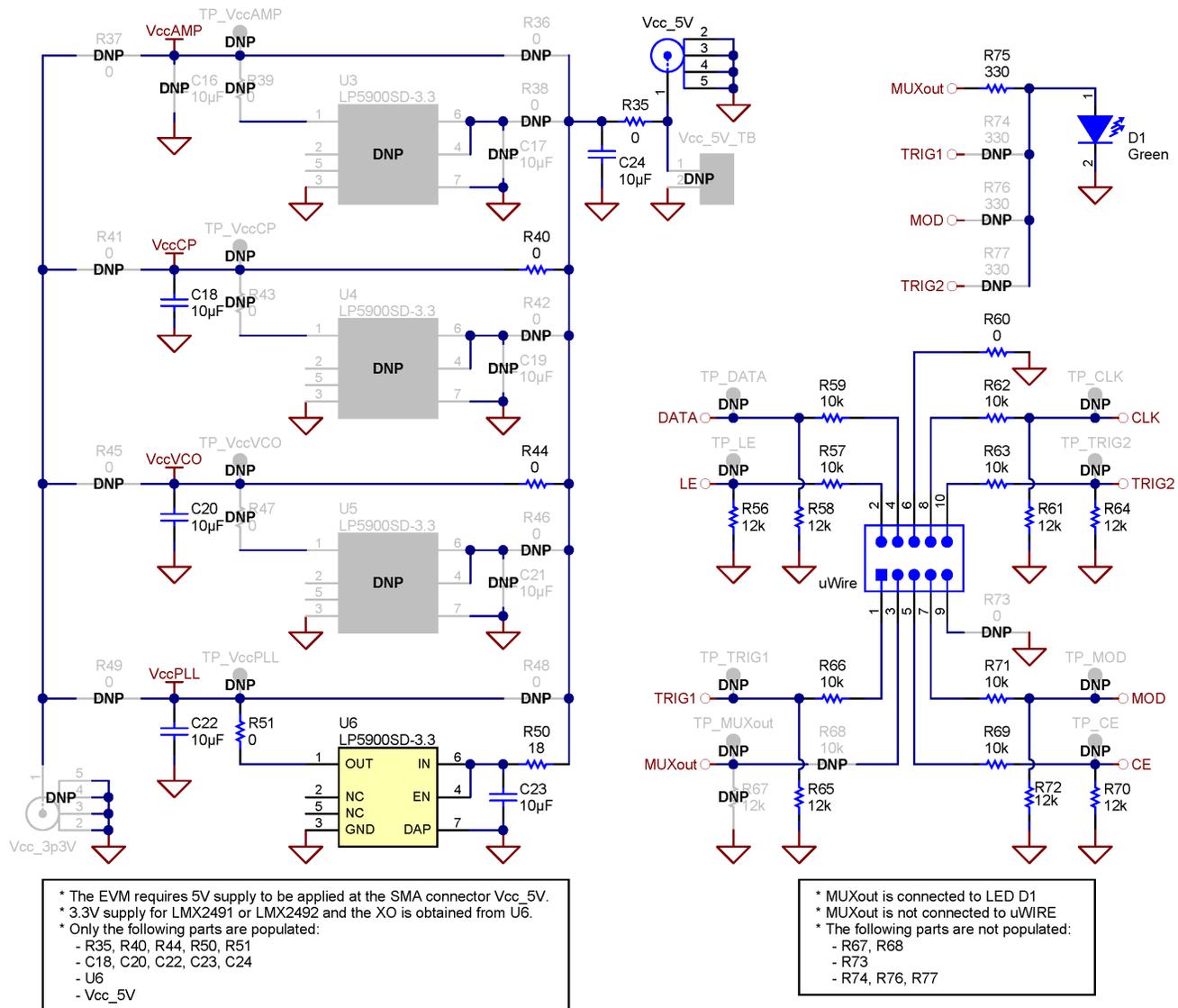


Figure 18. LMX2492EVM Schematic (Page 2)

5 PCB Layout and Layer Stack-up

5.1 PCB Layer Stack-up

The top layer is 1 oz copper.

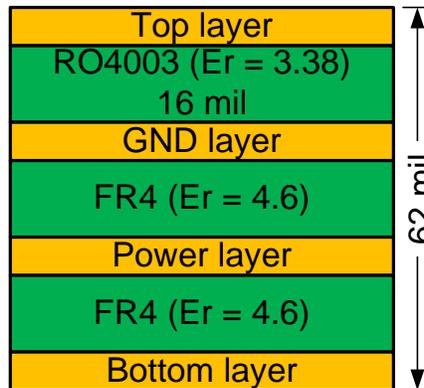


Figure 19. PCB Layer Stack-up

5.2 PCB Layout

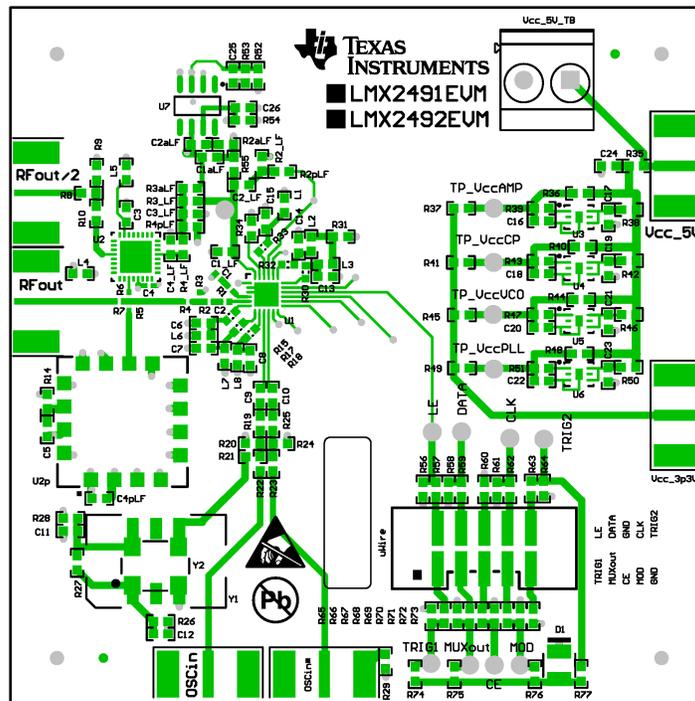


Figure 20. Top Layer

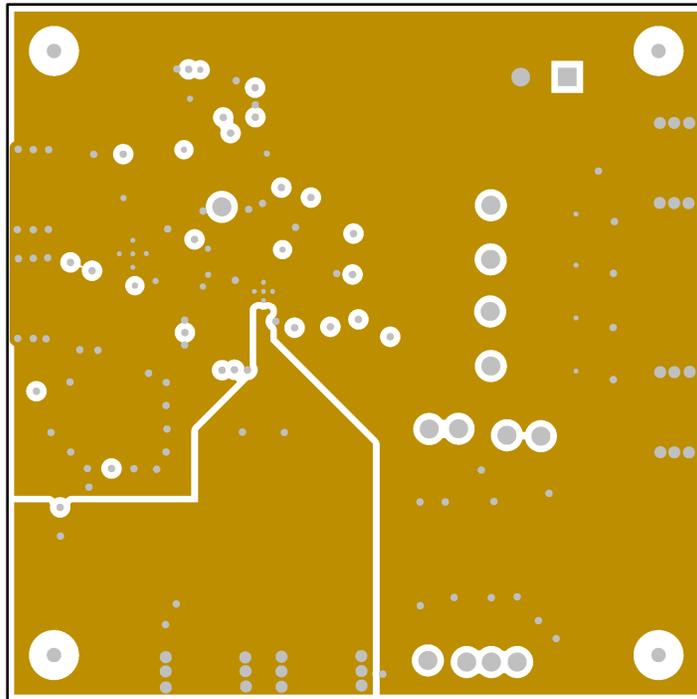


Figure 21. GND Layer

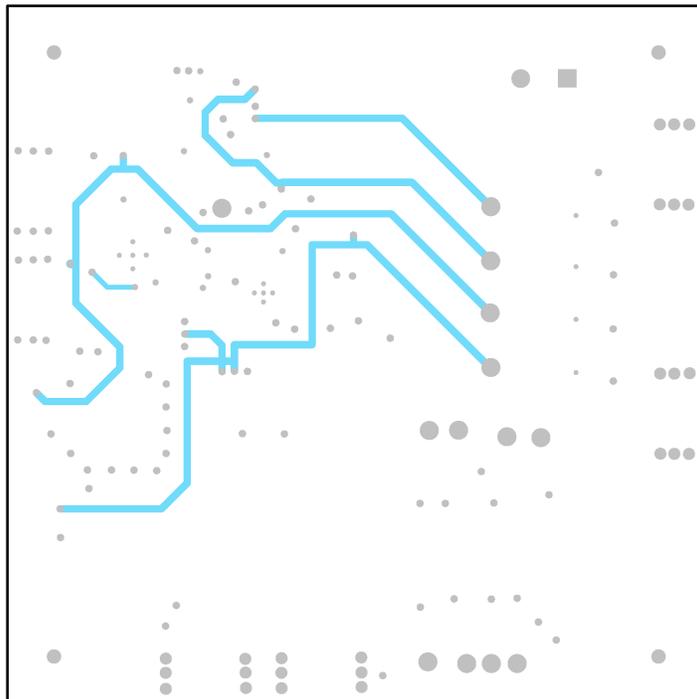


Figure 22. Power Layer

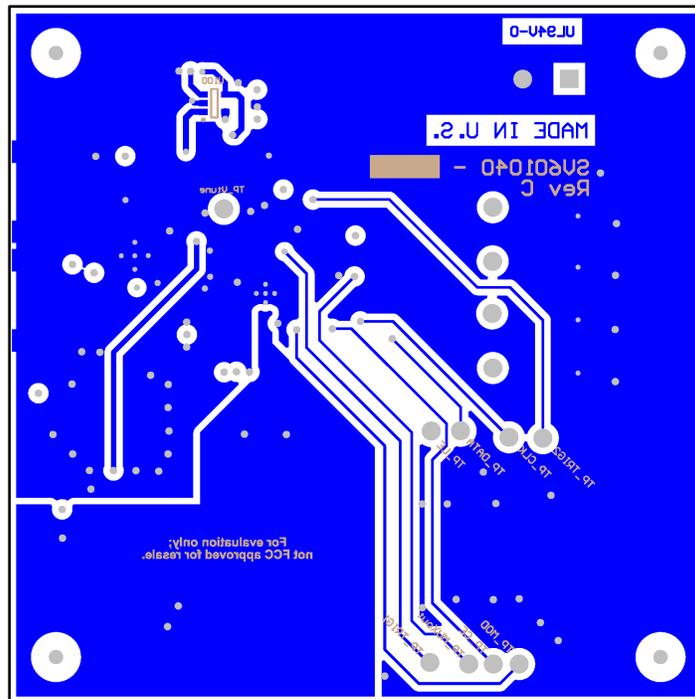


Figure 23. Bottom Layer

6 Bill of Materials

Table 2. Bill of Materials

DESIGNATOR	QUANTITY	DESCRIPTION	PART NUMBER	MANUFACTURER
C1, C2	2	CAP, CERM, 10 pF, 50 V, ±5%, COG/NP0, 0402	500R07S100JV4T	Johanson Technology
C1_LF	1	CAP, CERM, 68 pF, 50 V, ±5%, COG/NP0, 0603	C0603C680J5GACTU	Kemet
C2_LF	1	CAP, CERM, 3900 pF, 50 V, ±5%, COG/NP0, 0603	GRM1885C1H392JA01D	MuRata
C3, C11	2	CAP, CERM, 1 µF, 16 V, ±10%, X7R, 0603	C1608X7R1C105K	TDK
C3_LF	1	CAP, CERM, 150 pF, 50 V, ±5%, COG/NP0, 0603	C0603C151J5GACTU	Kemet
C4	1	CAP, CERM, 0.1 µF, 50 V, ±10%, COG/NP0, 0402	C1005X7R1H104K	TDK
C6, C7, C8, C9, C10	5	CAP, CERM, 0.1 µF, 16 V, ±5%, X7R, 0603	0603YC104JAT2A	AVX
C13, C14, C15	3	CAP, CERM, 100 pF, 50 V, ±5%, COG/NP0, 0603	C0603C101J5GACTU	Kemet
C18, C20, C22, C23, C24	5	CAP, CERM, 10 µF, 6.3 V, ±20%, X5R, 0603	C0603C106M9PACTU	Kemet
D1	1	LED, Green, SMD	SML-LX2832GC-TR	Lumex
L1, L2, L3, L4, L5, L6, L7, L8	8	3 A Ferrite Bead, 120 Ω @ 100 MHz, SMD	BLM18SG121TN1D	MuRata
OSCI _n , Vcc_5V	2	Connector, SMT, End launch SMA 50 Ω	142-0701-851	Emerson Network Power Connectivity
R1	1	RES, 51 Ω, 5%, 0.063 W, 0402	CRCW040251R0JNED	Vishay-Dale
R2, R6, R7	3	RES, 18 Ω, 5%, 0.063 W, 0402	CRCW040218R0JNED	Vishay-Dale
R2_LF	1	RES, 390 Ω, 5%, 0.1 W, 0603	CRCW0603390RJNEA	Vishay-Dale
R3	1	RES, 68 Ω, 5%, 0.063 W, 0402	CRCW040268R0JNED	Vishay-Dale
R3_LF	1	RES, 150 Ω, 5%, 0.1 W, 0603	CRCW0603150RJNEA	Vishay-Dale
R4	1	RES, 36 Ω, 5%, 0.063 W, 0402	CRCW040236R0JNED	Vishay-Dale
R4_LF, R15, R17, R18, R29, R30, R31, R32, R33, R35, R40, R44, R51, R60	14	RES, 0 Ω, 5%, 0.1 W, 0603	CRCW06030000Z0EA	Vishay-Dale
R8, R10, R19, R21, R22, R23, R25, R50	8	RES, 18 Ω, 5%, 0.1 W, 0603	CRCW060318R0JNEA	Vishay-Dale
R9, R20, R24	3	RES, 68 Ω, 5%, 0.1 W, 0603	CRCW060368R0JNEA	Vishay-Dale
R28	1	RES, 10 Ω, 5%, 0.1 W, 0603	CRCW060310R0JNEA	Vishay-Dale
R56, R58, R61, R64, R65, R70, R72	7	RES, 12k Ω, 5%, 0.1 W, 0603	CRCW060312K0JNEA	Vishay-Dale
R57, R59, R62, R63, R66, R69, R71	7	RES, 10k Ω, 5%, 0.1 W, 0603	CRCW060310K0JNEA	Vishay-Dale
R75	1	RES, 330 Ω, 5%, 0.1 W, 0603	RC0603JR-07330RL	Yageo America
RFout, RFout/2	2	Connector, SMT, End launch SMA 50 Ω	142-0701-851	Emerson Network Power
U1	1	500 MHz to 14 GHz Wideband, Low Noise Fractional N PLL With Ramp/Chirp Generation	LMX2492QRTWRQ1	Texas Instruments
U2	1	Voltage Controlled Oscillator 9.4 - 10.8 GHz	MAOC-009265-TR0500	MACOM
U6	1	Ultra Low Noise, 150 mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor	LP5900SD-3.3	Texas Instruments
uWire	1	Header (shrouded), 100mil, 5x2, Gold plated, SMD	52601-S10-8LF	FCI
Y2	1	OSC 100.0000 MHz 3.3 V ±25 PPM SMD	CWX813-100.0M	Connor-Winfield

7 Troubleshooting Guide

If the EVM does not work as expected, use the following chart to identify potential root causes. Couples of thing to note:

- Make modifications to the EVM or change the default settings until AFTER it is verified to be working.
- Register readback requires the correct hardware and software setup. See [Section 3.2.4](#) for details.
- The POR current of the LMX2492EVM is approximately 175 mA.
- The powerdown current of the LMX2492EVM is approximately 175 mA.

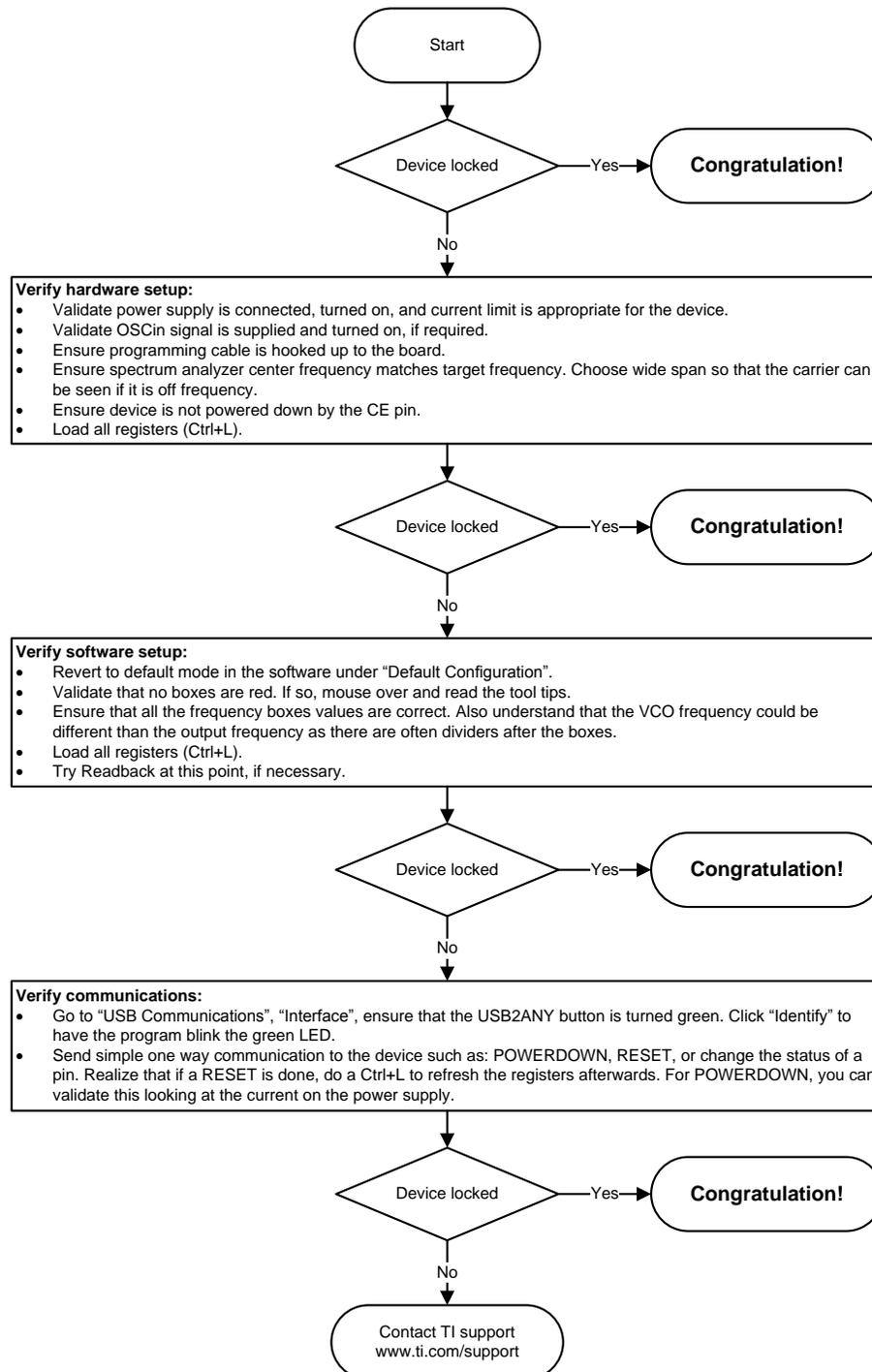


Figure 24. Troubleshooting Guide

USB2ANY Firmware Upgrade

Usually when the USB2ANY module is used at the first time, TICS Pro will request for a firmware update. Simply follow the pop-up instructions to complete the update. This is necessary to ensure that the USB connection between the PC and the USB2ANY module is properly setup, otherwise the programming to LMX2492EVM will not be successful.

1. When you see this message, click the "OK" button.

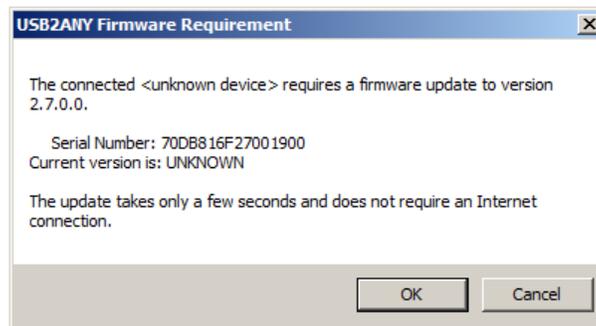


Figure 25. Firmware Requirement

2. Next, follow the on-screen procedure.

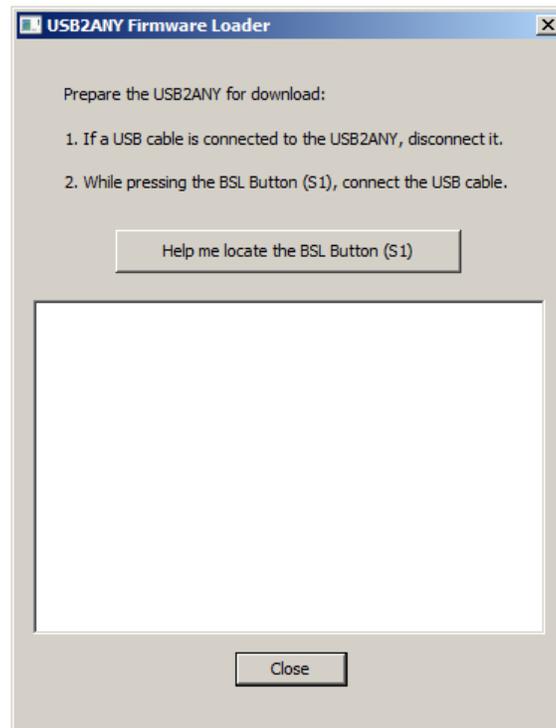


Figure 26. Firmware Loader

3. If you don't know the location of the BSL button, click the long button in the middle of the screen.

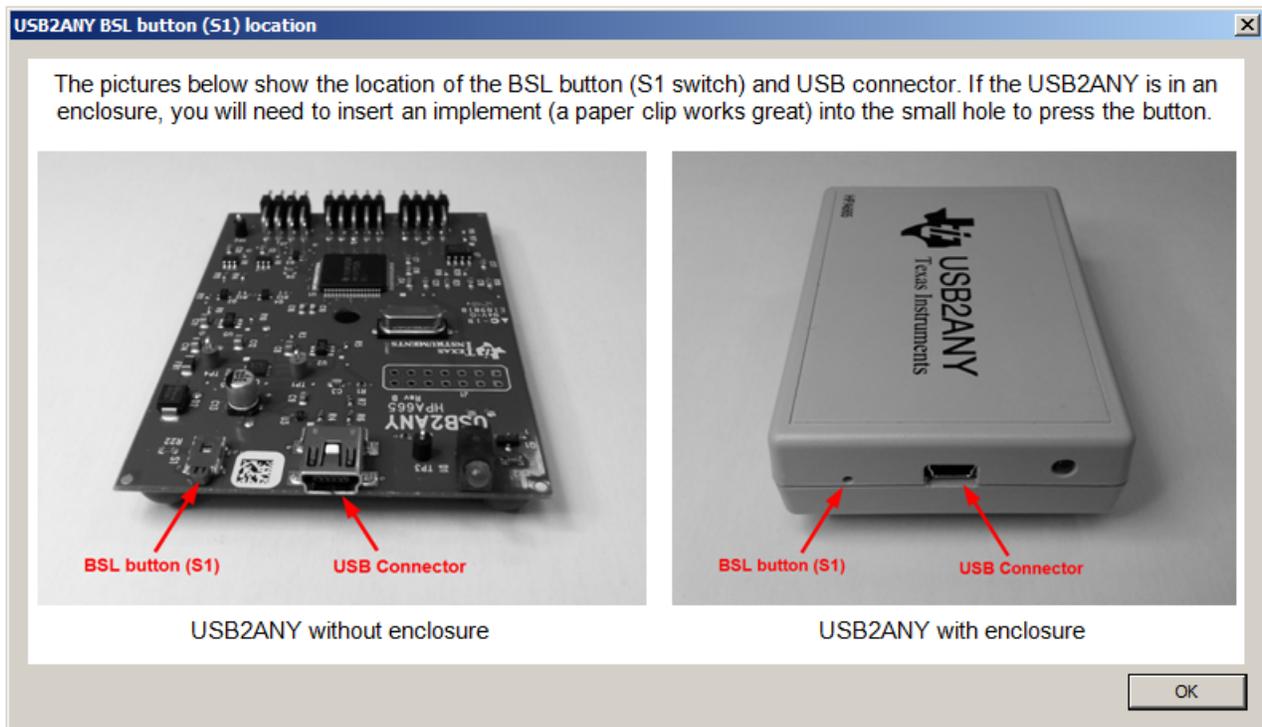


Figure 27. BSL Button

4. Click the "OK" button to go back to the previous screen. Follow the on-screen procedure until the below screen is pop-up.

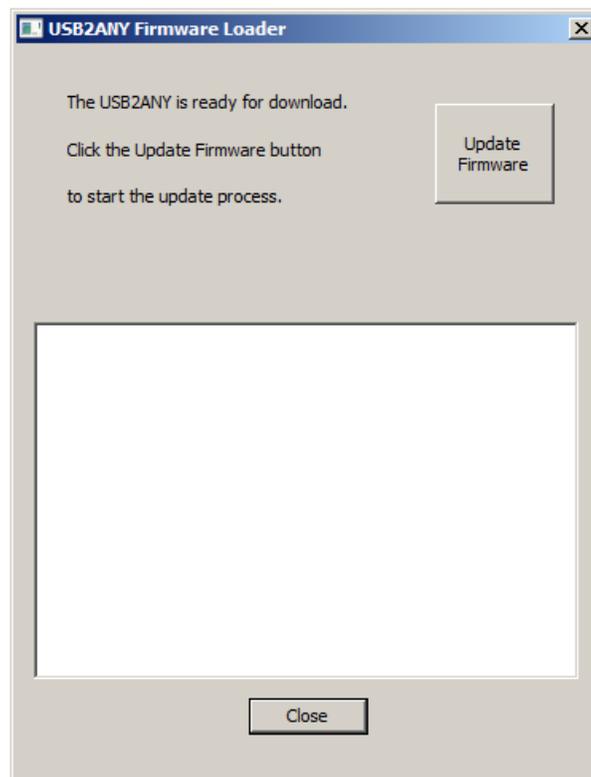


Figure 28. Update Firmware

5. Click the "Upgrade Firmware" button, the firmware will be upgrading. Click the "Close" button after it is done.

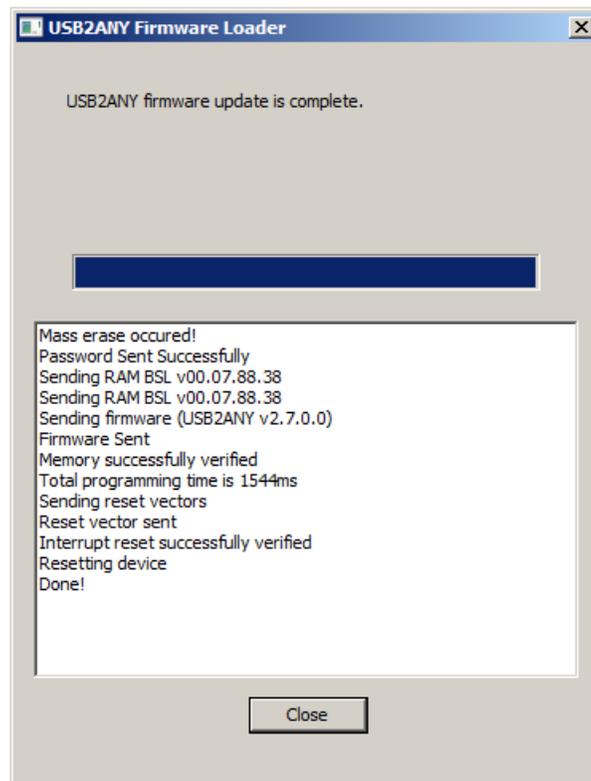


Figure 29. Firmware Update Completed

6. Check the USB connection in TICS Pro by clicking USB communications → Interface. Make sure the USB Connected button is turned green.

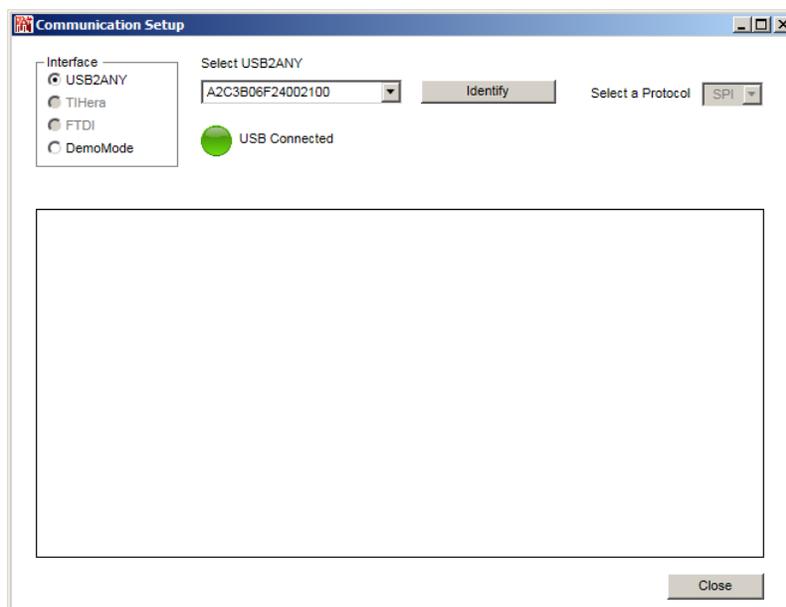


Figure 30. USB Communications

Using Different Reference Clock

There are different options to provide a reference clock to LMX2492EVM. By default, the EVM is configured for the on-board single-ended XO clock. To use external clock, R21 and R28 must be removed. If external differential clock is desired, OSCin* SMA connector is required.

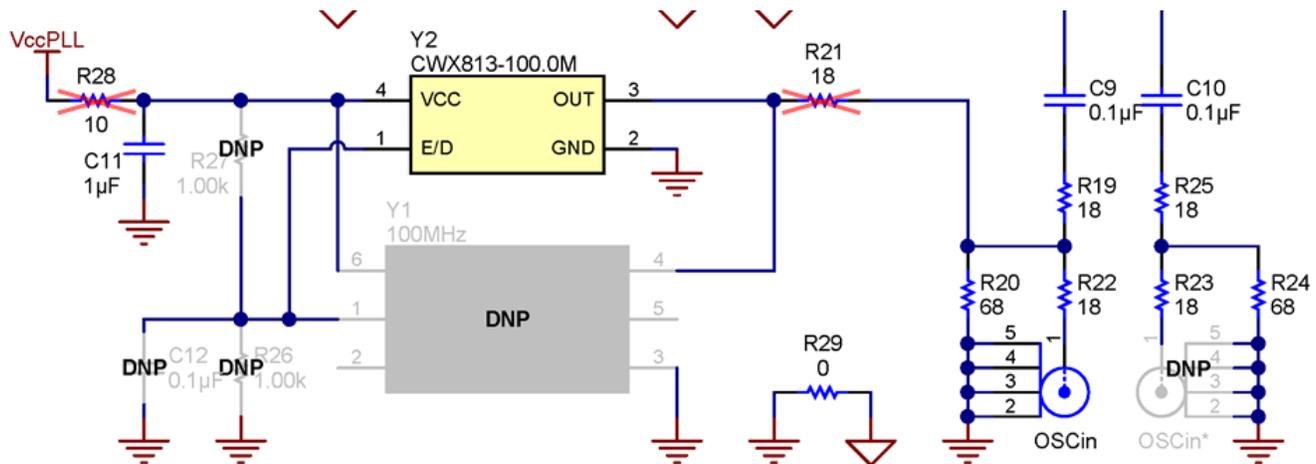


Figure 31. Reference Clock Input Configuration

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from D Revision (September 2015) to E Revision	Page
• Changed to use on-board XO	4
• Changed to use TICS Pro to program the device.....	4
• Changed VCO frequency and VCO gain.....	6
• Changed U2 part number.....	17
• Added Appendix A.....	19
• Added Appendix B.....	22

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CAUTION

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NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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