DAC128S085 12-Bit Micro-Power OCTAL Digital-to-Analog Converter With Rail-to-Rail Outputs

1 Features

- Ensured Monotonicity
- Low Power Operation
- Rail-to-Rail Voltage Output
- Daisy-Chain Capability
- Power-on Reset to 0 V
- Simultaneous Output Updating
- Individual Channel Power-Down Capability
- Wide Power Supply Range (2.7 V to 5.5 V)
- Dual Reference Voltages With Range of 0.5 V to V_A
- Operating Temperature Range of −40°C to 125°C
- Smallest Package in the Industry
- Resolution 12 Bits
- INL ±8 LSB (Maximum)
- DNL 0.75 / −0.4 LSB (Maximum)
- Settling Time 8.5 µs (Maximum)
- Zero Code Error 15 mV (Maximum)
- Full-Scale Error −0.75 %FSR (Maximum)
- Supply Power
  - 1.95 mW (3 V) / 4.85 mW (5 V) Typical
  - Power Down 0.3 µW (3 V) / 1 µW (5 V) Typical

2 Applications

- Battery-Powered Instruments
- Digital Gain and Offset Adjustment
- Programmable Voltage and Current Sources
- Programmable Attenuators
- Voltage Reference for ADCs
- Sensor Supply Voltage
- Range Detectors

3 Description

The DAC128S085 is a full-featured, general-purpose OCTAL 12-bit voltage-output digital-to-analog converter (DAC) that can operate from a single 2.7-V to 5.5-V supply and consumes 1.95 mW at 3 V and 4.85 mW at 5 V. The DAC128S085 is packaged in a 16-lead WQFN package and a 16-lead TSSOP package. The WQFN package makes the DAC128S085 the smallest OCTAL DAC in its class. The on-chip output amplifiers allow rail-to-rail output swing, and the 3-wire serial interface operates at clock rates up to 40 MHz over the entire supply voltage range. Competitive devices are limited to 25-MHz clock rates at supply voltages in the 2.7-V to 3.6-V range. The serial interface is compatible with standard SPI™, QSPI, MICROWIRE, and DSP interfaces. The DAC128S085 also offers daisy-chain operation, where an unlimited number of DAC128S085s can be updated simultaneously using a single serial interface.

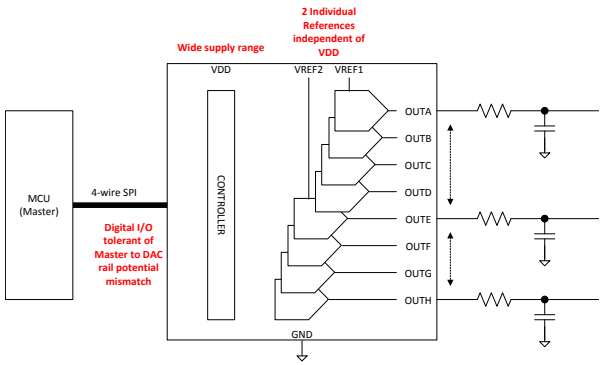
There are two references for the DAC128S085. One reference input serves channels A through D, while the other reference serves channels E through H. Each reference can be set independently between 0.5 V and V_A, providing the widest possible output dynamic range. The DAC128S085 has a 16-bit input shift register that controls the mode of operation, the power-down condition, and the register/output value of the DAC channels. All eight DAC outputs can be updated simultaneously or individually.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC128S085	TSSOP (16)	5.00 mm × 4.4 mm
	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision G (January 2015) to Revision H **Page**

- Switched WQFN and TSSOP pinouts to their correct titles ... 4
- Re-drew TSSOP pinout as a square to better reflect mechanical packaging drawings ... 4

Changes from Revision F (March 2013) to Revision G **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision E (March 2013) to Revision F **Page**

- Changed layout of National Data Sheet to TI format ... 23

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5 Description (continued)

A power-on reset circuit ensures that the DAC outputs power up to zero volts and remain there until there is a valid write to the device. The power-down feature of the DAC128S085 allows each DAC to be independently powered with three different termination options. With all the DAC channels powered down, power consumption reduces to less than 0.3 µW at 3 V and less than 1 µW at 5 V. The low power consumption and small packages of the DAC128S085 make it an excellent choice for use in battery-operated equipment.

The DAC128S085 is one of a family of pin-compatible DACs, including the 8-bit DAC088S085 and the 10-bit DAC108S085. All three parts are offered with the same pinout, allowing system designers to select a resolution appropriate for their application without redesigning their printed circuit board. The DAC128S085 operates over the extended industrial temperature range of −40°C to 125°C.

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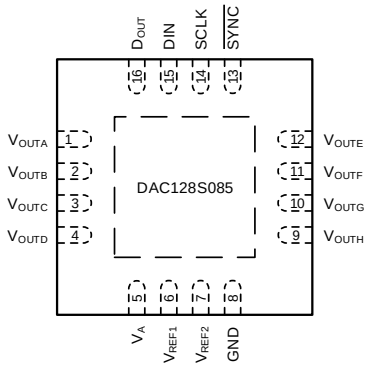
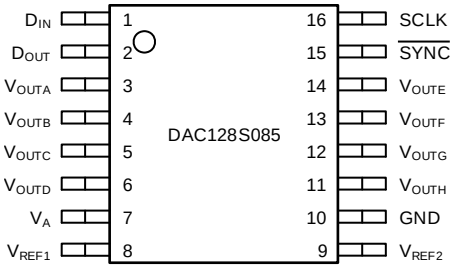
6 Pin Configuration and Functions

RGH Package
16-Pin WQFN
(Top View)



PW Package
16-Pin TSSOP
(Top View)



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TSSOP NO.	WQFN NO.		
D_{IN}	1	15	Digital Input	Serial Data Input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{SYNC}$.
D_{OUT}	2	16	Digital Output	Serial Data Output. D_{OUT} is utilized in daisy chain operation and is connected directly to a D_{IN} pin on another DAC128S085. Data is not available at D_{OUT} unless $\overline{SYNC}$ remains low for more than 16 SCLK cycles.
GND	10	8	Ground	Ground reference for all on-chip circuitry.
SCLK	16	14	Digital Input	Serial Clock Input. Data is clocked into the input shift register on the falling edges of this pin.
$\overline{SYNC}$	15	13	Digital Input	Frame Synchronization Input. When this pin goes low, data is written into the DAC's input shift register on the falling edges of SCLK. After the 16th falling edge of SCLK, a rising edge of $\overline{SYNC}$ causes the DAC to be updated. If $\overline{SYNC}$ is brought high before the 15th falling edge of SCLK, the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
V_A	7	5	Supply	Power supply input. Must be decoupled to GND.
V_{OUTA}	3	1	Analog Output	Channel A Analog Output Voltage.
V_{OUTB}	4	2	Analog Output	Channel B Analog Output Voltage.
V_{OUTC}	5	3	Analog Output	Channel C Analog Output Voltage.
V_{OUTD}	6	4	Analog Output	Channel D Analog Output Voltage.
V_{OUTE}	14	12	Analog Output	Channel E Analog Output Voltage.
V_{OUTF}	13	11	Analog Output	Channel F Analog Output Voltage.
V_{OUTG}	12	10	Analog Output	Channel G Analog Output Voltage.
V_{OUTH}	11	9	Analog Output	Channel H Analog Output Voltage.
V_{REF1}	8	6	Analog Input	Unbuffered reference voltage shared by Channels A, B, C, and D. Must be decoupled to GND.
V_{REF2}	9	7	Analog Input	Unbuffered reference voltage shared by Channels E, F, G, and H. Must be decoupled to GND.
PAD (WQFN only)	—	17	Ground	Exposed die attach pad can be connected to ground or left floating. Soldering the pad to the PCB offers optimal thermal performance and enhances package self-alignment during reflow.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Supply Voltage, V_A		6.5	V
Voltage on any Input Pin	−0.3	6.5	V
Input Current at Any Pin(3)		10	mA
Package Input Current(3)		30	mA
Power Consumption at T_A = 25°C		See (4)	
Junction Temperature		150	°C
Storage Temperature, T_{stg}	−65	150	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recomended Operating Ratings* indicate conditions for which the device is functional, but do not specify specific performance limits. For ensured specifications and test conditions, see *Electrical Characteristics*. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the *Absolute Maximum Ratings* is not recommended.
(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(3) When the input voltage at any pin exceeds 5.5 V or is less than GND, the current at that pin should be limited to 10 mA. The 30-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to three.
(4) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance ($R_{\theta JA}$), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / R_{\theta JA}$. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (for example, when input or output pins are driven beyond the operating ratings, or the power supply polarity is reversed). Such conditions should always be avoided.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model	±250	

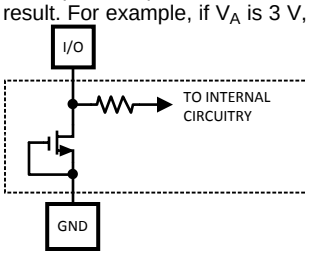
(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating Temperature Range		−40 ≤ T_A ≤ +125	°C
Supply Voltage, V_A	2.7	5.5	V
Reference Voltage, $V_{REF1,2}$	0.5	V_A	V
Digital Input Voltage(1)	0.0	5.5	V
Output Load	0	1500	pF
SCLK Frequency		40	MHz

(1) The inputs are protected as shown below. Input voltage magnitudes up to 5.5 V, regardless of V_A, will not cause errors in the conversion result. For example, if V_A is 3 V, the digital input pins can be driven with a 5-V logic device.



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7.4 Thermal Information

THERMAL METRIC(1)		DAC128S085		UNIT
		PW (TSSOP)	RGH (WQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98	34	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31	25	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43	11	
φ_{JT}	Junction-to-top characterization parameter	2	0.2	
φ_{JB}	Junction-to-board characterization parameter	43	11	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, $V_{REF1} = V_{REF2} = V_A$, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are at T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
STATIC PERFORMANCE						
	Resolution	$T_{MIN} \le T_A \le T_{MAX}$	12			Bits
	Monotonicity	$T_{MIN} \le T_A \le T_{MAX}$	12			Bits
INL	Integral Non-Linearity			±2		LSB
		$T_{MIN} \le T_A \le T_{MAX}$			±8	
DNL	Differential Non-Linearity			0.15		LSB
		$T_{MIN} \le T_A \le T_{MAX}$			0.75	
				−0.09		LSB
		$T_{MIN} \le T_A \le T_{MAX}$	−0.4			
ZE	Zero Code Error	I_{OUT} = 0		+5		mV
		$T_{MIN} \le T_A \le T_{MAX}$			15	
FSE	Full-Scale Error	I_{OUT} = 0		−0.1%		FSR
		$T_{MIN} \le T_A \le T_{MAX}$			−0.75%	
GE	Gain Error			−0.2%		FSR
		$T_{MIN} \le T_A \le T_{MAX}$			−1 %	
ZCED	Zero Code Error Drift			−20		µV/°C
TC GE	Gain Error Tempco			−1		ppm/°C
OUTPUT CHARACTERISTICS						
	Output Voltage Range	$T_{MIN} \le T_A \le T_{MAX}$	0		$V_{REF1,2}$	V
I_{OZ}	High-Impedance Output Leakage Current(2)	$T_{MIN} \le T_A \le T_{MAX}$			±1	µA
ZCO	Zero Code Output	V_A = 3 V, I_{OUT} = 200 µA		10		mV
		V_A = 3 V, I_{OUT} = 1 mA		45		mV
		V_A = 5 V, I_{OUT} = 200 µA		8		mV
		V_A = 5 V, I_{OUT} = 1 mA		34		mV
FSO	Full Scale Output	V_A = 3 V, I_{OUT} = 200 µA		2.984		V
		V_A = 3 V, I_{OUT} = 1 mA		2.933		V
		V_A = 5 V, I_{OUT} = 200 µA		4.987		V
		V_A = 5 V, I_{OUT} = 1 mA		4.955		V

(1) Test limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(2) This parameter is ensured by design and/or characterization and is not tested in production.

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Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, $V_{REF1} = V_{REF2} = V_A$, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are at T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
I_{OS}	Output Short Circuit Current (source)(3)	V_A = 3 V, V_{OUT} = 0 V, Input Code = FFFh		−50		mA
		V_A = 5 V, V_{OUT} = 0 V, Input Code = FFFh		−60		mA
I_{OS}	Output Short Circuit Current (sink)(3)	V_A = 3 V, V_{OUT} = 3 V, Input Code = 000h		50		mA
		V_A = 5 V, V_{OUT} = 5 V, Input Code = 000h		70		mA
I_O	Continuous Output Current per channel(2)	T_A = 105°C $T_{MIN} \le T_A \le T_{MAX}$			10	mA
		T_A = 125°C $T_{MIN} \le T_A \le T_{MAX}$			6.5	mA
C_L	Maximum Load Capacitance	R_L = ∞		1500		pF
		R_L = 2 kΩ		1500		pF
Z_{OUT}	DC Output Impedance			8		Ω
REFERENCE INPUT CHARACTERISTICS						
VREF1,2	Input Range Minimum			0.5		V
		$T_{MIN} \le T_A \le T_{MAX}$	2.7			
	Input Range Maximum	$T_{MIN} \le T_A \le T_{MAX}$			V_A	V
	Input Impedance			30		kΩ
LOGIC INPUT CHARACTERISTICS						
I_{IN}	Input Current(2)	$T_{MIN} \le T_A \le T_{MAX}$			±1	µA
V_{IL}	Input Low Voltage	V_A = 2.7 V to 3.6 V		1		V
		$T_{MIN} \le T_A \le T_{MAX}$			0.6	
		V_A = 4.5 V to 5.5 V		1.1		V
					0.8	
V_{IH}	Input High Voltage	V_A = 2.7 V to 3.6 V		1.4		V
		$T_{MIN} \le T_A \le T_{MAX}$	2.1			
		V_A = 4.5 V to 5.5 V		2		V
		$T_{MIN} \le T_A \le T_{MAX}$	2.4			
C_{IN}	Input Capacitance(2)	$T_{MIN} \le T_A \le T_{MAX}$			3	pF

(3) This parameter does not represent a condition which the DAC can sustain continuously. See the continuous output current specification for the maximum DAC output current per channel.

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Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, $V_{REF1} = V_{REF2} = V_A$, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are at T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP	MAX(1)	UNIT
POWER REQUIREMENTS							
V_A	Supply Voltage Minimum	$T_{MIN} \le T_A \le T_{MAX}$		2.7			V
	Supply Voltage Maximum	$T_{MIN} \le T_A \le T_{MAX}$				5.5	V
I_N	Normal Supply Current for supply pin V_A	f_{SCLK} = 30 MHz, output unloaded	V_A = 2.7 V to 3.6 V		460		µA
			$T_{MIN} \le T_A \le T_{MAX}$			560	
			V_A = 4.5 V to 5.5 V		650		µA
						830	
	Normal Supply Current for V_{REF1} or V_{REF2}	f_{SCLK} = 30 MHz, output unloaded	V_A = 2.7 V to 3.6 V		95		µA
			$T_{MIN} \le T_A \le T_{MAX}$			130	
			V_A = 4.5 V to 5.5 V		160		µA
						220	
I_{ST}	Static Supply Current for supply pin V_A	f_{SCLK} = 0, output unloaded	V_A = 2.7 V to 3.6 V		370		µA
			V_A = 4.5 V to 5.5 V		440		µA
	Static Supply Current for V_{REF1} or V_{REF2}	f_{SCLK} = 0, output unloaded	V_A = 2.7 V to 3.6 V		95		µA
			V_A = 4.5 V to 5.5 V		160		µA
I_{PD}	Total Power Down Supply Current for all PD Modes (2)	f_{SCLK} = 30 MHz, SYNC = V_A and D_{IN} = 0V after PD mode loaded	V_A = 2.7 V to 3.6 V		0.2		µA
						1.5	
			V_A = 4.5 V to 5.5 V		0.5		µA
			$T_{MIN} \le T_A \le T_{MAX}$			3	
		f_{SCLK} = 0, SYNC = V_A and D_{IN} = 0V after PD mode loaded	V_A = 2.7 V to 3.6 V		0.1		µA
			$T_{MIN} \le T_A \le T_{MAX}$			1	
			V_A = 4.5 V to 5.5 V		0.2		µA
			$T_{MIN} \le T_A \le T_{MAX}$			2	
P_N	Total Power Consumption (output unloaded)	f_{SCLK} = 30 MHz output unloaded	V_A = 2.7 V to 3.6 V		1.95		mW
			$T_{MIN} \le T_A \le T_{MAX}$			3	
			V_A = 4.5 V to 5.5 V		4.85		mW
			$T_{MIN} \le T_A \le T_{MAX}$			7	
		f_{SCLK} = 0 output unloaded	V_A = 2.7 V to 3.6 V		1.68		mW
			V_A = 4.5 V to 5.5 V		3.80		mW

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Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, $V_{REF1} = V_{REF2} = V_A$, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are at T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP	MAX(1)	UNIT
P_{PD}	Total Power Consumption in all PD Modes, (2)	f_{SCLK} = 30 MHz, SYNC = V_A and D_{IN} = 0V after PD mode loaded	V_A = 2.7 V to 3.6 V		0.6		µW
			$T_{MIN} \le T_A \le T_{MAX}$			5.4	
			V_A = 4.5V to 5.5V		2.5		µW
			$T_{MIN} \le T_A \le T_{MAX}$			16.5	
		f_{SCLK} = 0, SYNC = V_A and D_{IN} = 0V after PD mode loaded	V_A = 2.7 V to 3.6 V		0.3		µW
			$T_{MIN} \le T_A \le T_{MAX}$			3.6	
			V_A = 4.5 V to 5.5 V		1		µW
			$T_{MIN} \le T_A \le T_{MAX}$			11	

7.6 AC and Timing Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, $V_{REF1,2} = V_A$, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are at T_A = 25°C, unless otherwise specified.

			MIN(1)	NOM	MAX(1)	UNIT
f_{SCLK}	SCLK Frequency			40		MHz
		$T_{MIN} \le T_A \le T_{MAX}$			30	
t_s	Output Voltage Settling Time (2)	400h to C00h code change R_L = 2 kΩ, C_L = 200 pF		6		µs
		$T_{MIN} \le T_A \le T_{MAX}$			8.5	
SR	Output Slew Rate			1		V/µs
GI	Glitch Impulse	Code change from 800h to 7FFh		40		nV-sec
DF	Digital Feedthrough			0.5		nV-sec
DC	Digital Crosstalk			0.5		nV-sec
CROSS	DAC-to-DAC Crosstalk			1		nV-sec
MBW	Multiplying Bandwidth	$V_{REF1,2}$ = 2.5 V ± 2 Vpp		360		kHz
THD+N	Total Harmonic Distortion Plus Noise	$V_{REF1,2}$ = 2.5 V ± 0.5 Vpp 100 Hz < f_{IN} < 20 kHz		−80		dB
ONSD	Output Noise Spectral Density	DAC Code = 800 h, 10 kHz		40		nV/sqrt (Hz)
ON	Output Noise	BW = 30 kHz		14		µV
t_{WU}	Wake-Up Time	V_A = 3 V		3		µsec
		V_A = 5 V		20		µsec
$1/f_{SCLK}$	SCLK Cycle Time. See Figure 1			25		ns
		$T_{MIN} \le T_A \le T_{MAX}$	33			
t_{CH}	SCLK High time. See Figure 1			7		ns
		$T_{MIN} \le T_A \le T_{MAX}$	10			
t_{CL}	SCLK Low Time. See Figure 1			7		ns
		$T_{MIN} \le T_A \le T_{MAX}$	10			
t_{SS}	$\overline{SYNC}$ Set-up Time prior to SCLK Falling Edge. See Figure 1			3	1 / f_{SCLK} - 3	ns
		$T_{MIN} \le T_A \le T_{MAX}$	10			

(1) Test limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(2) This parameter is ensured by design and/or characterization and is not tested in production.

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AC and Timing Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, $V_{REF1,2} = V_A$, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are at T_A = 25°C, unless otherwise specified.

			MIN(1)	NOM	MAX(1)	UNIT
t_{DS}	Data Set-Up Time prior to SCLK Falling Edge. See Figure 1			1		ns
		$T_{MIN} \le T_A \le T_{MAX}$	2.5			
t_{DH}	Data Hold Time after SCLK Falling Edge. See Figure 1			1		ns
		$T_{MIN} \le T_A \le T_{MAX}$	2.5			
t_{SH}	SYNC Hold Time after the 16th falling edge of SCLK. See Figure 1			0	1 / f_{SCLK} - 3	ns
		$T_{MIN} \le T_A \le T_{MAX}$	3			
t_{SYNC}	$\overline{SYNC}$ High Time. See Figure 1			5		ns
		$T_{MIN} \le T_A \le T_{MAX}$	15			

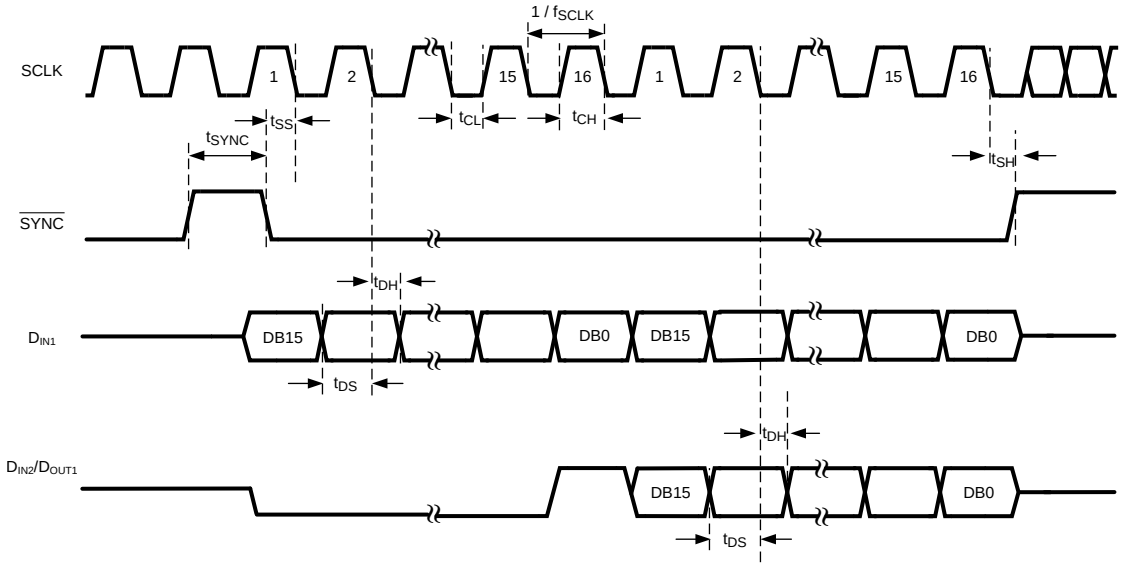

Figure 1. Serial Timing Diagram

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7.7 Typical Characteristics

V_A = 2.7 V to 5.5 V, $V_{REF1,2} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, unless otherwise stated

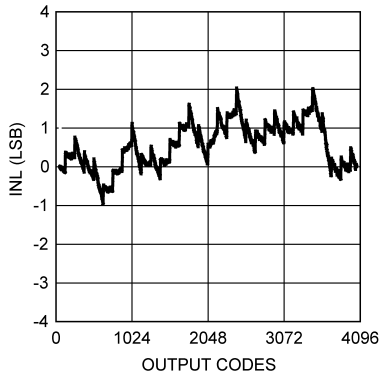

Figure 2. INL vs Code

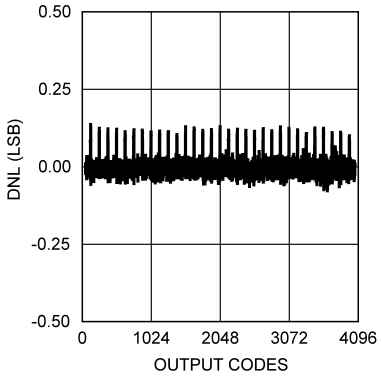

Figure 3. DNL vs Code

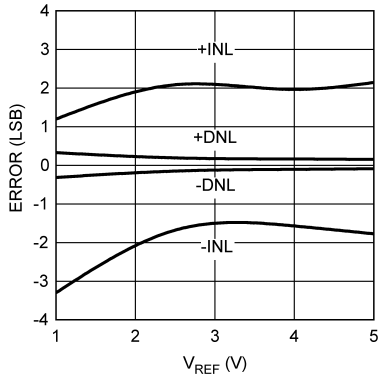

Figure 4. INL / DNL vs V_{REF}

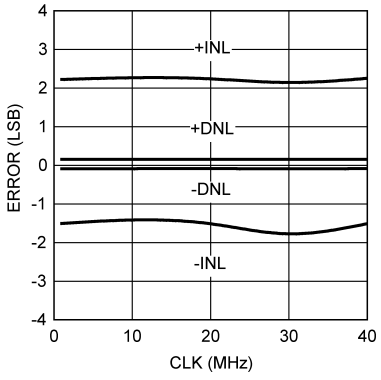

Figure 5. INL / DNL vs F_{SCLK}

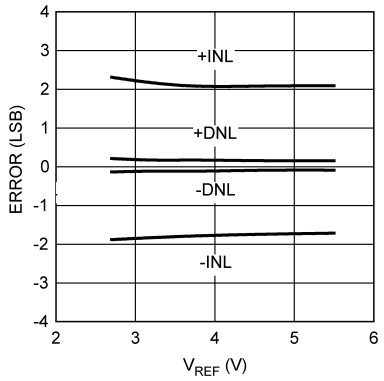

Figure 6. INL / DNL vs V_A

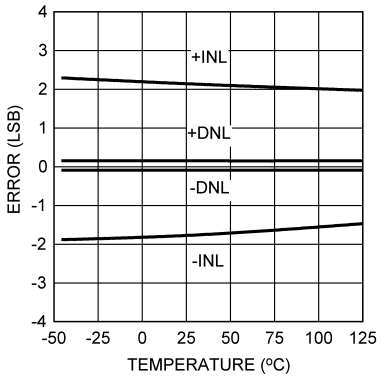

Figure 7. INL / DNL vs Temperature

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Typical Characteristics (continued)

V_A = 2.7 V to 5.5 V, $V_{REF1,2} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, unless otherwise stated

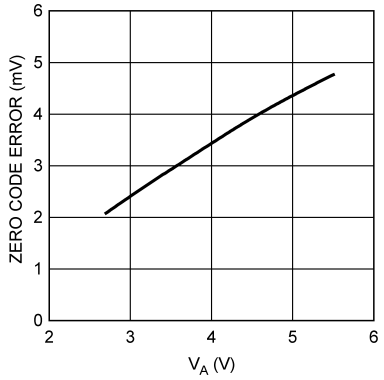

Figure 8. Zero Code Error vs V_A

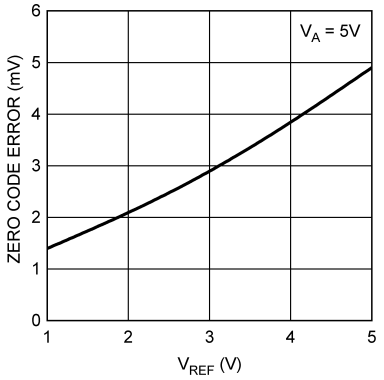

Figure 9. Zero Code Error vs V_{REF}

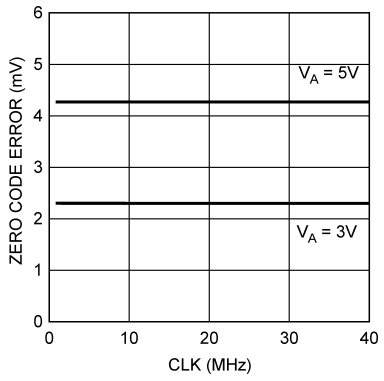

Figure 10. Zero Code Error vs F_{SCLK}

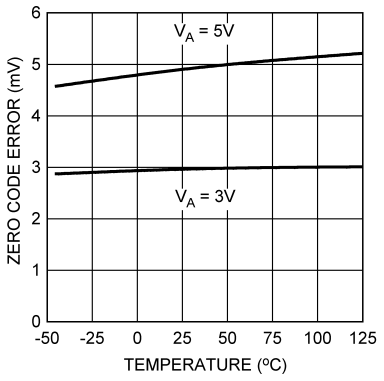

Figure 11. Zero Code Error vs Temperature

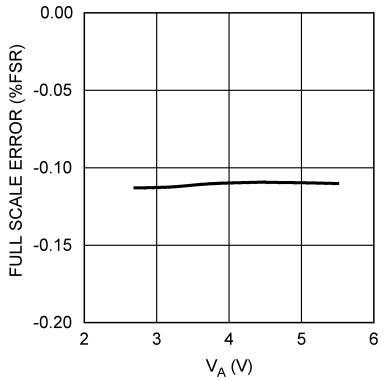

Figure 12. Full-Scale Error vs V_A

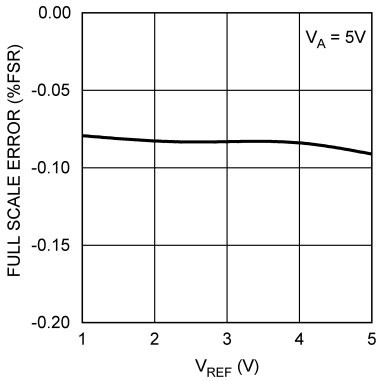

Figure 13. Full-Scale Error vs V_{REF}

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Typical Characteristics (continued)

V_A = 2.7 V to 5.5 V, $V_{REF1,2} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, unless otherwise stated

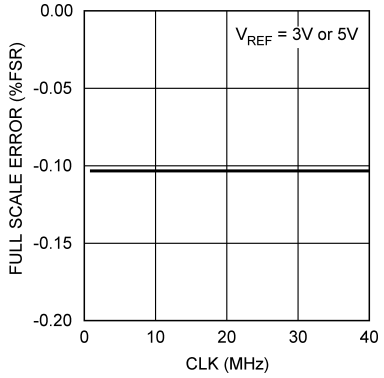

Figure 14. Full-Scale Error vs F_{SCLK}

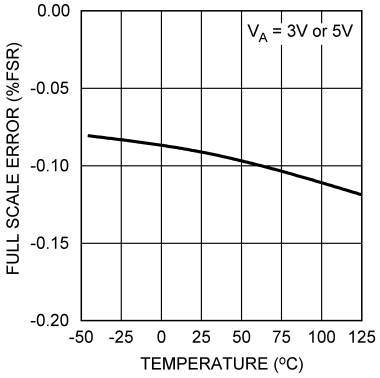

Figure 15. Full-Scale Error vs Temperature

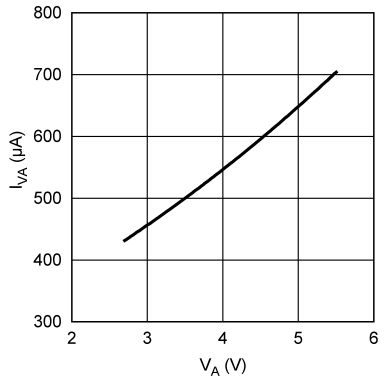

Figure 16. I_{VA} vs V_A

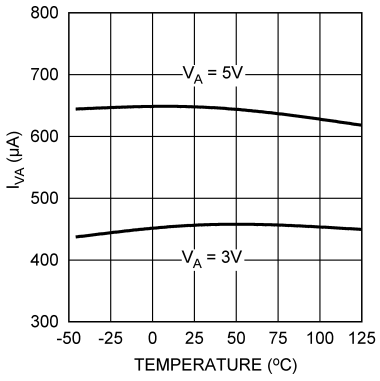

Figure 17. I_{VA} vs Temperature

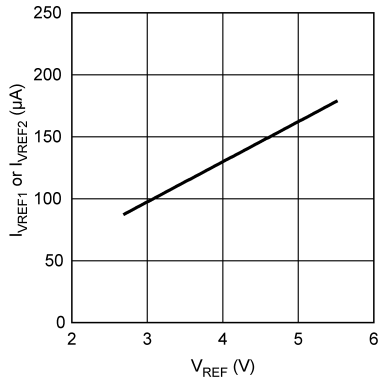

Figure 18. I_{VREF} vs V_{REF}

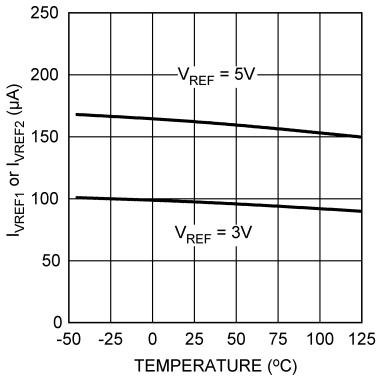

Figure 19. I_{VREF} vs Temperature

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Typical Characteristics (continued)

V_A = 2.7 V to 5.5 V, $V_{REF1,2} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, unless otherwise stated

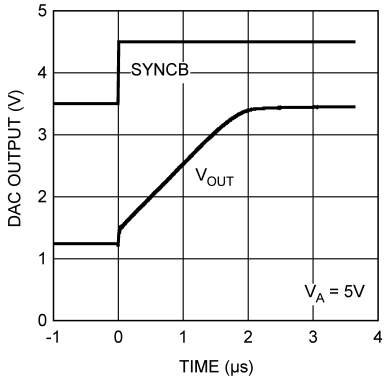

Figure 20. Settling Time

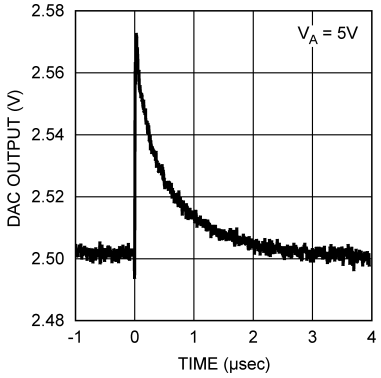

Figure 21. Glitch Response

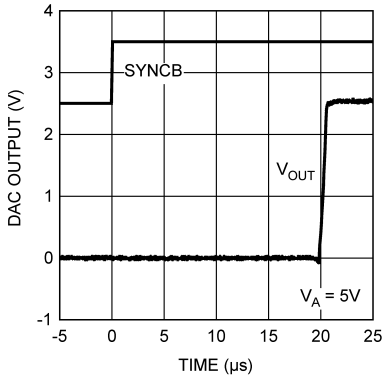

Figure 22. Wake-Up Time

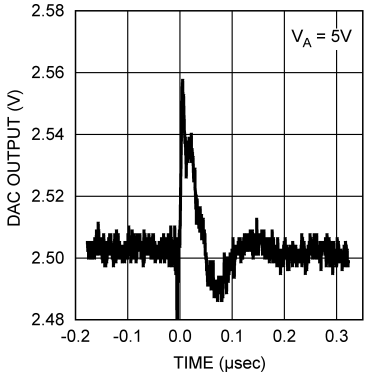

Figure 23. DAC-to-DAC Crosstalk

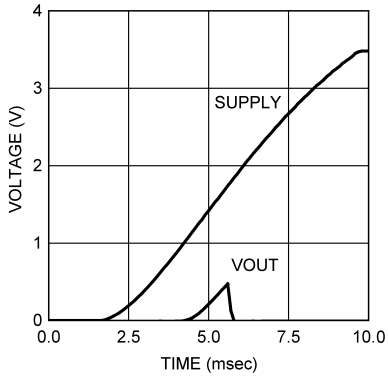

Figure 24. Power-On Reset

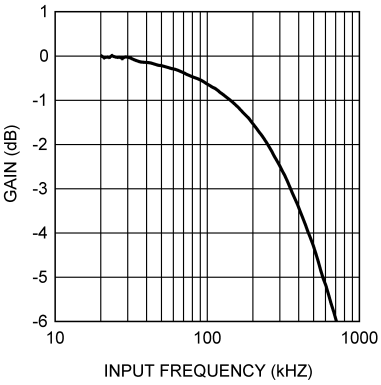

Figure 25. Multiplying Bandwidth

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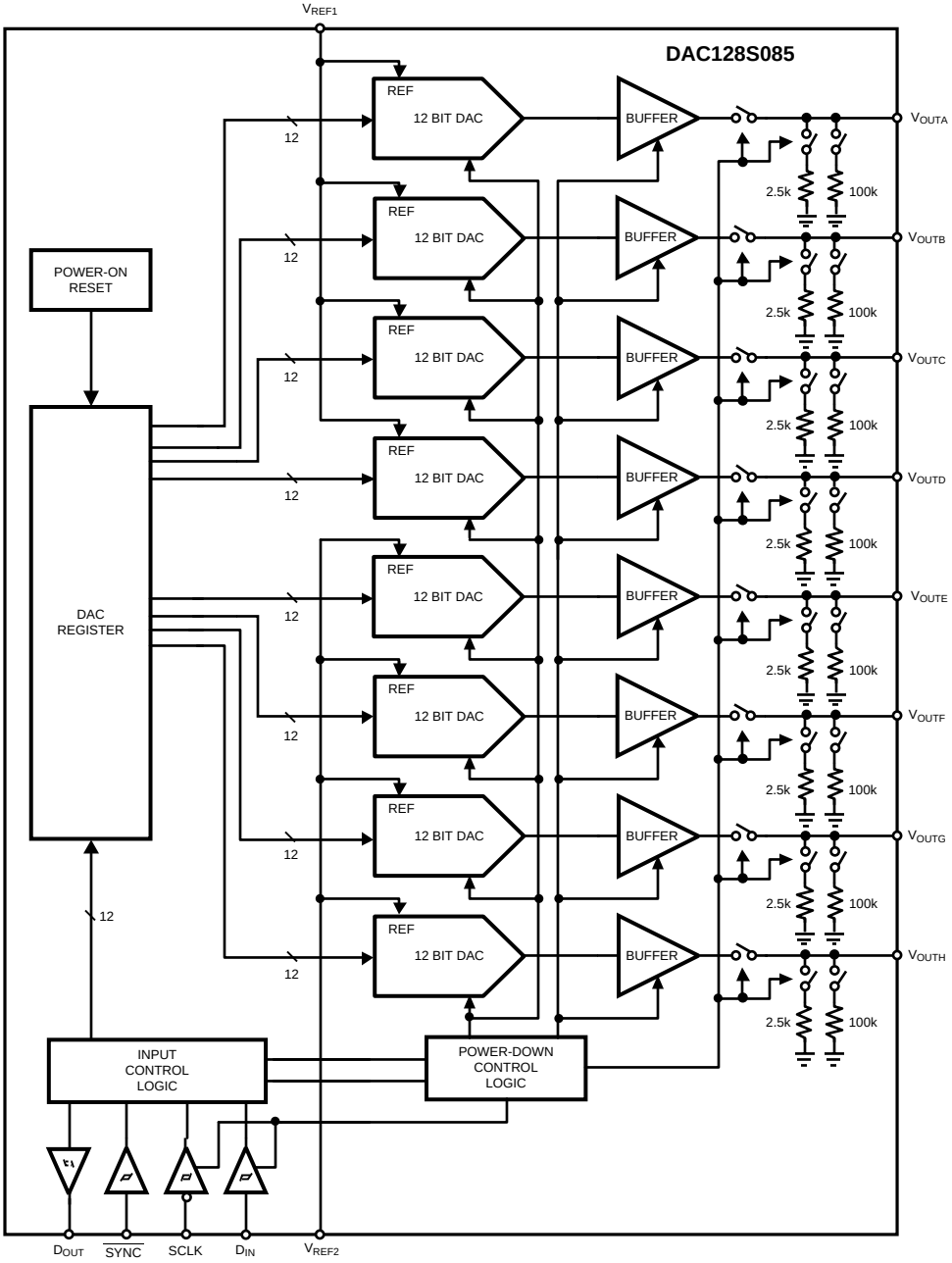
8 Detailed Description

8.1 Overview

The DAC128S085 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings followed by an output buffer. The reference voltages are externally applied at V_{REF1} for DAC channels A through D, and V_{REF2} for DAC channels E through H.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DAC Architecture

For simplicity, a single resistor string is shown in Figure 26. This string consists of 4096 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. The input coding is straight binary with an ideal output voltage of:

$$V_{OUTA,B,C,D} = V_{REF1} \times (D / 4096) \quad (1)$$

where

- *D* is the decimal equivalent of the binary code that is loaded into the DAC register.

$$V_{OUTE,F,G,H} = V_{REF2} \times (D / 4096) \quad (2)$$

D can take on any value between 0 and 4095. This configuration ensures that the DAC is monotonic.

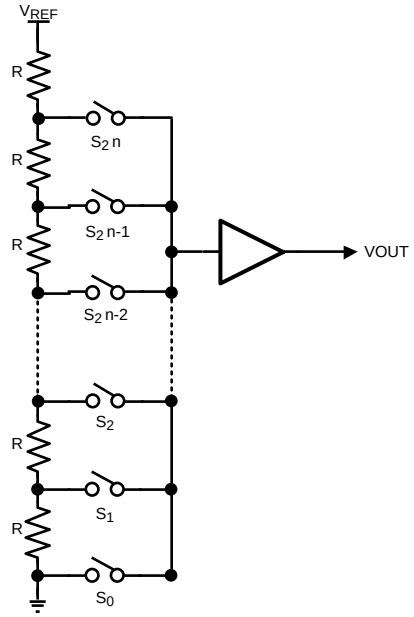


Figure 26. DAC Resistor String

Because all eight DAC channels of the DAC128S085 can be controlled independently, each channel consists of a DAC register and a 12-bit DAC. Figure 27 is a simple block diagram of an individual channel in the DAC128S085. Depending on the mode of operation, data written into a DAC register causes the 12-bit DAC output to be updated, or an additional command is required to update the DAC output. Further description of the modes of operation can be found in *Serial Interface*.

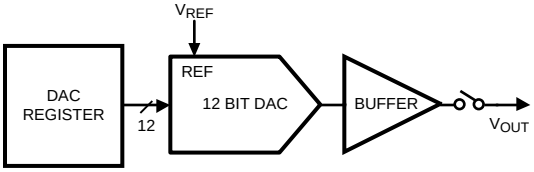


Figure 27. Single-Channel Block Diagram

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Feature Description (continued)

8.3.2 Output Amplifiers

The output amplifiers are rail-to-rail, providing an output voltage range of 0 V to V_A when the reference is V_A. All amplifiers, including rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0 V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. However, if the reference is less than V_A, only the lowest codes experience a loss in linearity.

The output amplifiers can drive a load of 2 kΩ in parallel with 1500 pF to ground or to V_A. The zero-code and full-scale outputs for given load currents are available in the *Electrical Characteristics*.

8.3.3 Reference Voltage

The DAC128S085 uses dual external references, V_{REF1} and V_{REF2}, which are shared by channels A, B, C, D and channels E, F, G, H, respectively. The reference pins are not buffered and have an input impedance of 30 kΩ. TI recommends driving V_{REF1} and V_{REF2} by voltage sources with low output impedance. The reference voltage range is 0.5 V to V_A, providing the widest possible output dynamic range.

8.3.4 Serial Interface

The three-wire interface is compatible with SPI, QSPI, and MICROWIRE, as well as most DSPs, and operates at clock rates up to 40 MHz. A valid serial frame contains 16 falling edges of SCLK. See Table 1 for information on a write sequence.

A write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Once $\overline{\text{SYNC}}$ is low, the data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. To avoid mis-clocking data into the shift register, it is critical that $\overline{\text{SYNC}}$ not be brought low on a falling edge of SCLK (see minimum and maximum setup times for $\overline{\text{SYNC}}$ in *AC and Timing Characteristics* and Figure 28). On the 16th falling edge of SCLK, the last data bit is clocked into the register. The write sequence is concluded by bringing the $\overline{\text{SYNC}}$ line high. Once $\overline{\text{SYNC}}$ is high, the programmed function (a change in the DAC channel address, mode of operation, or register contents) is executed. To avoid mis-clocking data into the shift register, it is critical that $\overline{\text{SYNC}}$ be brought high between the 16th and 17th falling edges of SCLK (see minimum and maximum hold times for $\overline{\text{SYNC}}$ in *AC and Timing Characteristics* and Figure 28).

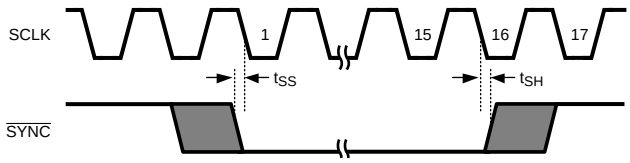

Figure 28. $\overline{\text{CS}}$ Setup and Hold Times

If $\overline{\text{SYNC}}$ is brought high before the 15th falling edge of SCLK, the write sequence is aborted and the data that has been shifted into the input register is discarded. If $\overline{\text{SYNC}}$ is held low beyond the 17th falling edge of SCLK, the serial data presented at D_{IN} will begin to be output on D_{OUT}. More information on this mode of operation can be found in *Daisy-Chain Operation*. In either case, $\overline{\text{SYNC}}$ must be brought high for the minimum specified time before the next write sequence is initiated with a falling edge of $\overline{\text{SYNC}}$.

Since the D_{IN} buffer draws more current when it is high, it should be idled low between write sequences to minimize power consumption. On the other hand, $\overline{\text{SYNC}}$ should be idled high to avoid the activation of daisy chain operation where D_{OUT} is active.

8.3.5 Daisy-Chain Operation

Daisy-chain operation allows communication with any number of DAC128S085s using a single serial interface. As long as the correct number of data bits are input in a write sequence (multiple of sixteen bits), a rising edge of $\overline{\text{SYNC}}$ will properly update all DACs in the system.

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Feature Description (continued)

To support multiple devices in a daisy chain configuration, SCLK and $\overline{SYNC}$ are shared across all DAC128S085s and D_{OUT} of the first DAC in the chain is connected to D_{IN} of the second. Figure 29 shows three DAC128S085s connected in daisy chain fashion. Similar to a single channel write sequence, the conversion for a daisy chain operation begins on a falling edge of $\overline{SYNC}$ and ends on a rising edge of $\overline{SYNC}$. A valid write sequence for n devices in a chain requires n times 16 falling edges to shift the entire input data stream through the chain. Daisy chain operation is ensured for a maximum SCLK speed of 30 MHz.

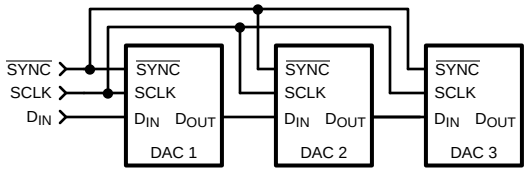

Figure 29. Daisy-Chain Configuration

The serial data output pin, D_{OUT}, is available on the DAC128S085 to allow daisy-chaining of multiple DAC128S085 devices in a system. In a write sequence, D_{OUT} remains low for the first 14 falling edges of SCLK before going high on the 15th falling edge. Subsequently, the next 16 falling edges of SCLK will output the first 16 data bits entered into D_{IN}. Figure 30 shows the timing of 3 DAC128S085s in Figure 29. In this instance, It takes 48 falling edges of SCLK followed by a rising edge of $\overline{SYNC}$ to load all three DAC128S085s with the appropriate register data. On the rising edge of $\overline{SYNC}$, the programmed function is executed in each DAC128S085 simultaneously.

When connecting multiple devices in a daisy-chain configuration, it is important to note that the DAC128S085 will update the D_{OUT} signal on the falling edge of SCLK, and this will be sampled by the next DAC in the daisy chain on the next falling edge of the clock. Ensure that the timing requirements are met for proper operation. Specifically, pay attention to the data hold time after the SCLK falling (t_{DH}) requirement. Improper layout or loading may delay the clock signal between devices. If delayed to the point that data changes prior to meeting the hold time requirement, incorrect data can be sampled. If the clock delay cannot be resolved, an alternative solution is to add a delay between the D_{OUT} of one device and D_{IN} of the following device in the daisy chain. This increases the hold time margin and allows for correct sampling. Be aware though, that the tradeoff with this fix is that too much delay eventually impacts the setup time.

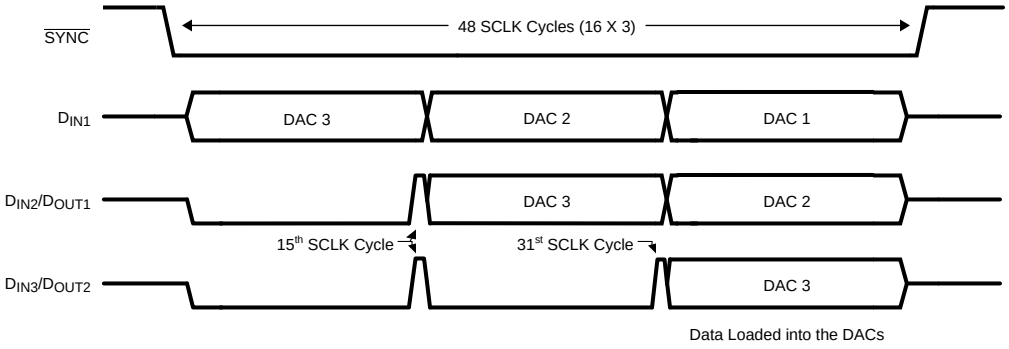

Figure 30. Daisy Chain Timing Diagram

8.3.6 DAC Input Data Update Mechanism

The DAC128S085 has two modes of operation, plus a few special command operations. The two modes of operation are Write Register Mode (WRM) and Write Through Mode (WTM). For the rest of this document, these modes will be referred to as WRM and WTM. The special command operations are separate from WRM and WTM because they can be called upon regardless of the current mode of operation. The mode of operation is controlled by the first four bits of the control register, DB15 through DB12. See Table 1 for a detailed summary.

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Feature Description (continued)

Table 1. Write Register and Write Through Modes

DB[15:12]	DB[11:0]	Description of Mode
1 0 0 0	X X X X X X X X X X X X	WRM: The registers of each DAC Channel can be written to without causing their outputs to change.
1 0 0 1	X X X X X X X X X X X X	WTM: Writing data to a channel's register causes the DAC output to change.

When the DAC128S085 first powers up, the DAC is in WRM. In WRM, the registers of each individual DAC channel can be written to without updating the DAC outputs. This is accomplished by setting DB15 to 0, specifying the DAC register to be written to in DB[14:12], and entering the new DAC register setting in DB[11:0] (see Table 2). The DAC128S085 remains in WRM until the mode of operation is changed to WTM. The mode of operation is changed from WRM to WTM by setting DB[15:12] to 1001. Once in WTM, writing data to a DAC channel register causes the DAC output to be updated as well. Changing a DAC channel register in WTM is accomplished in the same manner as in WRM. However, in WTM the DAC register and output are updated at the completion of the command (see Table 2). Similarly, the DAC128S085 remains in WTM until the mode of operation is changed to WRM by setting DB[15:12] to 1000.

Table 2. Commands Impacted by WRM and WTM

DB15	DB[14:12]	DB[11:0]	Description of Mode
0	0 0 0	D11 D10 ... D1 D0	WRM: D[11:0] written to ChA's data register only WTM: ChA's output is updated by data in D[11:0]
0	0 0 1	D11 D10 ... D1 D0	WRM: D[11:0] written to only the data register of ChB WTM: ChB's output is updated by data in D[11:0]
0	0 1 0	D11 D10 ... D1 D0	WRM: D[11:0] written to only the data register of ChC WTM: ChC's output is updated by data in D[11:0]
0	0 1 1	D11 D10 ... D1 D0	WRM: D[11:0] written only the data register of ChD WTM: ChD's output is updated by data in D[11:0]
0	1 0 0	D11 D10 ... D1 D0	WRM: D[11:0] written only the data register of ChE WTM: ChE's output is updated by data in D[11:0]
0	1 0 1	D11 D10 ... D1 D0	WRM: D[11:0] written only the data register of ChF WTM: ChF's output is updated by data in D[11:0]
0	1 1 0	D11 D10 ... D1 D0	WRM: D[11:0] written only the data register of ChG WTM: ChG's output is updated by data in D[11:0]
0	1 1 1	D11 D10 ... D1 D0	WRM: D[11:0] written only the data register of ChH WTM: ChH's output is updated by data in D[11:0]

The special command operations can be exercised at any time regardless of the mode of operation. There are three special command operations. The first command is exercised by setting data bits DB[15:12] to 1010. This allows the user to update multiple DAC outputs simultaneously to the values currently loaded in their respective control registers. This command is valuable if the user wants each DAC output to be at a different output voltage, but still have all the DAC outputs changed to their appropriate values simultaneously (see Table 3).

The second special command allows the user to alter the DAC output of channel A with a single write frame. This command is exercised by setting data bits DB[15:12] to 1011 and data bits DB[11:0] to the desired control register value. This command also causes the DAC outputs of the other channels to update to their current control register values. The user may choose to exercise this command to save a write sequence. For example, the user may wish to update several DAC outputs simultaneously, including channel A. To accomplish this task in the minimum number of write frames, the user would alter the control register values of all the DAC channels except channel A while operating in WRM. The last write frame would be used to exercise the special command *Channel A Write Mode*. In addition to updating the control register of channel A and output to a new value, all of the other channels would be updated as well. At the end of this sequence of write frames, the DAC128S085 would still be operating in WRM (see Table 3).

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The third special command allows the user to set all the DAC control registers and outputs to the same level. This command is commonly referred to as "broadcast" mode, as the same data bits are being broadcast to all of the channels simultaneously. This command is exercised by setting data bits DB[15:12] to 1100 and data bits DB[11:0] to the value that the user wishes to broadcast to all the DAC control registers. Once the command is exercised, each DAC output is updated by the new control register value. This command is frequently used to set all the DAC outputs to some known voltage such as 0 V, $V_{REF}/2$, or Full Scale. A summary of the commands can be found in Table 3.

Table 3. Special Command Operations

DB[15:12]	DB[11:0]	Description of Mode
1 0 1 0	X X X X H G F E D C B A	Update Select: The DAC outputs of the channels selected with a 1 in DB[7:0] are updated simultaneously to the values in their respective control registers.
1 0 1 1	D11 D10 ... D1 D0	Channel A Write: The control register and DAC output of channel A are updated to the data in DB[11:0]. The outputs of the other seven channels are also updated according to their respective control register values.
1 1 0 0	D11 D10 ... D1 D0	Broadcast: The data in DB[11:0] is written to all channel control registers and DAC output simultaneously.

8.3.7 Power-On Reset

The power-on reset circuit controls the output voltages of the eight DACs during power-up. Upon application of power, the DAC registers are filled with zeros and the output voltages are set to 0 V. The outputs remain at 0 V until a valid write sequence is made.

8.3.8 Transfer Characteristic

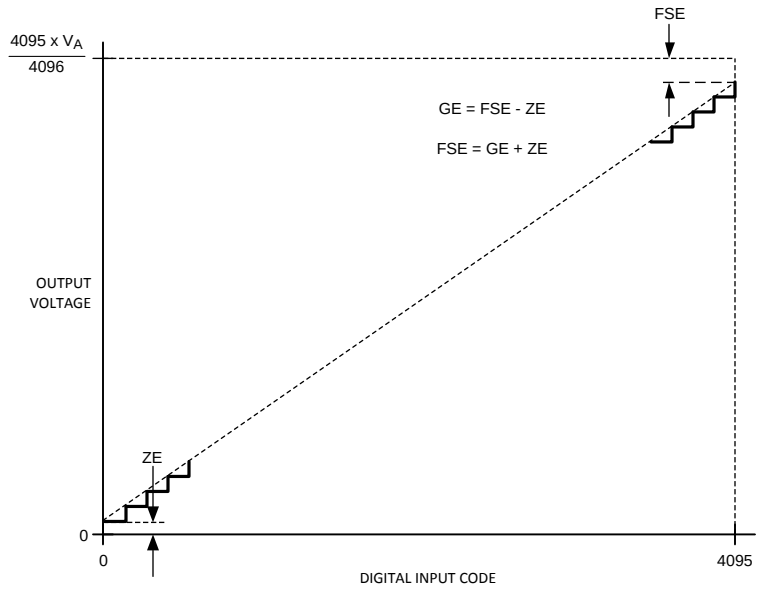

Figure 31. Input / Output Transfer Characteristic

8.4 Device Functional Modes

8.4.1 Power-Down Modes

The DAC128S085 has three power-down modes, where different output terminations can be selected (see Table 4). With all channels powered down, the supply current drops to 0.1 µA at 3 V and 0.2 µA at 5 V. By selecting the channels to be powered down in DB[7:0] with a 1, individual channels can be powered down separately, or multiple channels can be powered down simultaneously. The three different output terminations include high output impedance, 100 kΩ to ground, and 2.5 kΩ to ground.

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Device Functional Modes (continued)

The output amplifiers, resistor strings, and other linear circuitry are all shut down in any of the power-down modes. The bias generator, however, is only shut down if all the channels are placed in power-down mode. The contents of the DAC registers are unaffected when in power-down. Therefore, each DAC register maintains its value prior to the DAC128S085 being powered down unless it is changed during the write sequence that instructed it to recover from power down. Minimum power consumption is achieved in the power-down mode with $\overline{SYNC}$ idled high, D_{IN} idled low, and SCLK disabled. The time to exit power-down (Wake-Up Time) is typically 3 µsec at 3 V and 20 µsec at 5 V.

Table 4. Power-Down Modes

DB[15:12]	DB[11:8]	7	6	5	4	3	2	1	0	Output Impedance
1 1 0 1	X X X X	H	G	F	E	D	C	B	A	Hi-Z outputs
1 1 1 0	X X X X	H	G	F	E	D	C	B	A	100 kΩ outputs
1 1 1 1	X X X X	H	G	F	E	D	C	B	A	2.5 kΩ outputs

8.5 Programming

8.5.1 Programming the DAC128S085

This section presents the step-by-step instructions for programming the serial input register.

8.5.1.1 Updating DAC Outputs Simultaneously

When the DAC128S085 is first powered on, the DAC is operating in Write Register Mode (WRM). Operating in WRM allows the user to program the registers of multiple DAC channels without causing the DAC outputs to be updated. For example, below are the steps for setting Channel A to a full scale output, Channel B to three-quarters full scale, Channel C to half-scale, Channel D to one-quarter full scale and having all the DAC outputs update simultaneously.

As stated previously, the DAC128S085 powers up in WRM. If the device was previously operating in Write Through Mode (WTM), an extra step to set the DAC into WRM is required. First, the DAC registers must be programmed to the desired values. To set Channel A to an output of full scale, write 0FFF to the control register. This updates the data register for Channel A without updating the output of Channel A. Second, set Channel B to an output of three-quarters full scale by writing 1C00 to the control register. This updates the data register for Channel B. Once again, the output of Channel B and Channel A are not updated, because the DAC is operating in WRM. Third, set Channel C to half scale by writing 2800 to the control register. Fourth, set Channel D to one-quarter full scale by writing 3400 to the control register. Finally, update all four DAC channels simultaneously by writing A00F to the control register. This procedure allows the user to update four channels simultaneously with five steps.

Because Channel A was one of the DACs to be updated, one command step could have been saved by writing to Channel A last. Do this by writing to Channel B, C, and D first, and using the the special command Channel A Write to update the DAC register and output of Channel A. This special command also updates all DAC outputs while updating Channel A. With this sequence of commands, the user can update four channels simultaneously using four steps. A summary of this command can be found in Table 3.

8.5.1.2 Updating DAC Outputs Independently

If the DAC128S085 is currently operating in WRM, change the mode of operation to WTM by writing 9XXX to the control register. Once the DAC is operating in WTM, any DAC channel can be updated in one step. For example, if a design required Channel G to be set to half scale, the user can write 6800 to the control register to update the data register and DAC output of Channel G. Similarly, write 5FFF to the control register to set the output of Channel F to full scale. Channel A is the only channel that has a special command that allows its DAC output to be updated in one command, regardless of the mode of operation. Write BFFF to the control register to set the DAC output of Channel A to full scale in one step.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Using References as Power Supplies

While the simplicity of the DAC128S085 implies ease of use, it is important to recognize that the path from the reference input ($V_{REF1,2}$) to the DAC outputs has a zero Power Supply Rejection Ratio (PSRR). Therefore, the user must provide a noise-free supply voltage to $V_{REF1,2}$. To utilize the full dynamic range of the DAC128S085, the supply pin (V_A) and $V_{REF1,2}$ can be connected together and share the same supply voltage. Because the DAC128S085 consumes very little power, a reference source can be used as the reference input or the supply voltage. The advantages of using a reference source over a voltage regulator are accuracy and stability. Some low-noise regulators can also be used. Listed below are a few reference and power supply options for the DAC128S085.

9.2 Typical Application

The LM4132, with its ±0.05% accuracy over temperature, is a good choice as a reference source for the DAC128S085. The 4.096-V version is useful for a 0-V to 4.095-V output range. Bypassing the LM4132 voltage input pin with a 4.7-µF capacitor and the voltage output pin with a 4.7-µF capacitor improves stability and reduces output noise. The LM4132 comes in a space-saving 5-pin SOT-23.

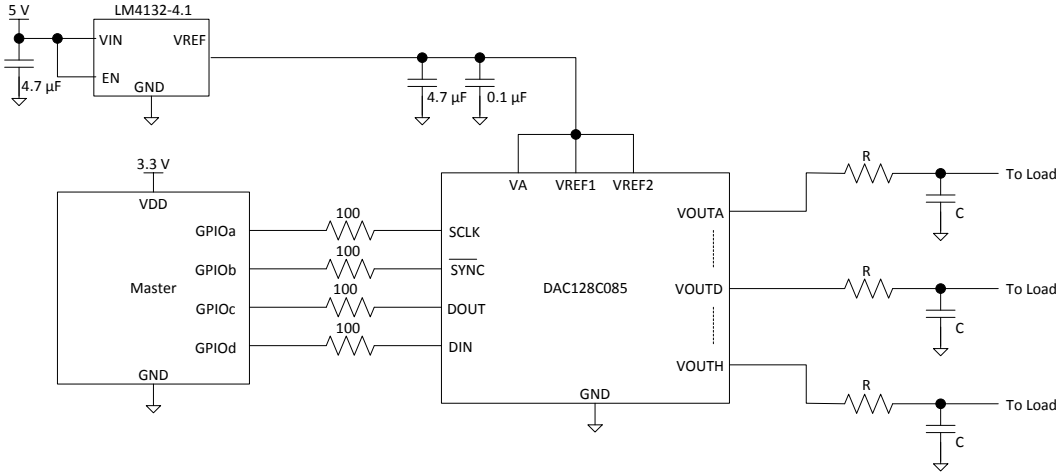

Figure 32. The LM4132 as a Power Supply

9.2.1 Design Requirements

There are two references for the DAC128S085. One reference input serves channels A through D, while the other reference serves channels E through H. The 16-bit input shift register of the DAC128S085 controls the mode of operation, the power-down condition, and the register/output value of the DAC channels. All eight DAC outputs can be updated simultaneously or individually.

9.2.2 Detailed Design Procedure

Each reference input pin can be set independently, or the reference pins can be shorted together as shown in Figure 32. Acceptable reference voltages are 0.5 V to V_A. Utilizing an RC filter on the output to roll off output noise is optional.

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Typical Application (continued)

9.2.3 Application Curve

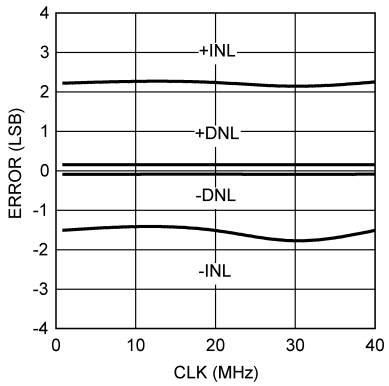

Figure 33. Typical Performance

10 Power Supply Recommendations

For best performance, the DAC128S085 power supply should be bypassed with at least a 1-µF and a 0.1-µF capacitor. The 0.1-µF capacitor must be placed right at the device supply pin. The 1-µF or larger valued capacitor can be a tantalum capacitor, while the 0.1-µF capacitor must be a ceramic capacitor with low ESL and low ESR. If a ceramic capacitor with low ESL and low ESR is used for the 1-µF value and can be placed right at the supply pin, the 0.1-µF capacitor can be eliminated. Capacitors of this nature typically span the same frequency spectrum as the 0.1-µF capacitor, and thus eliminate the need for the extra capacitor. The power supply for the DAC128S085 should only be used for analog circuits.

Avoid the crossover of analog and digital signals. This helps minimize the amount of noise from the transitions of the digital signals from coupling onto the sensitive analog signals, such as the reference pins and the DAC outputs.

11 Layout

11.1 Layout Guidelines

For best accuracy and minimum noise, the printed circuit board containing the DAC128S085 should have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be located in the same board layer. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design will utilize a "fencing" technique to prevent the mixing of analog and digital ground current. Separate ground planes should only be utilized when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the DAC128S085. Ensure that digital signals with fast edge rates do not pass over split ground planes. The signals must always have a continuous return path below their traces.

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11.2 Layout Example

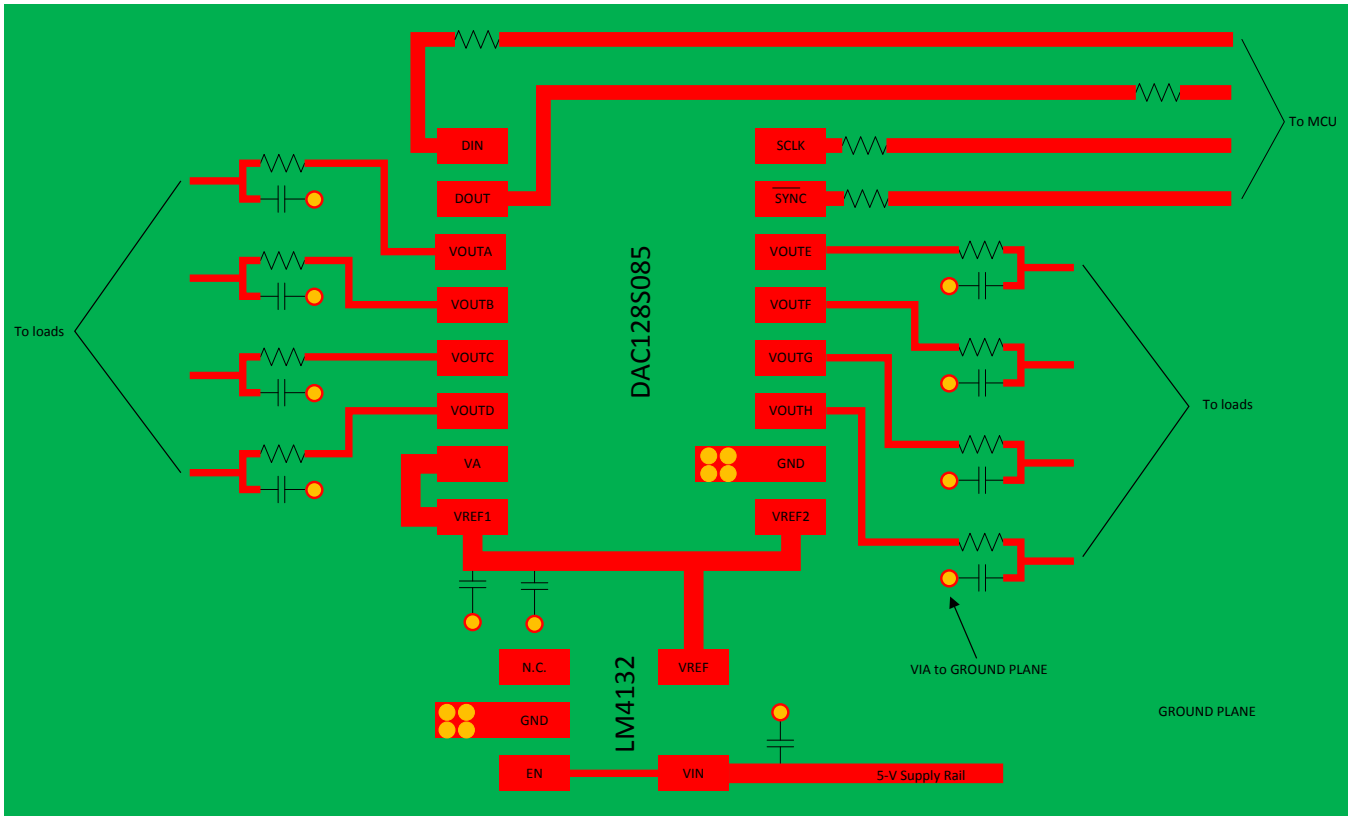

Figure 34. Layout Example

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Specification Definitions

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB, which is V_{REF} / 4096 = V_A / 4096.

DAC-to-DAC CROSSTALK is the glitch impulse transferred to a DAC output in response to a full-scale change in the output of another DAC.

DIGITAL CROSSTALK is the glitch impulse transferred to a DAC output at mid-scale in response to a full-scale change in the input register of another DAC.

DIGITAL FEEDTHROUGH is a measure of the energy injected into the analog output of the DAC from the digital inputs when the DAC outputs are not updated. It is measured with a full-scale code change on the data bus.

FULL-SCALE ERROR is the difference between the actual output voltage with a full scale code (FFFh) loaded into the DAC and the value of V_A x 4095 / 4096.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Zero and Full-Scale Errors as GE = FSE - ZE, where GE is Gain error, FSE is Full-Scale Error and ZE is Zero Error.

GLITCH IMPULSE is the energy injected into the analog output when the input code to the DAC register changes. It is specified as the area of the glitch in nanovolt-seconds.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The end point method is used. INL for this product is specified over a limited range, per the Electrical Tables.

LEAST SIGNIFICANT BIT (LSB) is the bit that has the smallest value or weight of all bits in a word. This value is

$$LSB = V_{REF} / 2^n \quad (3)$$

where

- V_{REF} is the supply voltage for this product, and n is the DAC resolution in bits, which is 12 for the DAC128S085.

MAXIMUM LOAD CAPACITANCE is the maximum capacitance that can be driven by the DAC with output stability maintained.

MONOTONICITY is the condition of being monotonic, where the DAC has an output that never decreases when the input code increases.

MOST SIGNIFICANT BIT (MSB) is the bit that has the largest value or weight of all bits in a word. Its value is 1/2 of V_A.

MULTIPLYING BANDWIDTH is the frequency at which the output amplitude falls 3 dB below the input sine wave on $V_{REF1,2}$ with the DAC code at full-scale.

NOISE SPECTRAL DENSITY is the internally generated random noise. It is measured by loading the DAC to mid-scale and measuring the noise at the output.

POWER EFFICIENCY is the ratio of the output current to the total supply current. The output current comes from the power supply. The difference between the supply and output currents is the power consumed by the device without a load.

SETTLING TIME is the time for the output to settle to within 1/2 LSB of the final value after the input code is updated.

TOTAL HARMONIC DISTORTION PLUS NOISE (THD+N) is the ratio of the harmonics plus the noise present at the output of the DACs to the rms level of an ideal sine wave applied to $V_{REF1,2}$ with the DAC code at mid-scale.

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Device Support (continued)

WAKE-UP TIME is the time for the output to exit power-down mode. This is the time from the rising edge of $\overline{\text{SYNC}}$ to when the output voltage deviates from the power-down voltage of 0 V.

ZERO CODE ERROR is the output error, or voltage, present at the DAC output after a code of 000h has been entered.

12.2 Documentation Support

12.2.1 Related Documentation

- *LM4132 SOT-23 Precision Low Dropout Voltage Reference*, SNVS372

12.3 Trademarks

SPI is a trademark of Motorola, Inc..
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC128S085CIMT/NO.Z	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X78C
DAC128S085CIMT/NOPB	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X78C
DAC128S085CIMTX/NO.Z	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X78C
DAC128S085CIMTX/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X78C
DAC128S085CISQ/NO.Z	Active	Production	WQFN (RGH) | 16	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	128S085
DAC128S085CISQ/NOPB	Active	Production	WQFN (RGH) | 16	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	128S085
DAC128S085CISQX/NO.Z	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	128S085
DAC128S085CISQX/NOPB	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	128S085

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

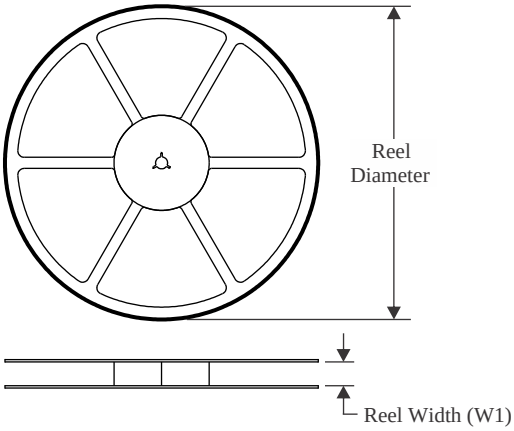
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

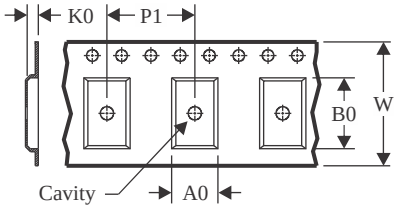
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

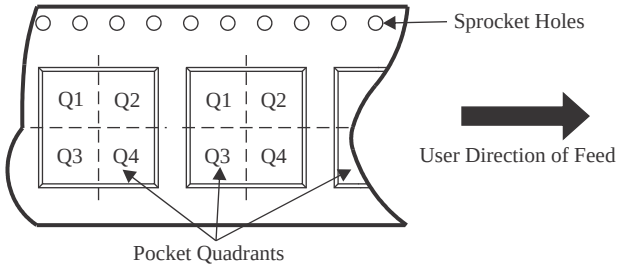


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

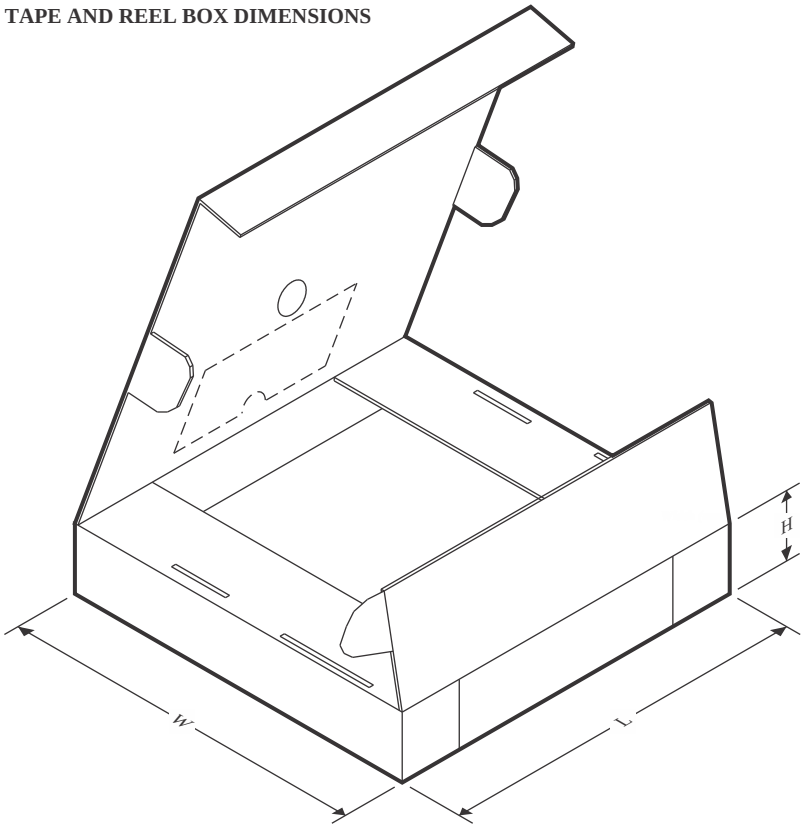
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC128S085CIMTX/ NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
DAC128S085CISQ/NOPB	WQFN	RGH	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DAC128S085CISQX/ NOPB	WQFN	RGH	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

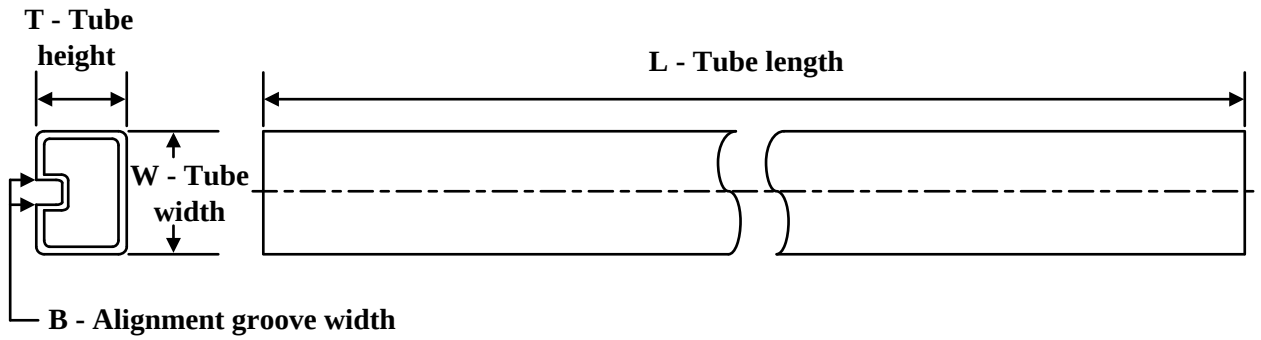
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC128S085CIMTX/ NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
DAC128S085CISQ/NOPB	WQFN	RGH	16	1000	210.0	185.0	35.0
DAC128S085CISQX/ NOPB	WQFN	RGH	16	4500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

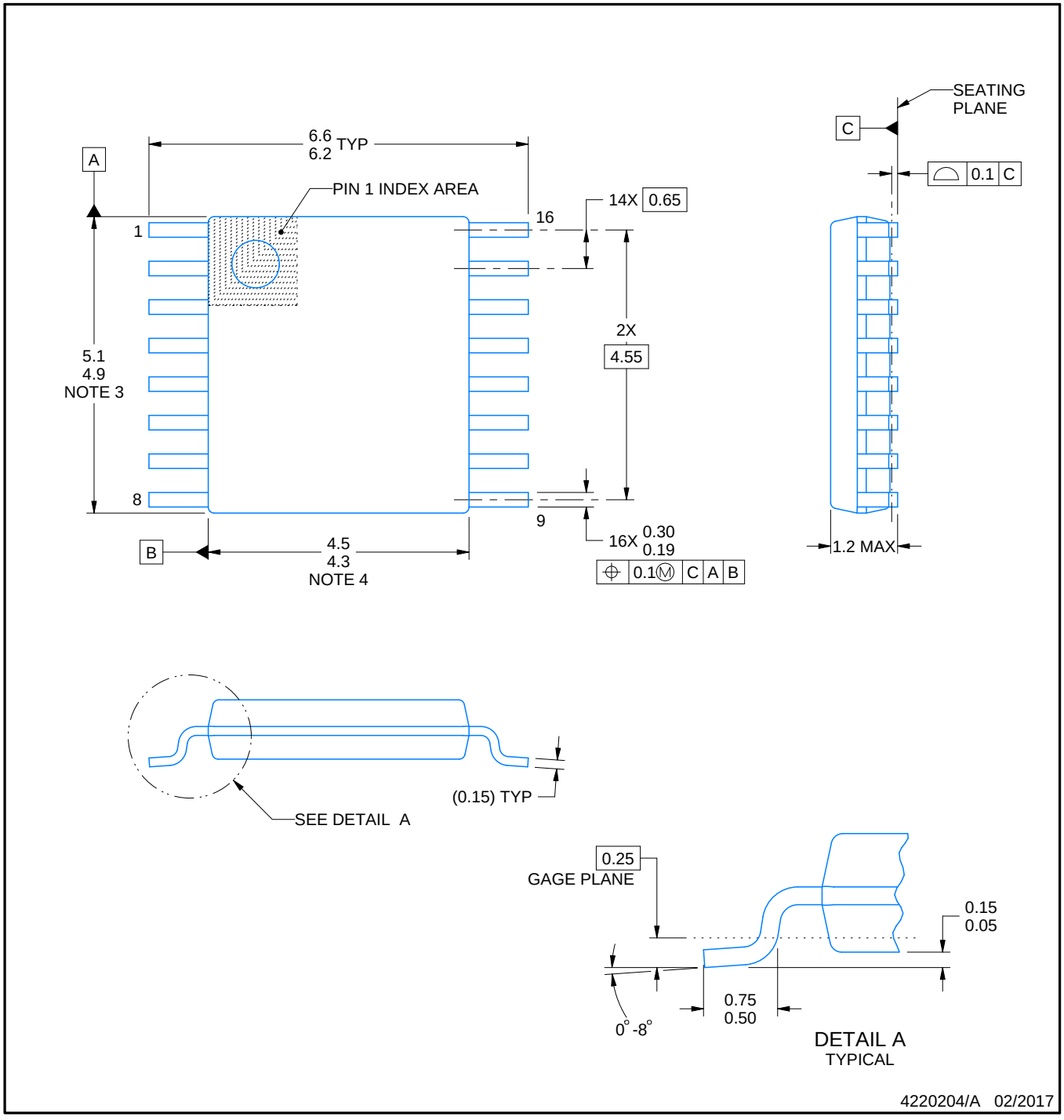
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC128S085CIMT/NO.Z	PW	TSSOP	16	92	495	8	2514.6	4.06
DAC128S085CIMT/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06

PACKAGE OUTLINE

PW0016A

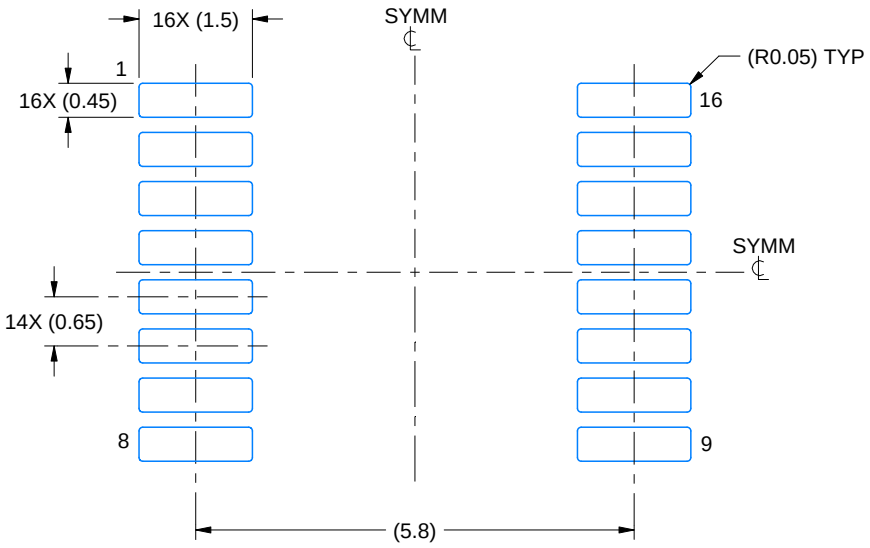
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



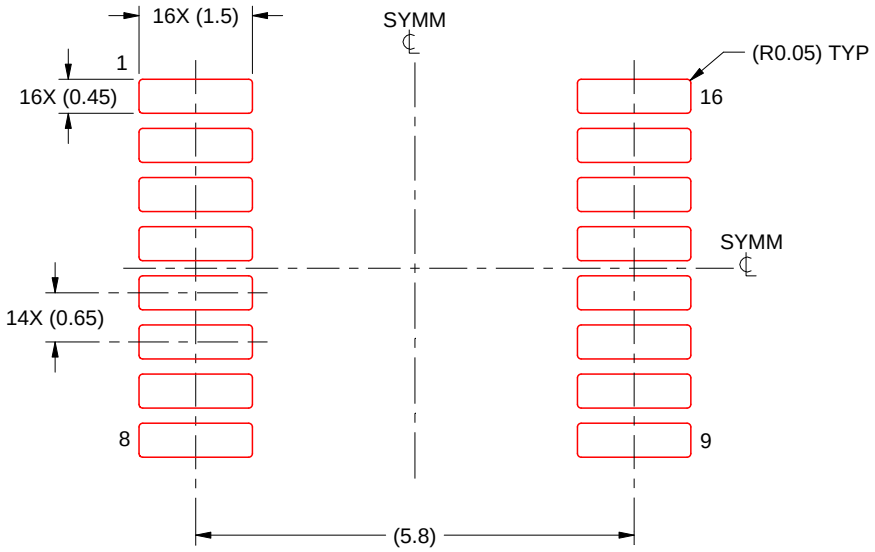
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

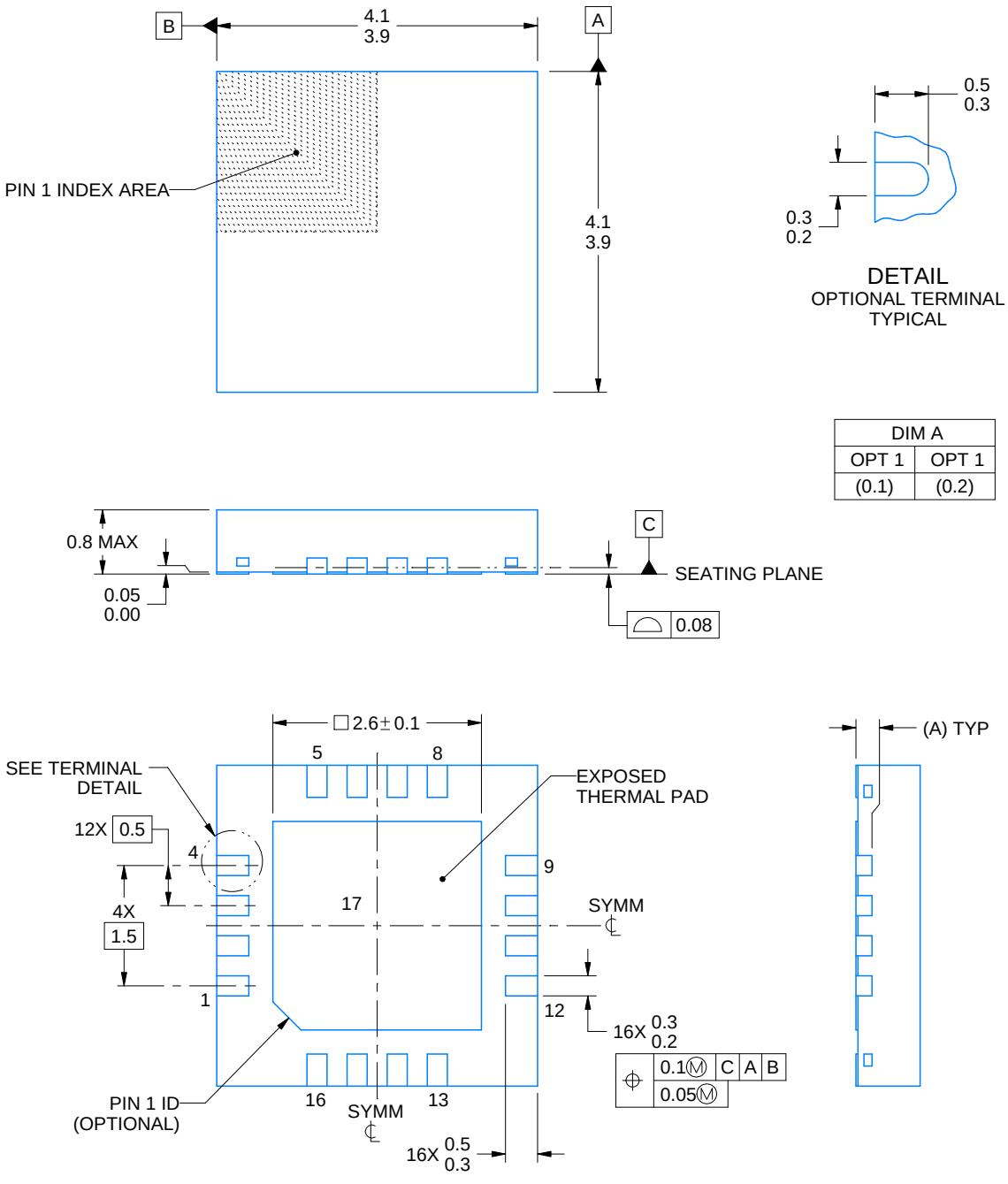
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

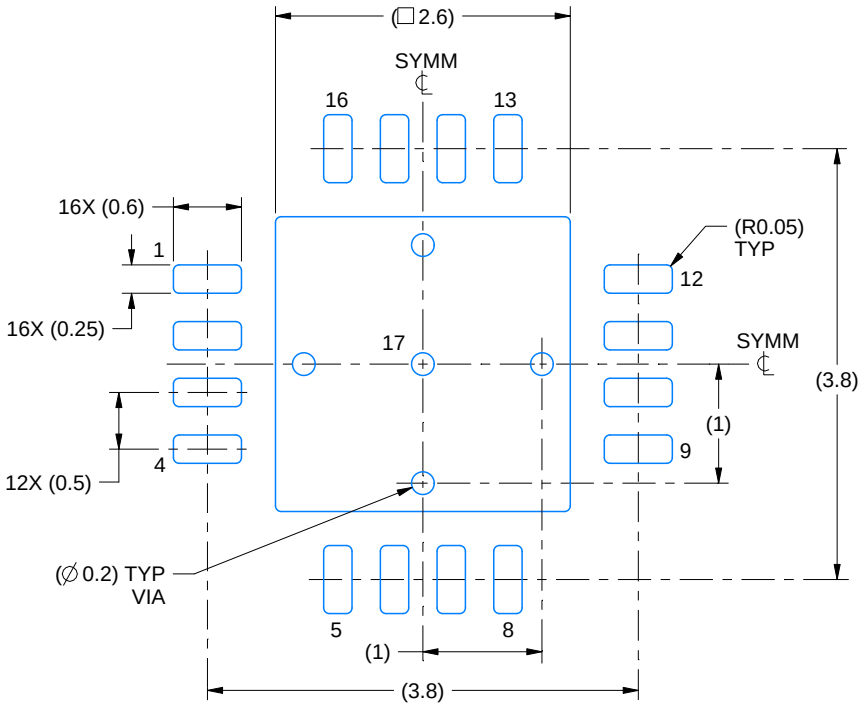
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

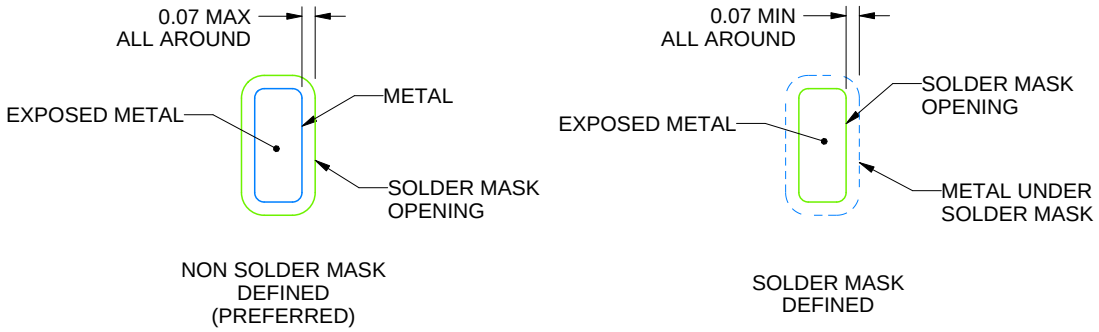
RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

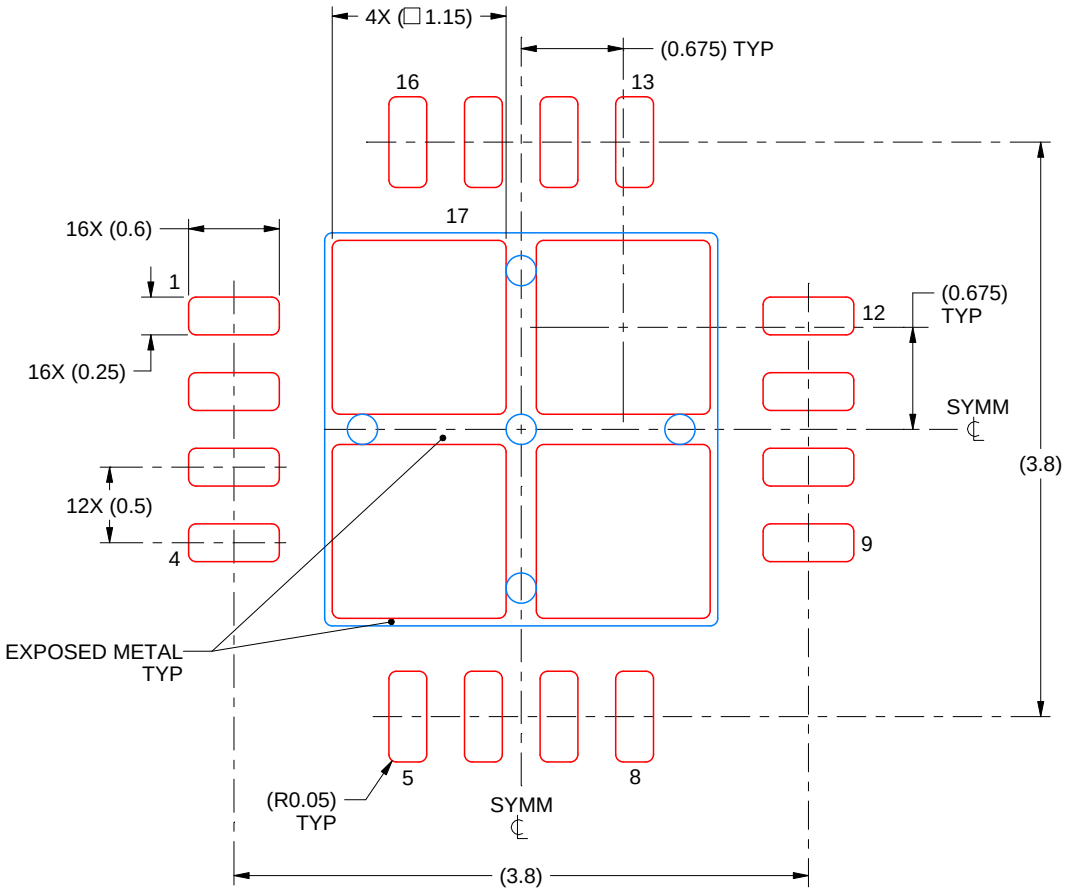


SOLDER MASK DETAILS

4214978/B 01/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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