Application Note

Low Power BAW Oscillators Clocking Industrial 100Mbit Ethernet PHY

Sandra Saba, Raghavendra Reddy *Clocks and Timing Solutions*

ABSTRACT

CDC6C is a low power, single-ended LVCMOS, BAW (Bulk Acoustic Wave) oscillator targeted for the use in Industrial, Automotive and Enterprise applications. The CDC6C is available in a wide range of frequencies including 25MHz, 33.333MHz and 50MHz. This document details the performance advantages of CDC6C compared to quartz oscillators clocking 100Base-Tx devices following test procedure highlighted in University of New Hampshire InterOperability Laboratory (IOL) test suite.

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Trademarks

1 Introduction

The CDC6C is a low power, LVCMOS, BAW oscillator with integrated integer divider to support large frequency output range anywhere from 1MHz to 200MHz. Each frequency is programmed using one-time-programmable memory or OTP for short. CDC6C can also support Vdd input from 1.8V-3.3V using a single supply rail allowing for numerous different configurations using a single IC. For more details on CDC6C capabilities view *CDC6Cx Low Power LVCMOS Output BAW Oscillator*. For the purposes of this evaluation a 25MHz CDC6C is used - CDC6CE025000ADLFR.

This document contains a summary of the test set up and measured results highlighting advantages to the Ethernet PHY's data packet transmission. CDC6C is tested under the specifications highlighted in IEEE 802.3 and IOL's (InterOperability Laboratory) interoperability test bed to determine advantages for 100Base-Tx devices, DP83822 in this case.

2 BAW Overview

2.1 BAW Structure Overview

Bulk Acoustic Wave (BAW) Resonator Technology BAW is a micro-resonator technology that enables the integration of high-precision and ultra-low jitter clocks directly into packages that contain other circuits. In the BAW oscillator, the BAW is integrated with a collocated precision temperature sensor, an ultra-low jitter, low power integer output divider (IOD), a single-ended LVCMOS output driver, and a small power-reset-clock management system consisting of several low noise LDOs.

Figure 2-1 shows the structure of the BAW resonator technology. The structure includes a thin layer of piezoelectric film sandwiched between metal films and other layers that confine the mechanical energy. The BAW uses this piezoelectric transduction to generate a vibration.

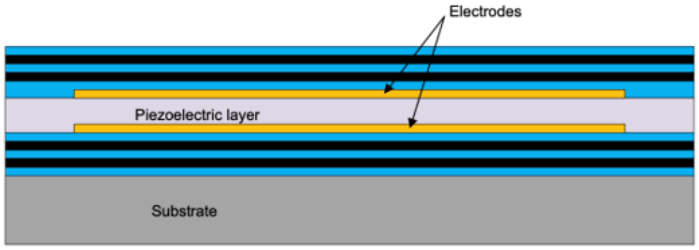

Figure 2-1. Structure of a Bulk Acoustic Wave (BAW) Resonator

2.2 BAW Oscillator Advantages

CDC6C has a number of advantages including frequency flexibility, temperature stability, power supply noise immunity among others. Table 2-1 and Table 2-2 summarize these advantages and showcases how BAW oscillators have solved design limitations found while using quartz oscillators. Additional information can be found in the following application notes:

- *Standalone BAW Oscillators Advantages Over Quartz Oscillators*
- *Vibration and Mechanical Shock Performance of TI's BAW Oscillators*
- *High Reliable BAW Oscillator MTBF and FIT Rate Calculations*

Table 2-1. BAW Resonator versus Quartz Resonator

Parameter	BAW	Quartz	Advantage
Frequency Flexibility	Alleviates supply constraints, single IC supports large range of frequencies through one time programming (OTP).	Output frequency is controlled through mechanical parameters that cannot be modified once cut.	BAW oscillator
Temperature Stability	±10ppm (Maintains temperature stability irrelevant of temperature range)	As temperature increases so does ppm stability	BAW oscillator
Vibration	Typical is 1 ppb/g.Passes MIL_STD_883F Method 2002 Condition A	Can be as high as 10+ppb/g. Typically does not pass MIL-STD.	BAW oscillator
Mechanical Shock	Less than 0.5ppm variation up to 1500 g. Passes MIL_STD_883F Method 2007 Condition B	Typically does not MIL-STD. Can fail at 2,000g	BAW oscillator

Table 2-2. Quartz Limitation Solved by BAW Oscillator

Parameter	BAW Oscillator Design	Quartz Limitation
Power supply noise	Integrated LDO for improved power supply noise rejection (-72dBc PSRR at 500kHz, 50mV ripple)	Typically has no integrated LDO
Mean time between failure	3.3 billion hours of operation	33 million hours of operation
Frequency flexibility	Support any frequency from 1MHz to 200MHz in LVCMOS variant	Limited by resonator crystal; different frequencies require different resonant crystal
Supply chain	Fabricated, assembled and packaged in house by TI	Multiple third party manufacturing to support build of different components (resonator, ASIC, Package, and so on.)
Land pattern	Universal – industry standard footprint	Land pattern can depend on supplier

3 IEEE 100Mbps Requirements

Texas Instruments (TI) follows the specifications mentioned in the technical document titled FAST ETHERNET CONSORTIUM clause 25, Physical Medium Dependent (PMD) Test Suite Version 3.5. This technical document is released by University of New Hampshire InterOperability Laboratory (IOL).

Tests are categorized into two groups which are ACTIVE OUPUT INTERFACE(AOI) TESTS(Group1) and ACTIVE INPUT INTERFACE(AII) Test (Group2). More detailed explanation on each specification can be found in the doc mentioned above.

Table 3-1 provides a summary of the test set up and the tests that are done using the inbuilt Ethernet software available in Tektronix oscilloscope.

Table 3-1. Tektronix TekExpress Ethernet 100BASE-T: Test Set up Description

Test Set Up	Description
Test date	2024-05-03
Device type	Ethernet
TEkExpress Ehternet Version	10.2.1.11
TEkExpress Firmware Version	4.11.0.45
Execution mode	Live
Compliance Mode	True
Overall test result	Pass
Scope Information	MSO70404C, C600447
Scope F/W Version	10.12.1 Build 26
Return loss signal generator	AFG31152
DATA probe Model	P6248
DATA probe serial number	B022354

Table 3-2. Tektronix TekExpress Ethernet 100BASE-T: Test Name Summary Table

Test Name	Evaluation status
AOI template	Pass
Fall time (Pos)	Pass
Fall time (Neg)	Pass
Rise time (Pos)	Pass
Rise time (Neg)	Pass
RF symmetry (Pos)	Pass
RF symmetry (Neg)	Pass
Overshoot (Pos)	Pass
Overshoot (Neg)	Pass
Differential output voltage (Pos)	Pass
Differential output voltage (Neg0	Pass
Amplitude symmetry	Pass
Jitter (Pos)	Pass
Jitter (Neg)	Pass
Duty Cycle Distortion	Pass

3.1 Test Summary on Channel A

Table 3-3 summarizes the specifications for the previous mentioned tests and measured results of channel A from both the CDC6C and quartz oscillators.

Table 3-3. Test Summary Average of 10 Channel A Measurements

Test No.	Test Name	Low Limit	High Limit	CDC6C Average Measured	Quartz Average Measured	Units
1	AOI template	N.A	1	0	0	Hits
2	Fall time (Pos)	3	5	3.96897	4.00266	ns
3	Fall time (Neg)	3	5	3.85165	3.89152	ns
4	Rise time (Pos)	3	5	3.96931	4.01750	ns
5	Rise time (Neg)	3	5	3.85290	4.25979	ns
6	RF symmetry (Pos)	N.A	500.0	140.68743	101.89091	ps
7	RF symmetry (Neg)	N.A	500.0	99.86156	51.00726	ps
8	Overshoot (Pos)	N.A	5.0	1.73302	2.06688	%
9	Overshoot (Neg)	N.A	5.0	1.79440	1.93031	%
10	Differential output voltage (Pos)	0.95	1.05	0.98036	0.98014	V
11	Differential output voltage (Neg0	-1.05	-0.95	- 0.97686	-0.97649	V
12	Amplitude symmetry	0.98	1,02	1.00449	1.00318	
13	Jitter (Pos)	N.A	1.4	0.59000	0.58000	ns
14	Jitter (Neg)	N.A	1.4	0.53200	0.62000	ns
15	Duty Cycle Distortion	N.A	500	251.72400	240.55200	ps

4 CDC6C Clocking DP83822 Evaluation

Jitter and Bit Error Rate (BER) are two important measurements when using Ethernet PHY devices as this affects signal integrity and packet data. The worse the jitter the worse the timing accuracy of data signal. This results in Ethernet packer corruption. The following highlights test procedure, set up and results of both jitter and BER comparing on board quartz oscillator and TI CDC6C BAW based oscillator.

Test conducted using Ethernet PHY, DP83822 EVM, to compare with onboard quartz oscillator and BAW oscillator CDC6CE025000ADLFR. BAW oscillator output is coming from CDC6CEVM connected to Ethernet PHY EVM through jumper cable connected to the clock in pin. See Figure 4-1 illustrating location of jumper pins in red box.

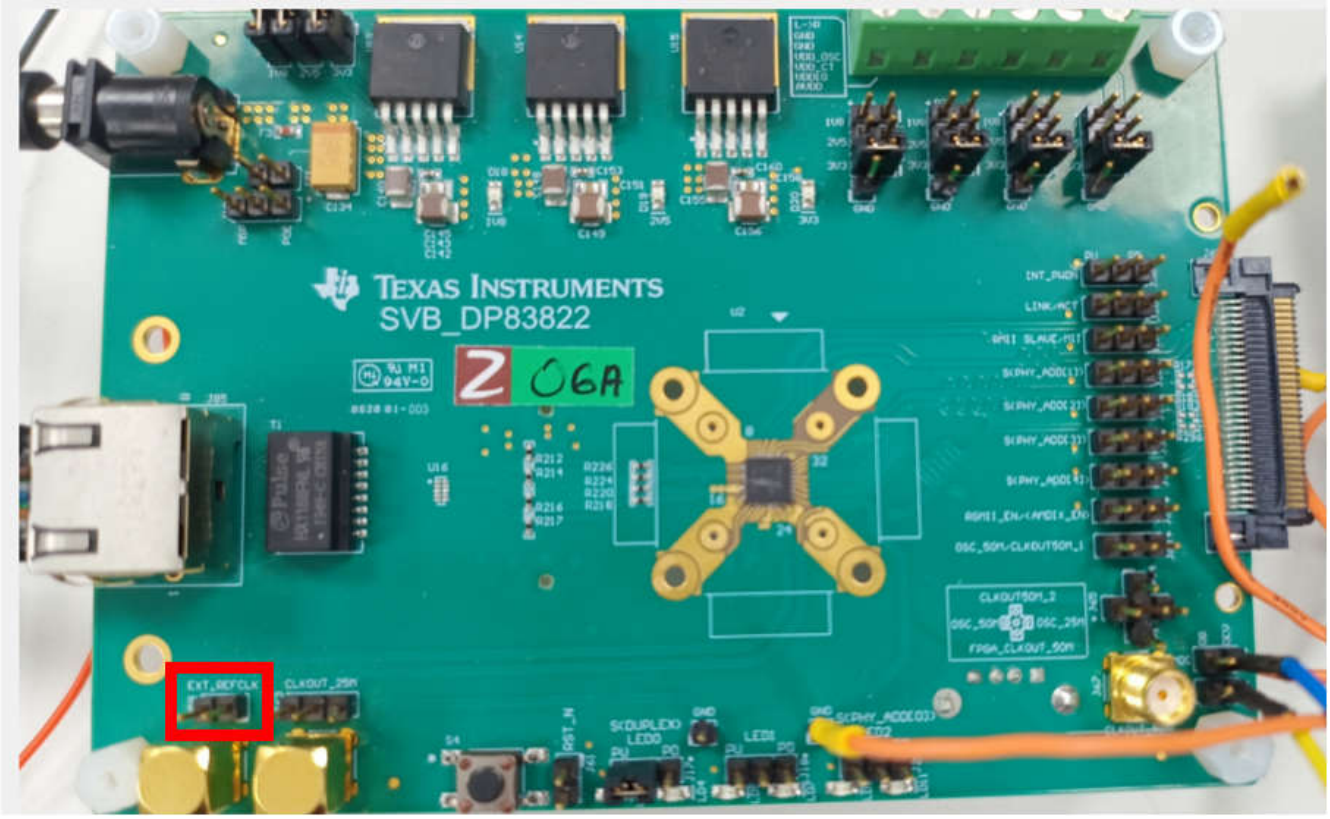

Figure 4-1. DP83822 EVM

To test the oscillators jitter performance the PHY EVM is connected to a test fixture where channels A and B are read. MLT-3 Pattern on MDI CHA (P9) and CHB (P10) is generated in test mode. Figure 4-2 and Figure 4-3 show the jitter test set up and Table 4-1 highlights results of quartz v CDC6C oscillator effect on PHY output.

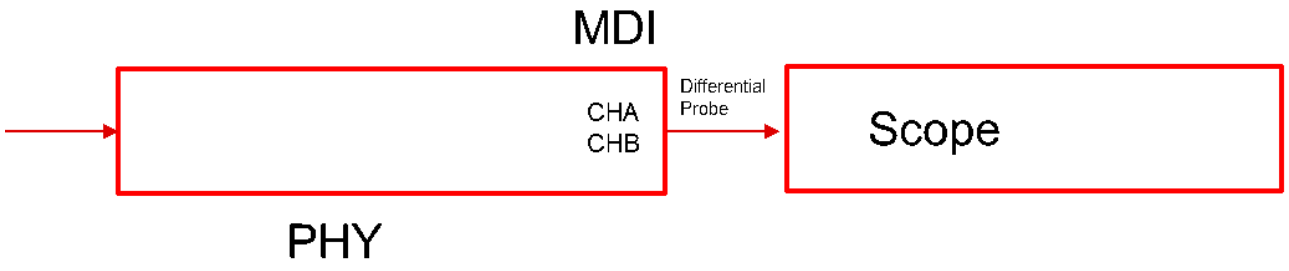

Figure 4-2. Jitter Test Block Diagram

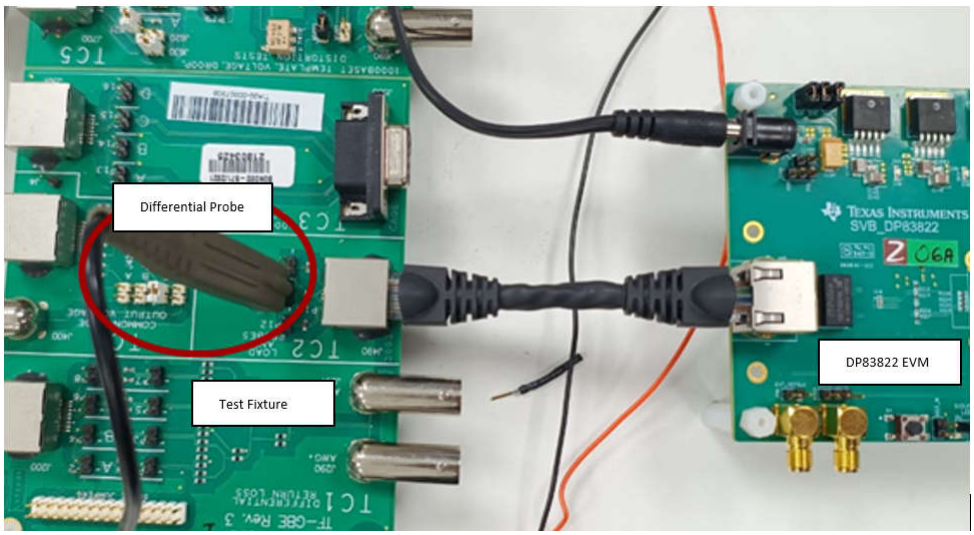

Figure 4-3. Jitter Test Fixture

Table 4-1. Average of 10 Jitter Measurement Iterations of Channels A and B Using Quartz and CDC6C

Parameter	CHA average	CHB average	Units
CDC6C Pos_E	0.56	0.544	ns
CDC6C Neg_E	0.532	0.468	ns
Quartz Pos_E	0.685	0.643	ns
Quartz Neg_E	0.647	0.593	ns

To test oscillator effect on BER the DP83822 PHY EVM is connected to a packet generator with 100m copper interface while looping back the packets into the PHY. BER tested using UNH interoperability test suite. This test maintained the same oscillator set up as jitter test, see Figure 4-4.

Data transmitted and received from the packet generator are random data pattern and random frame size through a continuous packet generation. 113,505,895,589 bytes are transmitted and received with no failures for 1e11 bytes observed as highlighted in Table 4-1 using CDC6C as the reference input clock to DP83822.

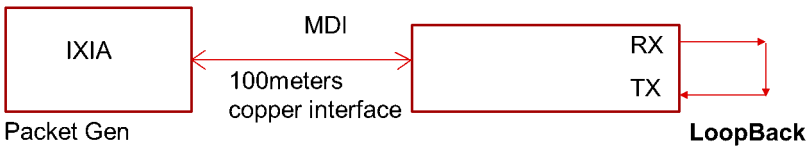

Figure 4-4. Bit Error Rate Test Block Diagram

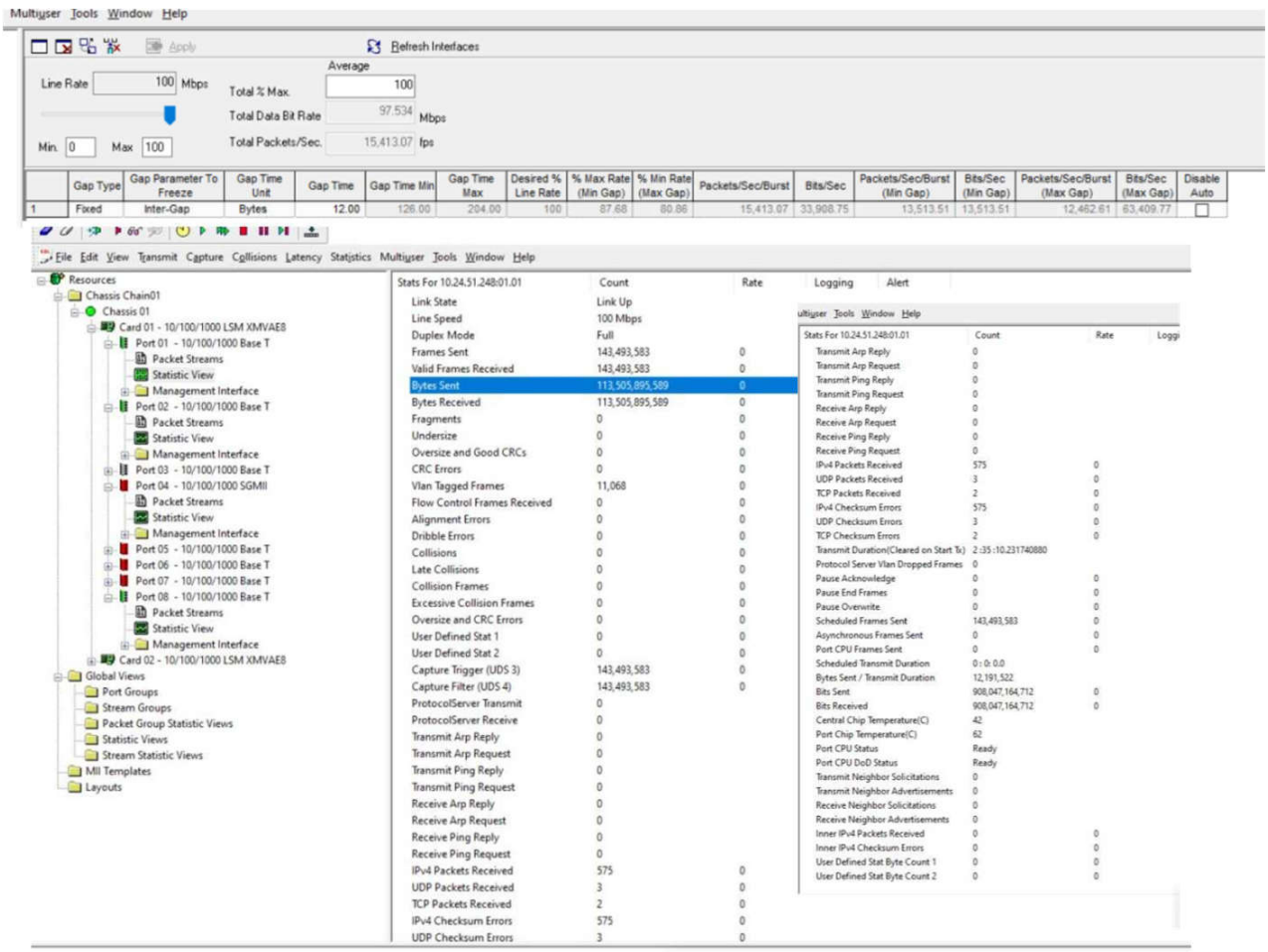

Figure 4-5. BER Test Results of DP83822 Clocked With CDC6C Oscillator

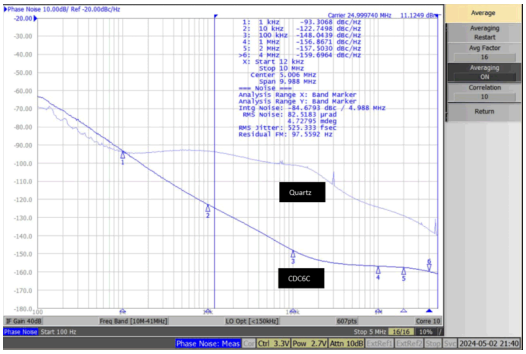

Figure 4-6. Phase Noise and Jitter Measurement Comparing Quartz and BAW Oscillators

5 Clocking for Different Ethernet PHY

Table 5-1. Clocking for Different PHY

Ethernet PHY Part Number	Signaling Differences	Oscillator Recommendation
DP83822	Current mode driver	CDC6C
DP83826	Voltage mode driver	CDC6C

6 Summary

Based on jitter and bit error tests performed, the following are key observations.

- CDC6C passes the IEEE 100Mbps requirements of IEEE 802.3 and IOL's (InterOperability Laboratory) interoperability test bed
- BAW oscillator helps reduce output jitter of both channels A and B which reduces the noise of Ethernet PHY output.
- BAW oscillator help improve PHY performance and in turn improves bit error rate of the Ethernet PHY

7 References

- Texas Instruments, *CDC6Cx Low Power LVCMOS Output BAW Oscillator*
- FAST ETHERNET CONSORTIUM clause 25, Physical Medium Dependent (PMD) Test Suite Version 3.5. University of New Hampshire InterOperability Laboratory (IOL)
- Texas Instruments, *High Reliable BAW Oscillator MTBF and FIT Rate Calculations*, application note.
- Texas Instruments, *Standalone BAW Oscillators Advantages Over Quartz Oscillators*, application note.
- Texas Instruments, *Vibration and Mechanical Shock Performance of TI's BAW Oscillators*, application note.
- Texas Instruments, *DP8382x IEEE 802.3u Compliance and Debug*, application note.
- Texas Instruments, *DP83822 JItter Ananlysis*, application note.

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