Application Brief

Compilation of RF Synthesizer Resources

Narala Reddy

This App Brief documents articles related to TI RF Synthesizers in one place to help customers locate TI RF synthesizers.

This section involves faster locking the PLL loop, configuring the PLL loop, PLLatinum sim setup, factors affecting the PLL true performance, and more.

1. *What to Do When Your PLL Does Not Lock*
2. *Don't Let Bad Reference Signals Destroy the Phase Noise in Your PLL/synthesizer*
3. *Streamline RF Synthesizer VCO Calibration and Optimize PLL Lock Time*
4. *Dramatically Improve Your Lock Time with VCO Instant Calibration* : LMX2820 has the fast lock time compared to all the RF synths available to date, which is covered in this article.
5. *Common Mistakes While Designing With Rf Clock Synthesizers and How To Mitigate the Same*
6. *Active Loop Filters Designs*
7. *High Isolation, Fast Frequency Switching With LMX2820 in Ping-Pong Architecture*

Features and Performance Improvement: This involves extra features that RF synthesizers offer with external components like external PFD option and external VCO mode.

1. *Frequency Shift Keying with LMX2571*
2. *LMX2820 RF Synthesizer Phase Noise Improvement With Alternative Topologies*

Phase Sync:

1. *How to Phase Synchronize Multiple LMX2820 Devices*

Advanced Options: This involves more esoteric features available in RF synthesizers and options to optimize spur magnitudes.

1. *Using a Programmable Input Multiplier to Minimize Integer Boundary Spurs*
2. *How division impacts spurs, phase noise, and phase*
3. *Integer Boundary Spurs*
4. *MASH_SEED Optimization and Impact on Spurs*
5. *High-Frequency Delay Adjustments Between Two RF Synthesizers*
6. *Optimizing loop filter bandwidth for modulated PLL ramping waveforms*
7. *Fractional N Frequency Synthesis*

Miscellaneous: This covers the topics where PLL is used as an input (for example: ADC, DAC) and other factors that can improve PLL performance.

1. *How supply noise impacts clocking devices* : All TI RF synthesizers have internal LDOs for good PSRR. Some cases like external VCO mode are helpful as supply can directly go to external VCOs without internal LDOs.
2. *Sine to Square Wave Conversion Using Clock Buffers* : This article talks about the design for the slow slew rate impact on the degradation of in-band performance of PLL.
3. *Using the MSP430FR5969 EVM to Program the LMX2594 PLL Synthesizer*
4. *High-speed Data Converter Clocking for JESD204B*
5. *Clocking Optimization for RF Sampling Analog-to-Digital Converters*
6. *Impact of PLL Jitter to GSPS ADC's SNR and Performance Optimization*

Trademarks

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265