Application Note

EMI Reduction Strategies With Clocking Devices

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ABSTRACT

Electromagnetic interference (EMI) is any unwanted interference in an electrical circuit caused by an external source. EMI can be categorized as conducted or radiated. Conducted EMI is a form of conduction coupling caused by parasitic impedance, power, and ground connections. Radiated EMI is the coupling of unwanted signals from radio transmission. This application note discusses how to minimize radiated EMI from clocking devices through frequency planning and printed circuit board (PCB) design.

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1 Introduction

When designing a PCB layout for EMI sensitive applications, a good practice is to implement an initial design optimized for best EMI performance. This application note discusses these layout strategies as well as how to fully utilize clocking device features to achieve the best EMI performance.

2 Output Recommendations

2.1 Differential vs. Single-Ended

Clocking waveforms tend to have a very high slew rate. This harsh change in voltage is prone to causing large EMI spikes, both at the output frequency and at subsequent harmonics. 25MHz, for example, is likely to have EMI spurs at 25MHz, 50MHz (2nd harmonic), 75MHz (3rd harmonic), and so on. While generating these outputs, harmonics are unavoidable, therefore choosing the proper output type helps mitigate the power of the spurs.

Using a differential output type, such as LVDS or HCSL, is the best case. Differential signals use both a P and N trace, with each trace being 180 degrees out of phase with the other. When P is HIGH, N is LOW, and vice versa (Figure 2-1). Additionally, differential signals are routed very close together throughout the PCB from the clock generator to the end device. This pattern and short distance serve to efficiently minimize the EMI impact of an individual trace.

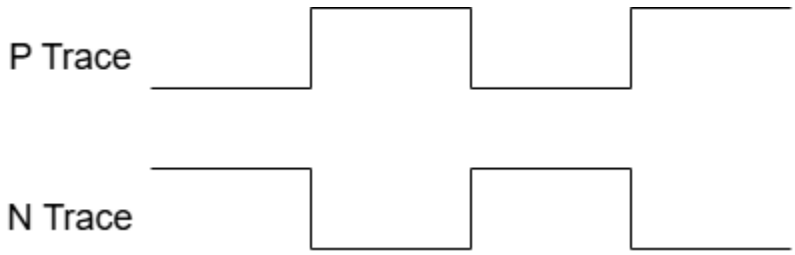

Figure 2-1. P and N Traces

We can apply the same method to single-ended output types, such as CMOS. Single-ended output types do not have the same P and N relation as differential signals do; typically only the P or N trace is utilized. But many clocking devices such as the LMK3C0105 can produce two single-ended signals 180 degrees out of phase with each other from a single output channel block. We can use this to our advantage by trying to mimic differential signals as closely as possible. Routing the traces as a differential pair allows for the best EMI performance. If only one half of the LVCMOS pair is being used, then route both traces and terminate the unused trace as close to the receiver as possible. If the LVCMOS pair is being used for two different receivers, create a frequency plan and PCB layout that allows for the clocking pair to be routed as differentially as possible.

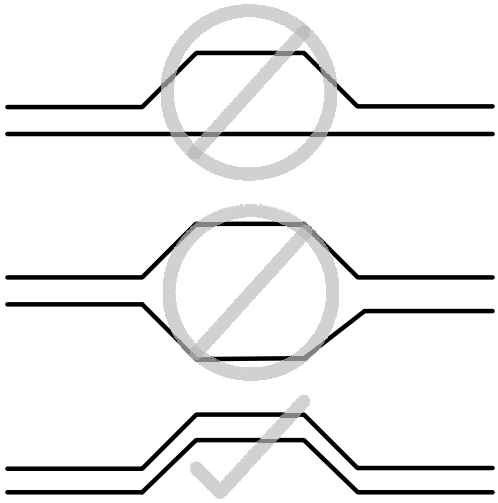

Figure 2-2. Differential Pair Symmetry

When using CMOS, this is also important to consider the trace length. Longer traces for this output type require more power, which in turn creates larger EMI output spurs. This is best to use lower power output types whenever possible, whether differential or single-ended (for example, LVCMOS instead of CMOS or LP-HCSL instead of HCSL).

2.2 Slew Rate

Slew rate refers to the rate of change of the voltage level. Clocking signals are typically square waves, this is common to have a faster slew rate compared to other types of signals. The quick change in voltage level causes a current surge in the circuit, creating an EMI spike. To mitigate this, devices such as the CDC6C have slew rate control (also known as adjustable rise or fall time). Decreasing the slew rate reduces the current surge, resulting is a lower powered EMI spike.

2.3 Spread Spectrum Clocking

Spread Spectrum Clocking (SSC) is the most commonly used tactic to mitigate this source of EMI. SSC is able to reduce the peak amplitude of a digital clock signal by shifting the frequency in a controlled manner, thereby distributing the energy in the frequency domain. This does not, however, affect the amplitude of the clock in the time domain. Center-Spread SSC spreads the energy evenly on either side of the target frequency. Down-Spread SSC only spreads the energy to frequencies below the target. Both versions of SSC can vary in intensity. Figure 2-3 shows the results for 0% (blue), ±0.5% (green), ±1%(cyan) and ±2% (red) center-spread SSC. Clocking devices such as the CDCE6214 and the LMK3H family have SSC capability.

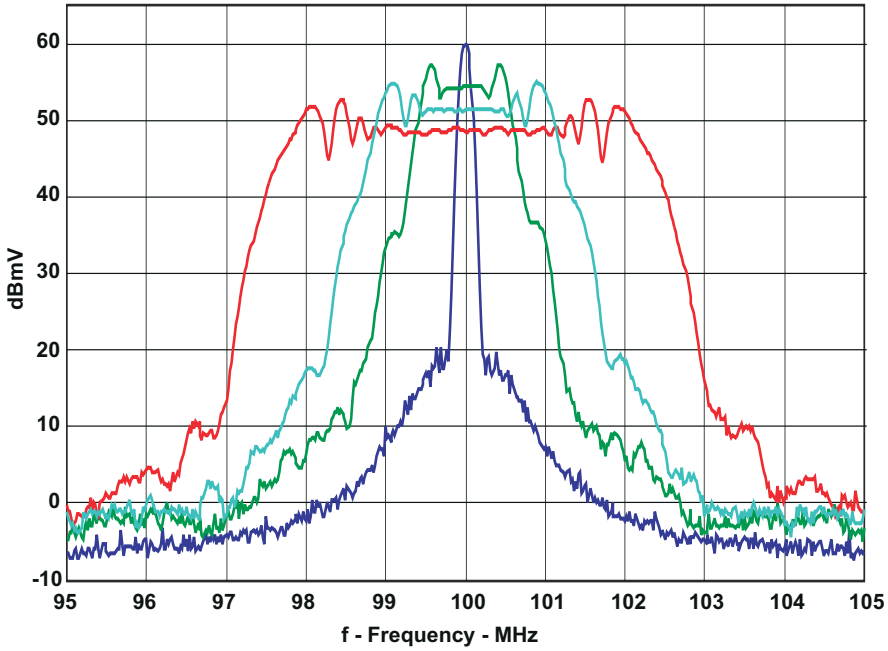

Figure 2-3. 100MHz Output With 0%, ±0.5%, ±1%, and ±2% SSC

More information can be found in the *Spread Spectrum Clocking Using the CDCS502/503*, application note.

3 PCB Design

3.1 Stackup

For maximum EMI mitigation, arrange the PCB stackup to have the clock signal and power traces routed as a stripline (Figure 3-1). Surrounding these high energy sources with ground aids in field containment. Figure 3-2 shows an example of an 8-layer stackup. This example uses Layers 1, 3, and 6 for power and signal traces, surrounding each of those layers with ground planes. While this alone does not fully encompass the traces, this stackup does cover a majority of the surface area, helping to limit radiated EMI.

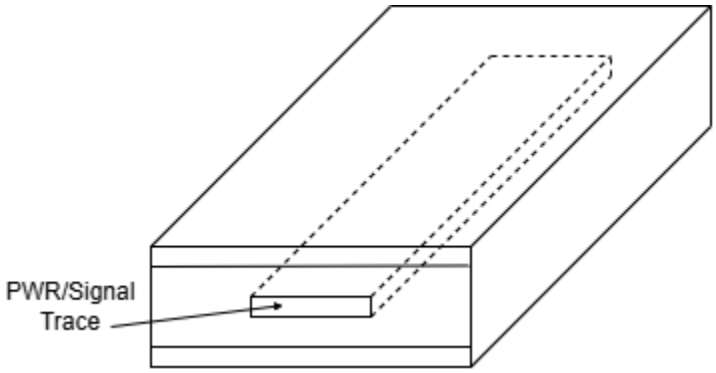

Figure 3-1. Stripline

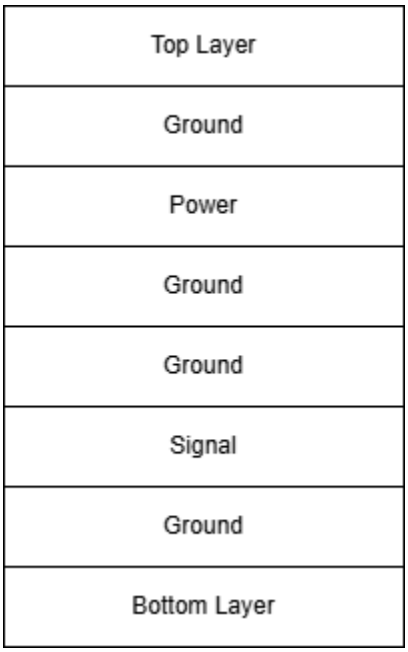

Figure 3-2. 8-Layer PCB Stackup Example

In addition to layer order, it's crucial to consider how the material characteristics impact trace impedance. The trace width and stackup must work to properly impedance match the traces for the output type being used. For example, LVCMOS typically requires 50Ω trace impedance, while LP-HCSL typically uses 85Ω or 100Ω. When the device and signal layer are not impedance matched, this transition can lead to large EMI spurs. Most PCB software and manufacturers have tools that are able to assist in this. If vias are being used to route the clock trace to a different layer, the impedance of the vias must be taken into account as well.

3.2 Power Filtering

A common source of EMI is when frequencies couple into and radiate from the power plane. If seeking CISPR-25 certification, this is especially critical as the antenna measurements are taken from the power cables of the device (Figure 3-3).

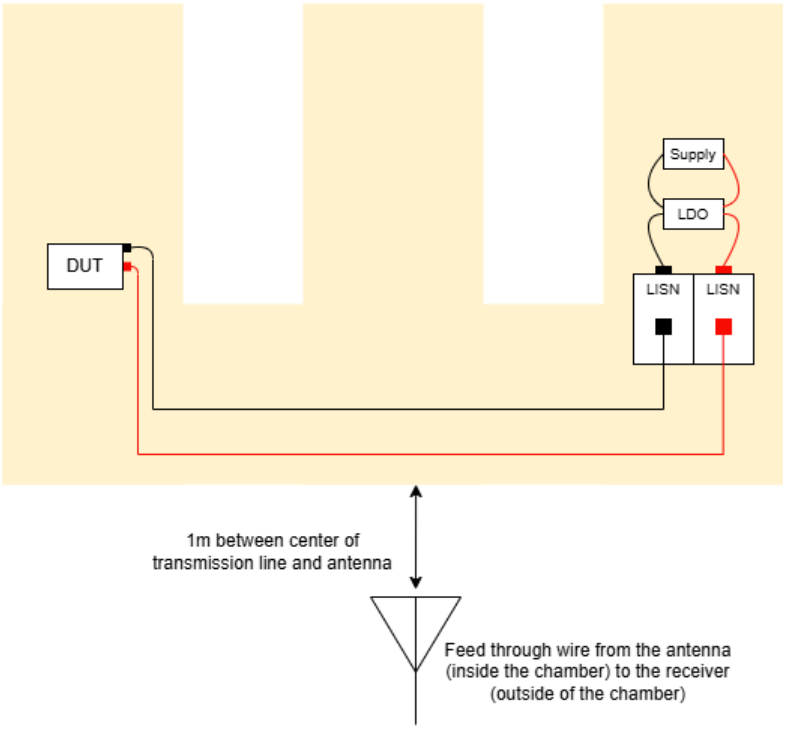

Figure 3-3. CISPR-25 Setup

Using decoupling capacitors is the primary method for creating a clean power in the circuit. Capacitors store energy when connected to a DC power source, so if the voltage fluctuates from the nominal value, the stored energy within the capacitor releases and is delivered to the load. This averages out the overall voltage, keeping the supply steady and reducing EMI spurs.

Common values for decoupling capacitors are 0.1uF and 1uF; however, these values are not capable of filtering out every frequency. Capacitors have finite internal resistance, with both resistive and inductive properties. The frequency at which resonance occurs and where the capacitive reactance and inductive reactance are equal is known as the self-resonance frequency (SRF). This frequency is where the impedance of the capacitor becomes zero. We require our decoupling capacitor to have the lowest impedance possible at the frequency we want to filter on our power supplies.

In the case of clocking, the CDC6C has a variety of rise time options. Automotive applications usually use clocks with much slower rise times due to the advantage of EMI effects being mitigated. The CDC6 Slow Mode 4 has a typical rise time of 2.7ns. This 2.7ns rise time can correspond to EMI spurs at 370MHz and the subsequent harmonics. In this case, a decoupling capacitor with an SRF of 370MHz can reduce the switching noise impact on the power and effectively discharge when the load current spikes.

Wurth Elektronik provides an *EMI Filter Designer tool* that can help choose the appropriate capacitor and ferrite bead values to target a specific frequency.

3.3 Avoid Bottlenecking

As stated in the prior section, the power and ground planes can be a powerful source of EMI radiation. A common mistake in PCB design is creating *bottlenecks* in the power and ground traces. *Bottlenecking* occurs when a large concentration of power is forced into a smaller area.

In the following images, the red colored arrows represent a higher concentration of power, while the green colored arrows represent a lower concentration.

In Figure 3-4, the VDD trace shifts to a narrower trace. Where the two connect is the *bottleneck*. That area is heavily concentrated with current and can act as an antenna for EMI, shown with the red colored arrows.

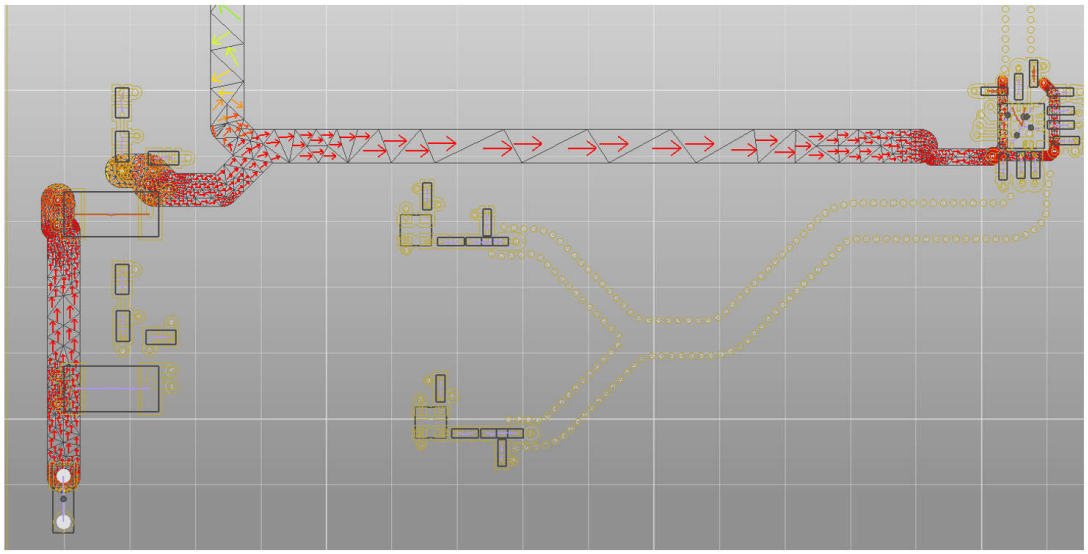

Figure 3-4. Narrow Power Trace

In the new layout (Figure 3-5), the entire plane is utilized, rather than a single trace, decreasing the power concentration at any given point, shown by the green arrows.

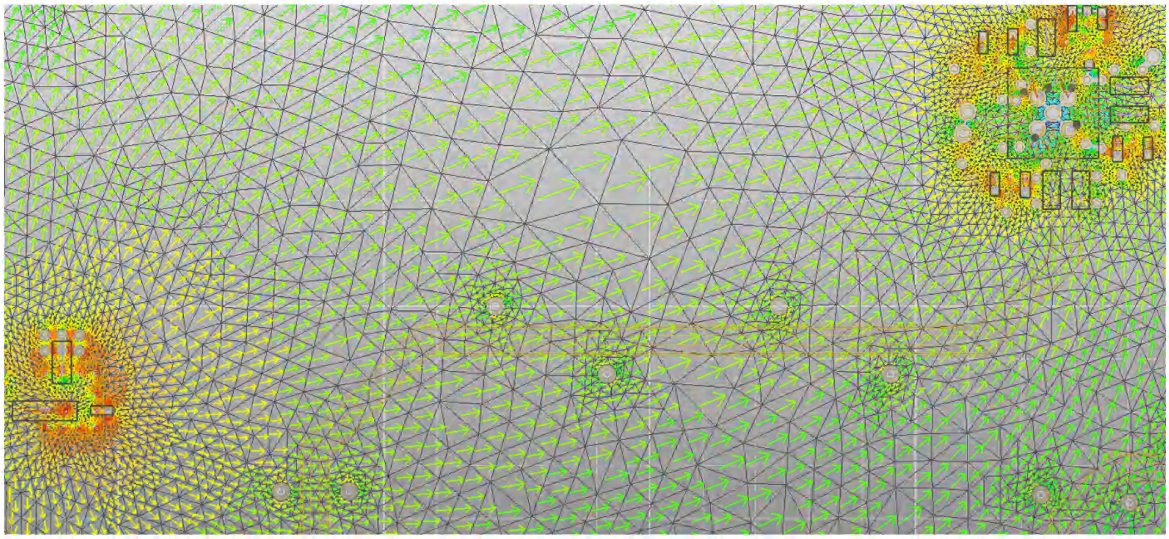

Figure 3-5. Wider Power Trace

3.4 Strategic Via Placements

3.4.1 Distributing Power Concentrations

Any large concentration of power is likely to cause an EMI spur. While the Section 3.3 section discusses this with trace width, high power concentrations can be found in other areas in the PCB. Vias and passive components tend to have these higher concentrations at connection points. If the via is significantly smaller than the trace width, for example, this transition can act as an antenna. Similarly, a large passive component pad connecting to a smaller trace width or a transition between two planes can have the same effect.

3.4.1.1 Via Sizes

Running a trace through a via causes a disruption in the current flow, which is likely to cause an EMI spike. However, having vias significantly larger than the trace width creates an even harsher transition (Figure 3-6). This harsher transition can act as an antenna, creating larger EMI spurs. When running a trace through a via, have the trace width be slightly larger than the via (Figure 3-7).

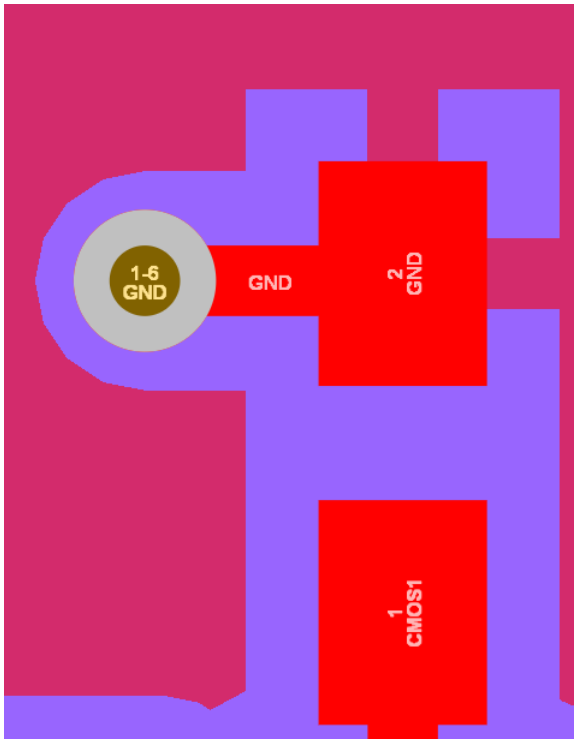

Figure 3-6. Passive with Narrow Trace to Ground Via

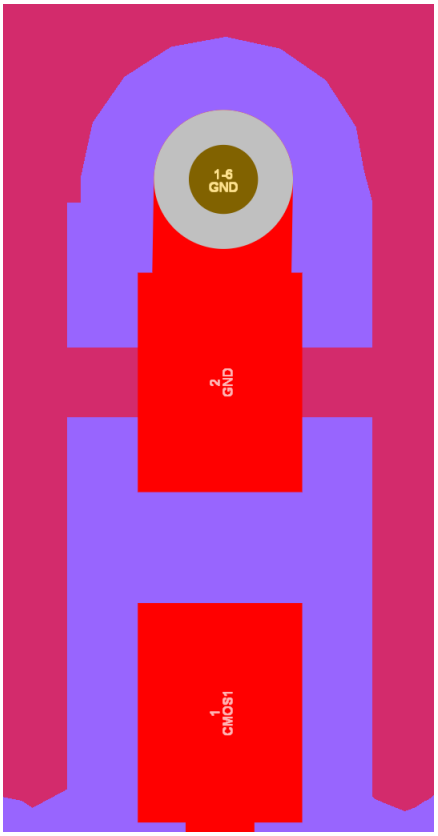

Figure 3-7. Passive with Wider Trace to Ground Via

3.4.1.2 Pads and Pours

A large passive component pad connecting to a smaller trace width can also be a source of EMI spikes (Figure 3-8). When connecting the passives, have the trace width match the pad size. Similarly, when connecting a net between two planes, use several vias to distribute the energy more evenly (Figure 3-9). This is especially crucial for power and ground nets.

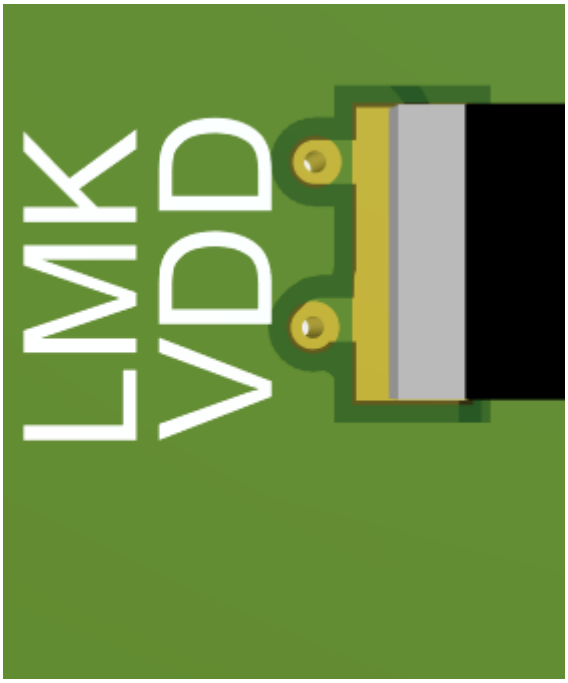

Figure 3-8. Large Passive with Few Vias

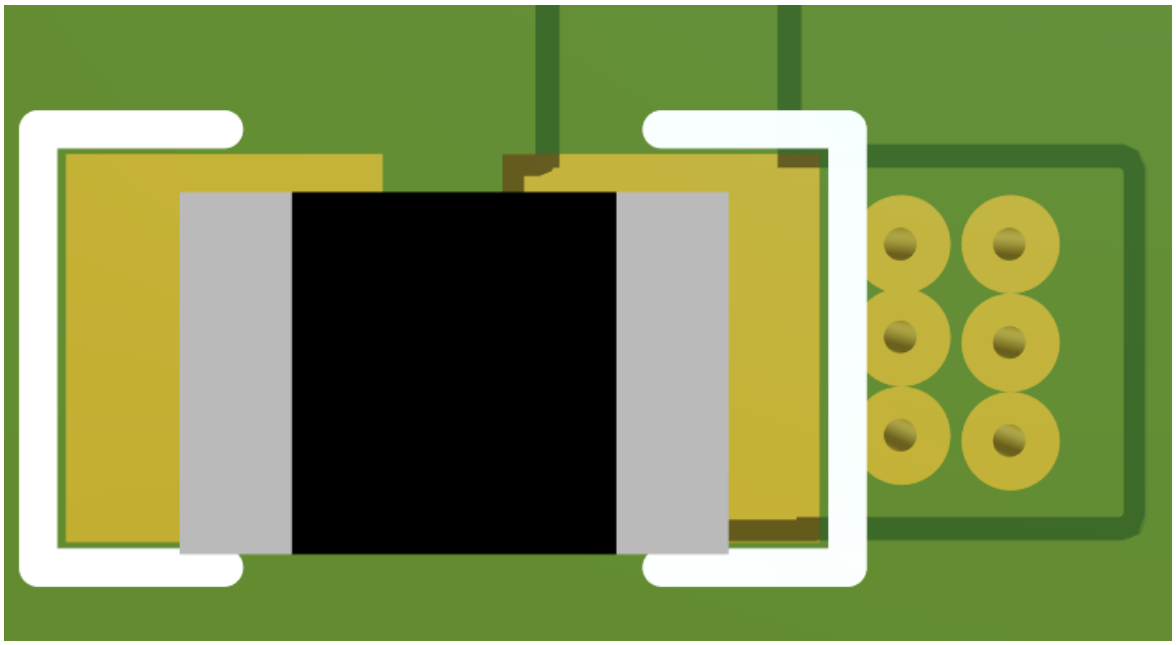

Figure 3-9. Large Passive with Many Vias

3.4.2 Shielding and Stitching Vias

A common method for EMI mitigation in PCB design is the use of through-hole stitching and shielding vias. Stitching refers to using a general pattern of ground vias scattered across the entire board. Spacing between each via can vary based on the needs of the design. These vias connect, or *staple*, the ground planes of the PCB together, creating an overall strong ground for the circuit. The additional grounds also serve to further surround the power plane or traces, aiding in field containment (Figure 3-10). Having a strong ground in the circuit is one of the **most** effective ways of reducing EMI.

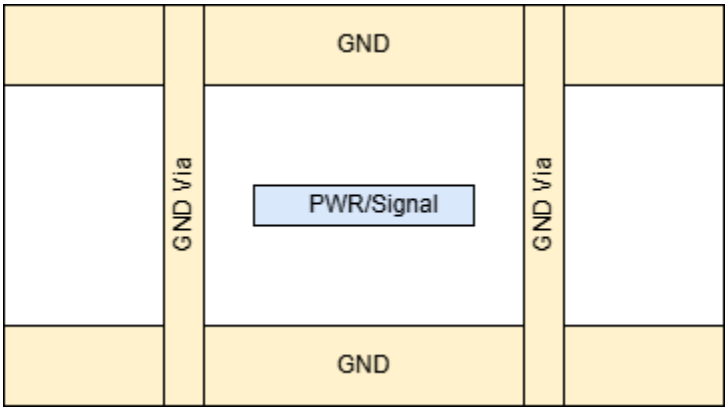

Figure 3-10. Stripline Stackup with Vias

The best practice is to place an additional ground via at connection points (Figure 3-11). Connection points are anywhere a trace is connecting to another element, such as a via or passive. The extra via allows for a shorter path to ground, reducing inductance and EMI.

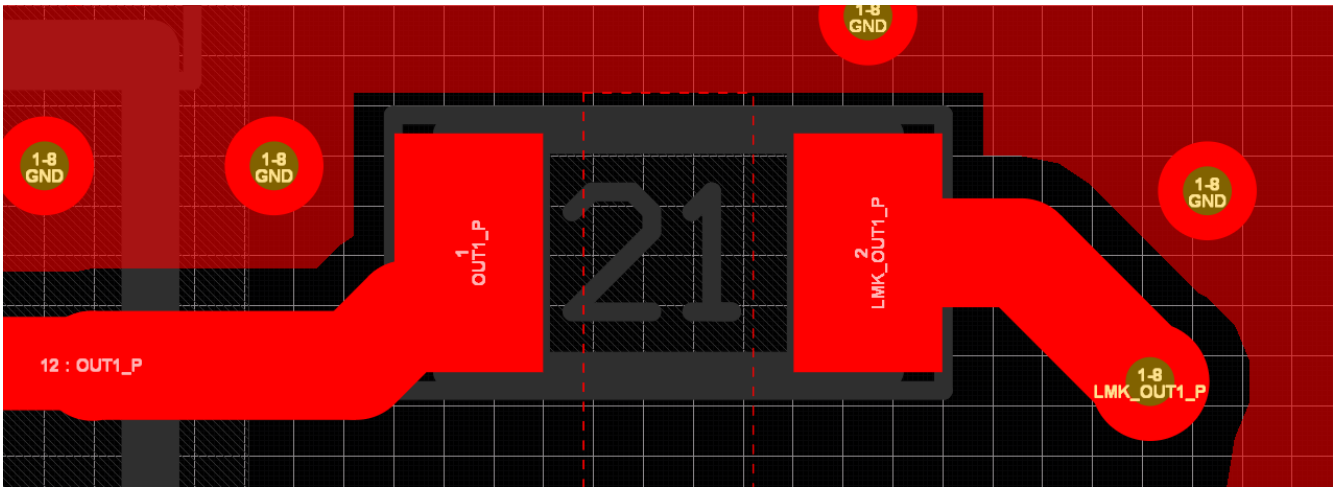

Figure 3-11. Resistor with Ground Vias near Trace Connection Points

Shielding, like stitching, also utilizes ground vias. However, instead of being scattered throughout the entirety of the board, shielding vias are placed alongside the signal traces (Figure 3-12). These vias are able to assist in filtering out certain frequencies. Space the array of vias 1/20th of the wavelength for lower clocking frequencies or 1/10th of the wavelength for higher frequencies. While this method prioritizes striplining specific traces, using through-hole vias can have a similar effect to using stitching vias, strengthening the overall ground and striplining parts of the power plane.

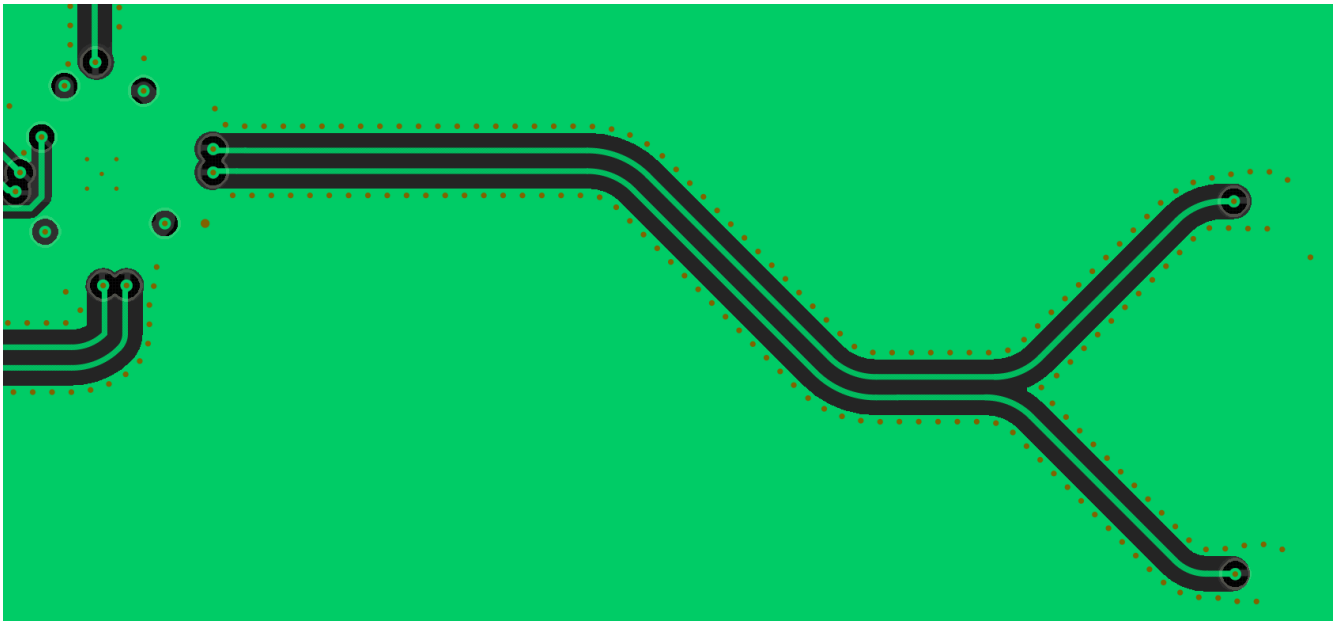

Figure 3-12. Clock Traces with Shielding Vias

4 Minimize Possible Antennas

4.1 Stubs

Any stub in the circuit can become an antenna, and those on the surface of the PCB do not have the additional GND layer on top for field containment. Component pads, especially DNP ones, are a regularly found example of a stub. This is best to have a ground pour across the top layer surrounding the components and have a ground plane as a second layer to reduce the effects.

4.2 Net Pours

When creating a ground pour across the top layer of a PCB, the automated software can sometimes form ground *fingers* in between components (Figure 4-1). These *fingers* can be removed by cutting the ground pour (Figure 4-2).

Figure 4-1. Ground Finger

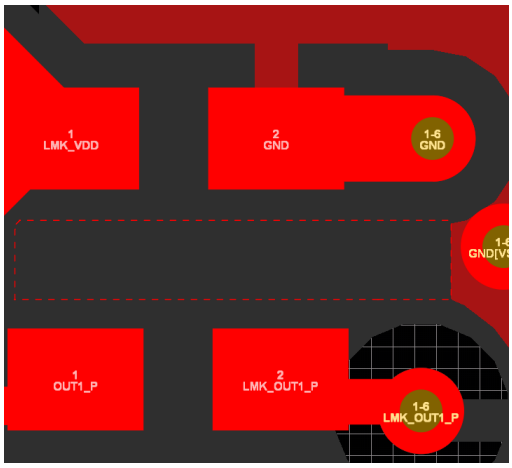

Figure 4-2. Ground Finger Removed

Similarly, check net pours for smooth borders. Any *snags* in the pour can lead to the current flow getting *stuck* and radiating (Figure 4-3).

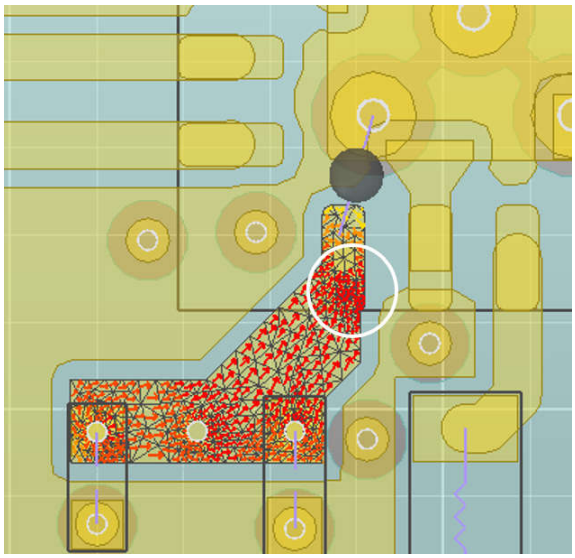

Figure 4-3. Power Pour with Snag

5 Summary

PCB layout is one of the main contributors to EMI performance of a system. When designing a board, this is crucial to maintain a clean power supply (via capacitors and ferrite beads) and a strong ground (via additional ground vias). The PCB layer stackup and trace layout can also be optimized for additional ground shielding and smooth power flow.

When using clocking devices, different settings, such as SSC, can be used to reduce EMI emissions further.

6 References

- Texas Instruments, *PCB Design for Reduced EMI*, application note
- Texas Instruments, *High-Speed Layout Guidelines for Reducing EMI for LVDS SerDes Designs*, application note.
- Texas Instruments, *Spread Spectrum Clocking Using the CDCS502/503*, application note.
- Texas Instruments, *Time-Saving and Cost-Effective Innovations for EMI Reduction in Power Supplies*, marketing white paper.
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- Texas Instruments, *CDC6Cx Low Power LVCMOS Output BAW Oscillator*, data sheet.
- Altium, *Designing a 6-Layer PCB Stackup for Enhanced EMC*, PCB design.
- Würth Elektronik, *EMI Filter Designer*.

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