Application Note

Impact of PLL Jitter to GSPS ADC's SNR and Performance Optimization

ABSTRACT

Jitter noise contributed by the clock source (frequency synthesizer or phase-locked loop (PLL)) has a big impact on the performance of new generation high-performance Gsps analog-to-digital converters (ADC).

Both in-band and out of-band noise performance of the PLL impact the ADC signal-to-noise ratio (SNR), and consequently the effective resolution of the ADC (ENOB). The noise contributed by the PLL can be reduced by operating the PLL Phase Frequency Detector (PFD) at higher frequencies, reducing the input -output multiplication factor N, and using a bandpass filter to reduce far-out noise (or noise floor). This application note describes how to estimate the jitter requirements, translate that into a PLL phase noise requirement, and determine (recommending) the filter bandwidth needed to minimize the SNR performance degradation due to the clocking source. While this analysis is generic and applies to any PLL and ADC, a specific example will be provided by using TI LMX2594 high performance PLL and ADC12DJ5200 12-bit, 5-GSPS ADC.

Table of Contents

List of Figures

List of Tables

Trademarks

1 PLL Phase Noise and RMS Jitter

The generation of accurate waveforms plays a crucial role in almost all electronic equipment, from radar to consumer electronics. A frequency synthesizer, or Phase-Locked Loop (PLL), is defined as a system that generates one or many frequencies from a very accurate and stable reference, in such a way that the ratio of the output to the reference frequency is an integer (integer-N PLL) or fractional number (fractional-N PLL).

$$F_{OUT} = (N \times F) \tag{1}$$

where

- F_{OUT} is the output frequency
- F_{REF} is the reference frequency
- N is either an integer or fractional number

For more information on PLL and frequency synthesis, refer to [1], [2], [3]. The ideal output of a sinewave generator is given by Equation 2:

$$A \sin(\omega_o t + \varphi) \tag{2}$$

The corresponding spectrum is a delta (Dirac) function at frequency Fo = ωo / 2π. In the real world, the generated signal will be:

$$A\left[1 + n_a(t)\right] \sin\left[\omega_o t + \varphi + n_\varphi(t)\right] \tag{3}$$

where

- $n_a(t)$ is the amplitude noise, which in most cases is negligible
- $n_\phi(t)$ is the phase noise

The corresponding spectrum will exhibit a skirt around the carrier frequency, as depicted in Figure 1-1.

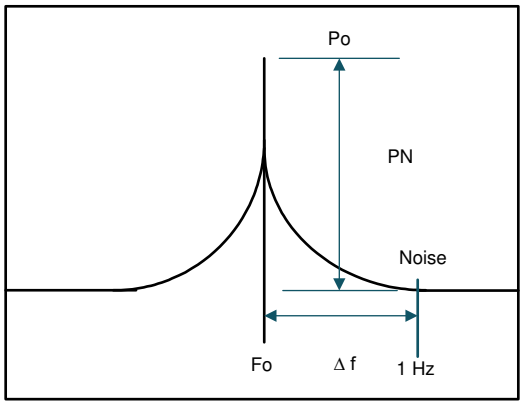

Figure 1-1. Ideal and Real Output Spectrum for a Sinusoidal Signal

To quantify phase noise, consider a unit bandwidth (1 Hz) at an offset Δf with respect to F_O, calculate the noise power in this bandwidth and divide the result by the carrier power:

$$PN(\Delta f) = \frac{N_{1Hz}(\Delta f)}{P_o}\left[\frac{rad^2}{Hz}\right] \tag{4}$$

where

- PN(Δf) is the single sideband (SSB) phase noise at offset frequency Δf

In dB:

$$PN_{dB}(\Delta f) = 10\log\left(\frac{N_{1Hz}(\Delta f)}{P_o}\right)\left[\frac{dBc}{Hz}\right] \quad (5)$$

Figure 1-2 shows a typical PLL phase noise plot.

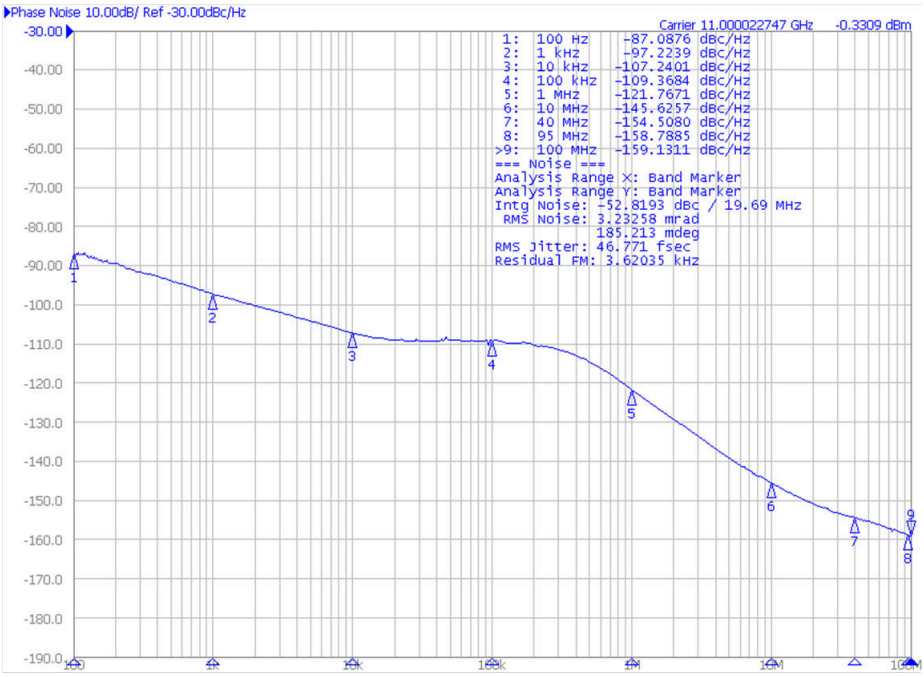

Figure 1-2. Typical PLL Phase Noise Plot (LMX2594 Phase Noise at 11 GHz)

Depending on the specific application, phase noise can be specified as a mask, in which case phase noise target values at given offset frequencies are provided, or as integrated RMS noise, over a given integration bandwidth:

$$PN_{rms} = \int_{f\min}^{f\max} PN(f)\,df\left[rad^2\right] \quad (6)$$

where

- fmin and fmax are the lower and higher integration limits, respectively

In dB:

$$PN_{db} = 10\log(PN_{rms})[dBc] \quad (7)$$

Phase jitter can be calculated from the integrated RMS noise as:

$$\varnothing_{rms} = \sqrt{2PN_{rms}}\,[rad] \quad (8)$$

Equation 9 shows the phase jitter in degrees.

$$\varnothing_{deg} = \frac{180}{\pi}\varnothing_{rms} \tag{9}$$

where

- The factor 2 takes into account that phase noise is defined as SSB and noise is actually present on both sides of the carries (dual sideband (DSB) noise).

Time jitter can be calculated from phase jitter as:

$$T_j = \frac{\varnothing_{rms}}{2\pi F_o}[s] \tag{10}$$

Time jitter is typically specified for clocking application, where accurate sample time is required, and can be interpreted as the spread around the zero crossing of the clock signal, as depicted in Figure 1-3.

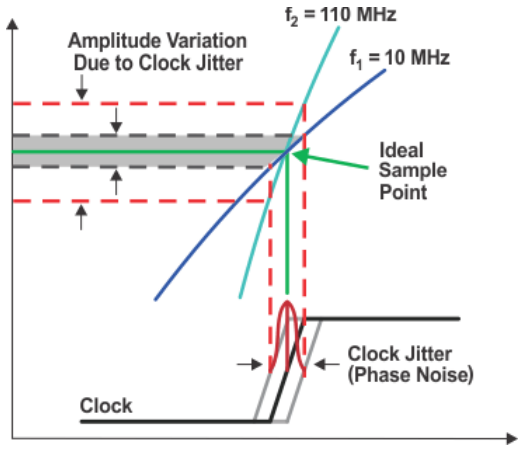

Figure 1-3. Jitter in the Time Domain

2 ADC SNR and Jitter Impact

This section discusses the effect of the clock generator phase noise and jitter on the performance of the data converter, focusing on analog-to-digital converter (ADC) and signal-to-noise ratio (SNR) as an indicator of the ADC dynamic range and linearity. The sampling clock jitter (Tj) is the combination of the jitter contributed by the clock source (T_{jclk}) and the internal ADC aperture jitter (T_{japt}):

$$T_j = \sqrt{\left(T_{japt}\right)^2 + \left(T_{jclk}\right)^2}[s] \tag{11}$$

The ADC SNR degradation due to jitter (total) can be calculated as:

$$SNR_{jitter}(f) = -20\log\left(2\pi f T_j\right)[dBc] \tag{12}$$

If SNRADC is called the contribution to the ADC SNR due to quantization and thermal noise, noting that ADC parameters are usually expressed in dB from full scale (dBFs) to account for input signal level, then the total SNR can be calculated as:

$$SNR(f) = -20\log\left(\sqrt{\left(10^{\frac{BO - SNR_{jitter}}{20}}\right)^2 + \left(10^{\frac{-SNR_{ADC}}{20}}\right)^2}\right)[dBFs] \tag{13}$$

where

- BO is the input signal level back off from ADC full scale

If the harmonic distortion (THD) is included, also expressed in dBFs, define the ADC signal-to-noise and distortion (SINAD) as:

$$SINAD(f) = -20\log\left(\sqrt{\left(10^{\frac{-SNR(f)}{20}}\right)^2 + \left(10^{\frac{-THD}{20}}\right)^2}\right)[dBFs] \quad (14)$$

Finally, calculate the effective number of bits of the ADC (ENOB) as:

$$ENOB(f) = \frac{SINAD(f) - 1.76}{6.02} \quad (15)$$

2.1 Examples

1. Determine the PLL jitter requirement for 12-bit 5-GSPS ADC with 53-dBFs SNR for a 4-GHz input signal at –1 dBFs. Assume a 3-dB maximum degradation of SNR and ADC aperture jitter of 50 fs.
   - Solution: using Equation 11 through Equation 15, incorporated in the jitter calculator tool, complete a budget analysis as depicted in Figure 2-1. At 4-GHz input frequency, 1 dB back off from full scale, for 3-dB SNR degradation (1/2 bit ENOB), the maximum allowed total jitter is calculated at 100 fs, and assuming 50-fs aperture jitter, the max clock jitter is 86 fs, or –51 dBc. The plots shows clock jitter requirements versus input frequency.

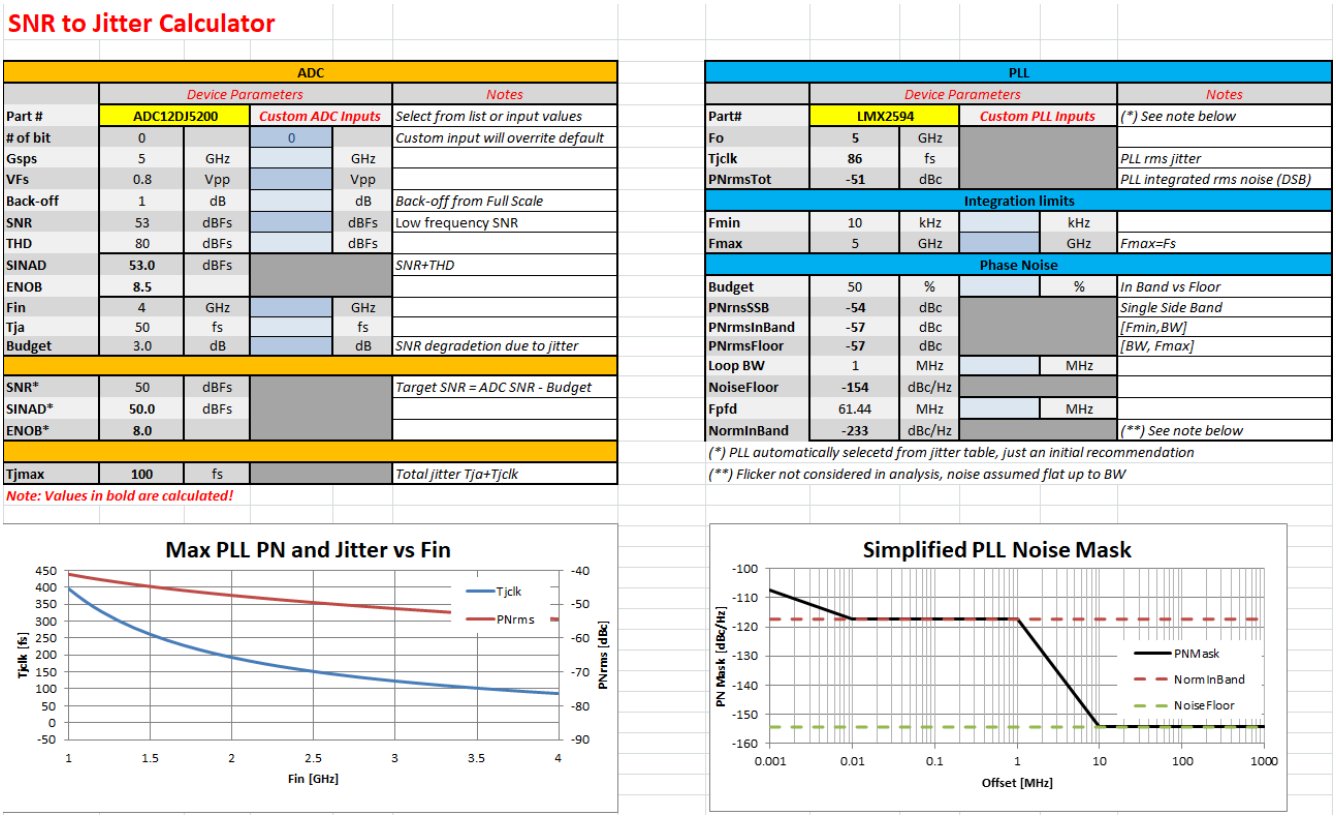

Figure 2-1. Jitter vs Fin Requirements

2. For the ADC in example 2.1, determine SNR and ENOB if the PLL jitter is 100 fs.
   - Solution: similarly to the previous example, use to calculate the SNR of the ADC. The total jitter, including 50 fs of aperture jitter is now 94 fs, which corresponds to an SNR of 51.6 dBFs, and ENOB of 8.3 bit, see Figure 2-2. The plot shows the same parameters as a function of clock jitter.

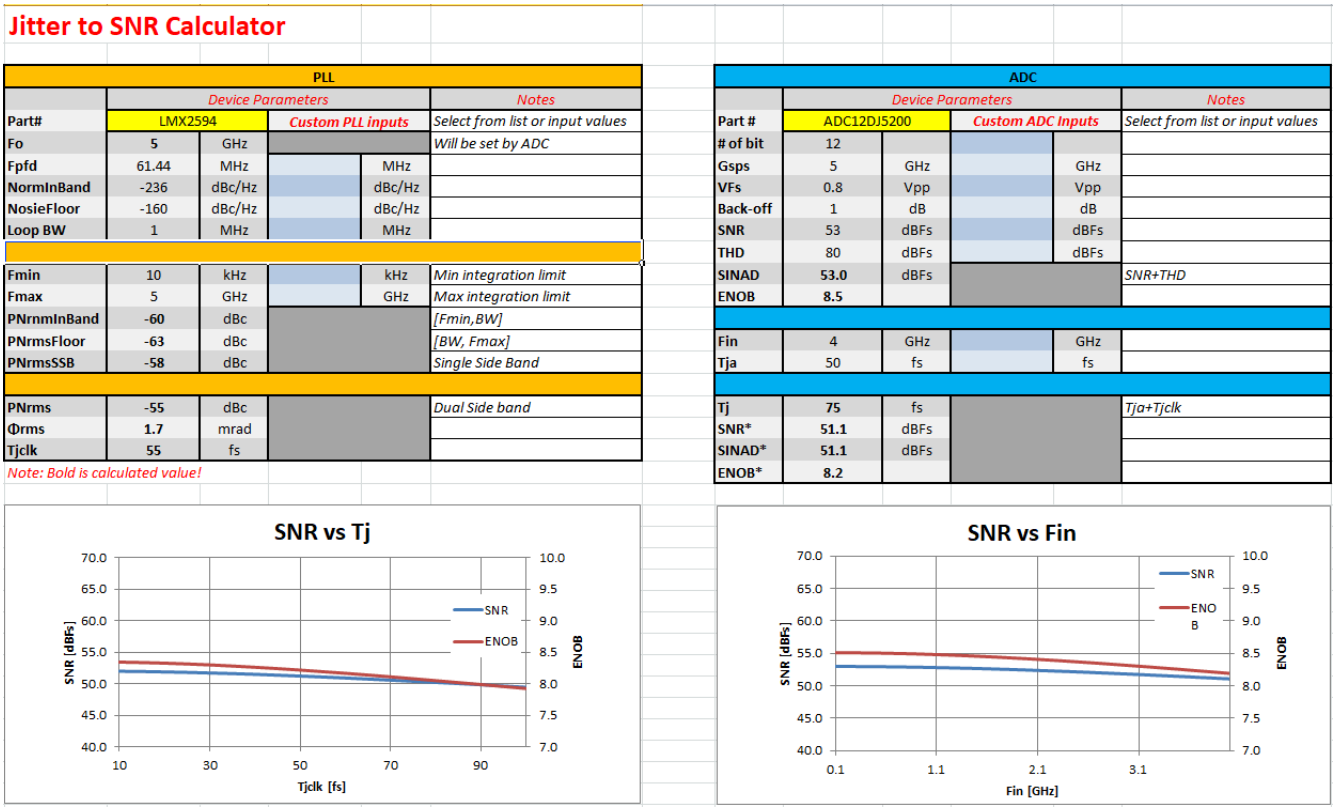

Figure 2-2. SNR and ENOB vs Clock Jitter

3 Simulations and Filter Requirements

The previous two sections described how to calculate phase noise and jitter and the clock jitter impact to the ADC performance, specifically SNR, SINAD, and ENOB. For low data rate ADC, generally speaking, PLL close in noise is dominant, but for new generation Gsps ADC, with sampling frequency now well above 3 GHz, and 10 GHz in the DAC case, PLL noise floor (out of band noise) start becoming more and more important (due to the high limit of integration bandwidth). To minimize the impact of the clock jitter to the ADC SNR, a filter can be added after the PLL. If the signal level is degraded due to the loss of the filter, a low phase noise amplifier can be added after the filter to restore the signal level driving into the ADC. Now try to evaluate the filter bandwidth requirement by first setting up a simulation test bench as Figure 3-1 shows.

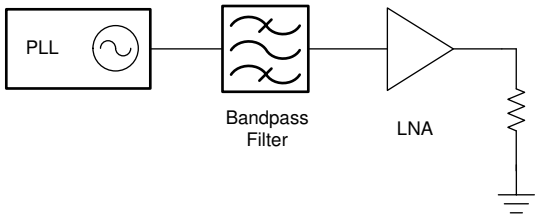

Figure 3-1. Simulation Setup

The phase noise profile of the LMX2594 PLL, as Figure 1-2 shows, is imported and used as the clock source. This is followed by a programmable bandpass filter, and a low noise amplifier. Simulated integrated noise, jitter, and SNR both at the filter and LNA output are shown in Figure 7. For comparison, the plots shows high and low limits respectively due to the PLL with no bandpass filter and when an ultra-low noise signal source like R&S SMA100A or B is used.

Figure 3-2 and Figure 3-3 show the simulation results.

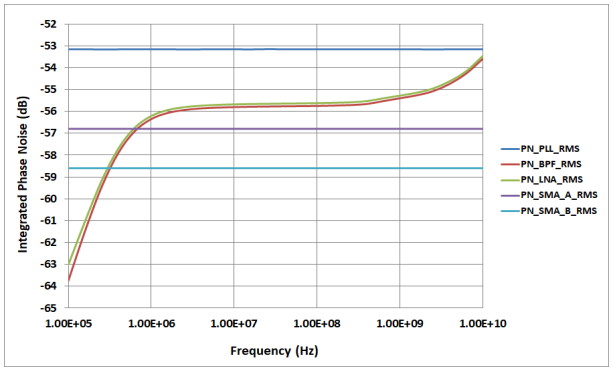

Figure 3-2. Phase Noise vs Frequency

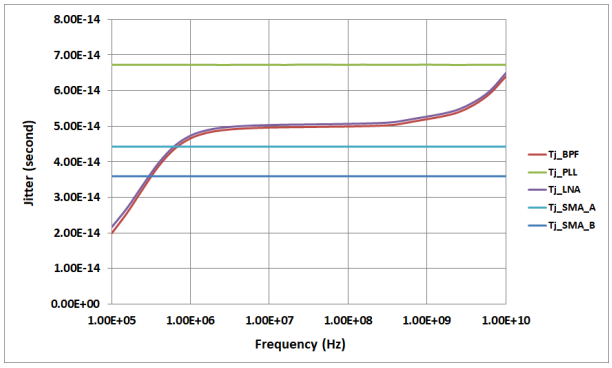

Figure 3-3. Jitter vs Filter Bandwidth

For this analysis we assume a clocking frequency of 5 GHz, and aperture jitter of 50 fsec for the ADC as discussed before. Because the impact of the clock jitter on the ADC is a function of frequency, we report the SNR of ADC at 1-GHz and 4-GHz input frequency. The greater impact at higher input frequency (4 GHz) is clear, with about 2-dB degradation when compared to the signal generator. Also note how the bandpass filter helps improve the SNR, recovering the full 2-dB degradation when the BW is < 300 kHz. However, must point out that this corresponds to a very selective filter, in line with a cavity filter available in the lab, not easily implemented as discrete or SMT on the system board. It is worth noticing that even a more relaxed filter can still improve the SNR more than 1 dB at higher input frequencies. This is very important in wide band or high IF systems.

The plot in Figure 3-4 shows simulated SNR for signal generator, PLL(LMX2594) with no filter, PLL with SMT filter and PLL with cavity filter. For the last two cases, s-parameters provided by vendor have been used in the simulation.

The simulation clearly shows that the highly-selective filter reduces the impact of the PLL jitter to the level of the signal generator typically used for the ADC characterization.

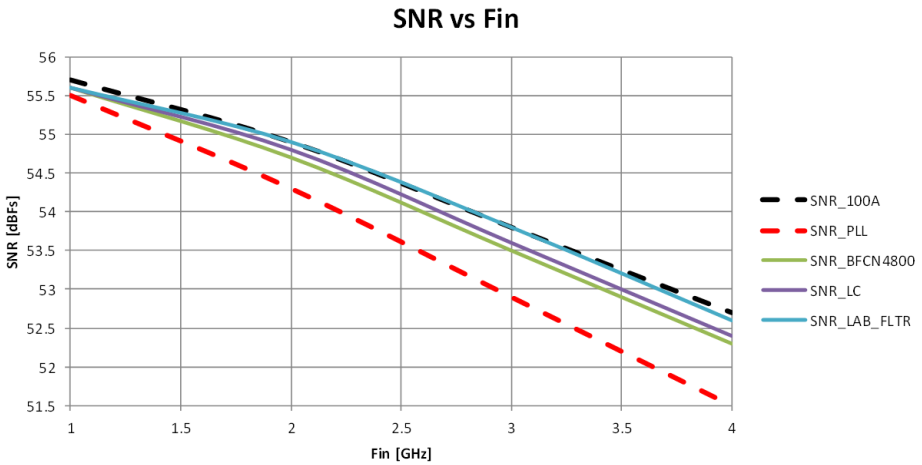

Figure 3-4. Simulated SNR vs Frequency With Different Sources

Figure 3-4 shows the SNR improves from PLL only to SMA100 equivalent as the selectivity of the filter increases from SMT (Mini-Circuit BFCN-4800) to cavity (lab filter).

4 Measurement Setup

To test the theory and simulation results described in the previous section the next step is to do the measurements.

The ADC12DJ5200RFEVM was used to perform the SNR measurement. Figure 4-1 shows the measurement setup. The R&S SMA100A signal generator is used for clocking the ADC12DJ5200RF. The clocking was filtered with a bandpass filter. The next set of measurements were performed with the same setup but the clocking signal was not filtered with the bandpass filter.

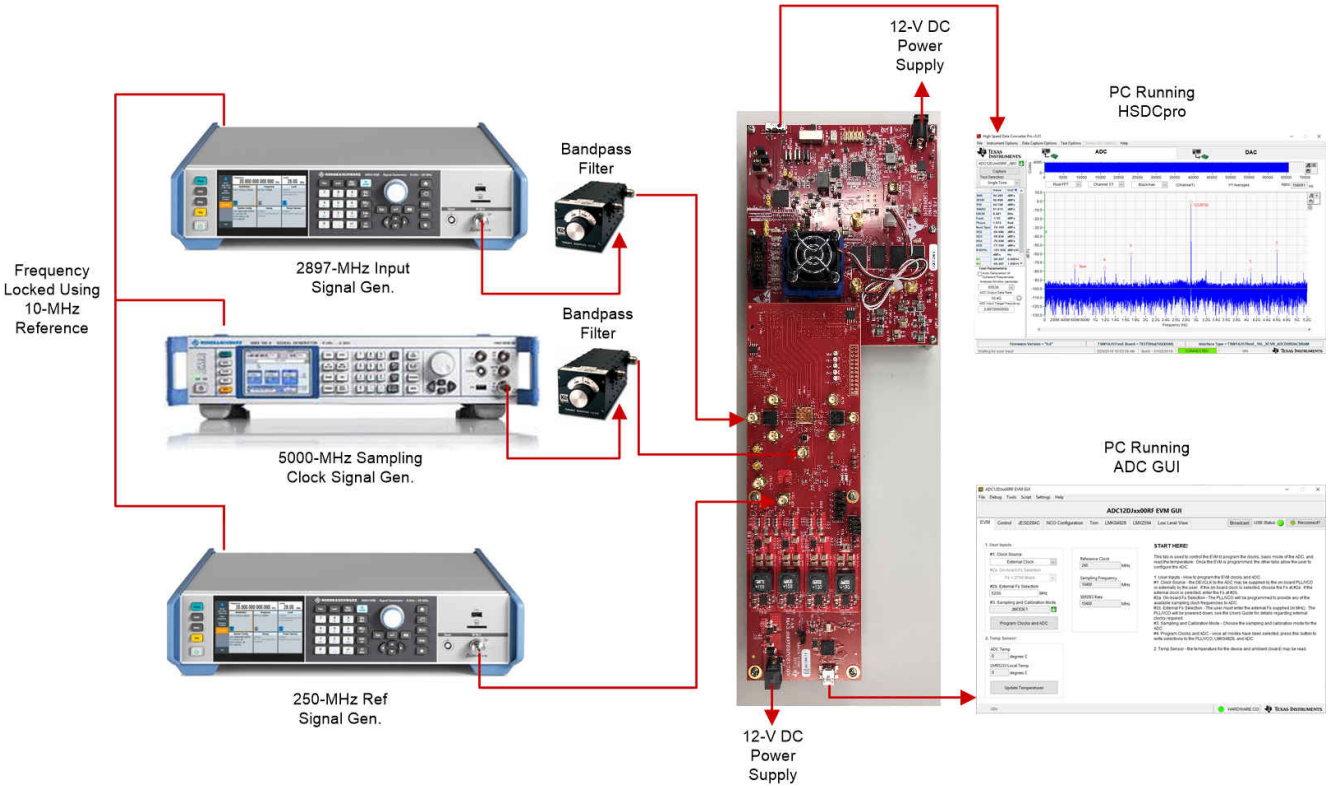

Figure 4-1. SMA100A Signal Generator Used for Clocking the ADC12DJ5200RF With the Bandpass Filter

Figure 4-2 shows the setup where the LMX2594 synthesizer was used to clock the ADC12DJ5200RF. Similar test procedures as described in the previous section were used where the measurements were done with and without the bandpass filter after the LMX2594 device.

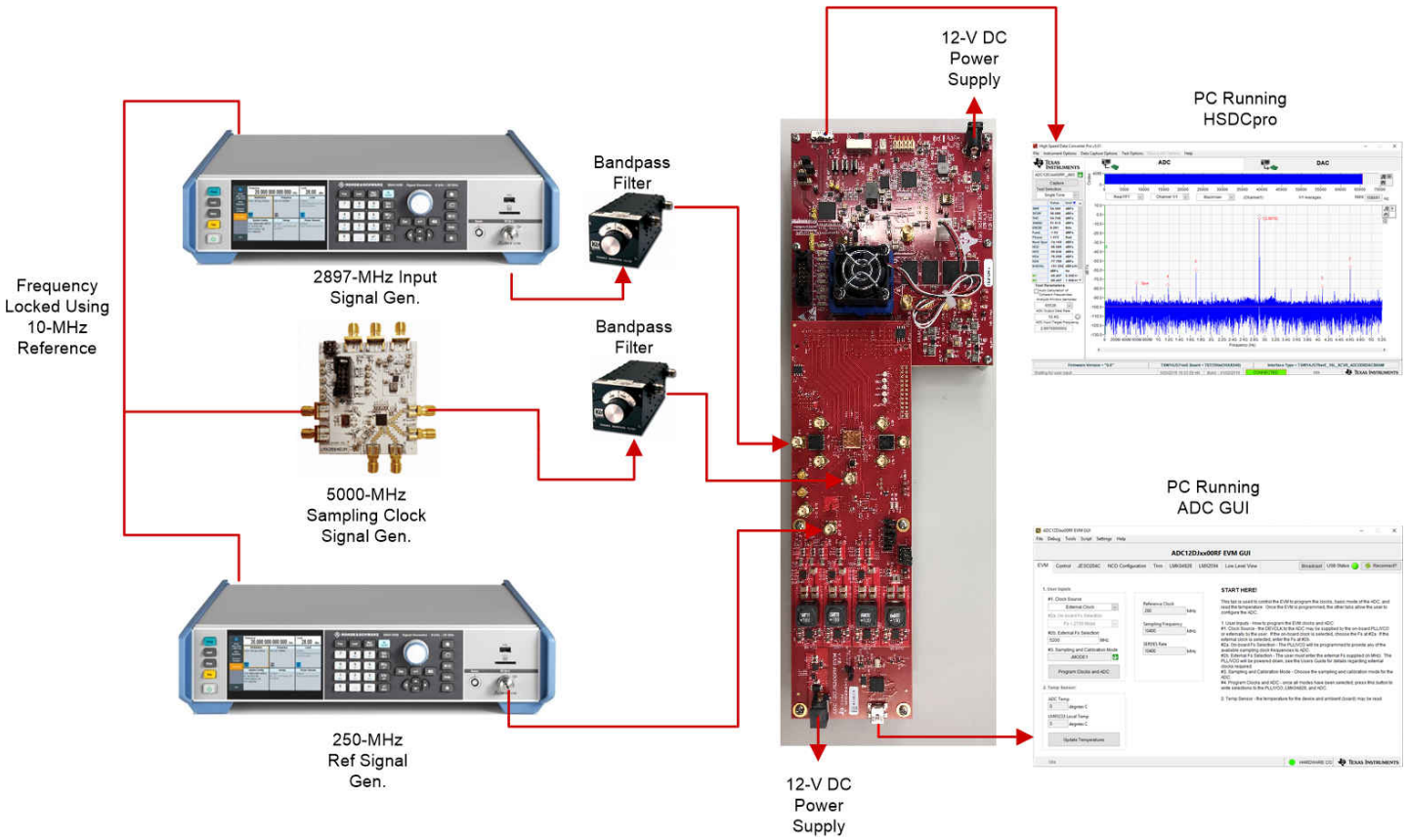

Figure 4-2. LMX2594 Used for Clocking the ADC12DJ5200RF With the Bandpass Filter

For all the measurements, a 5-GHz clock signal was used. The ADC was configured in single channel mode which uses both the rising and falling edge of the clock and the ADC was effectively sampling at 10 GSPS. The different input frequencies (1 GHz, 3 GHz and 4 GHz) were used for the measurements. Since these measurements are performed to show the effects of the phase noise of the clock signal, all the interleaving spurs are excluded from the SNR calculations.

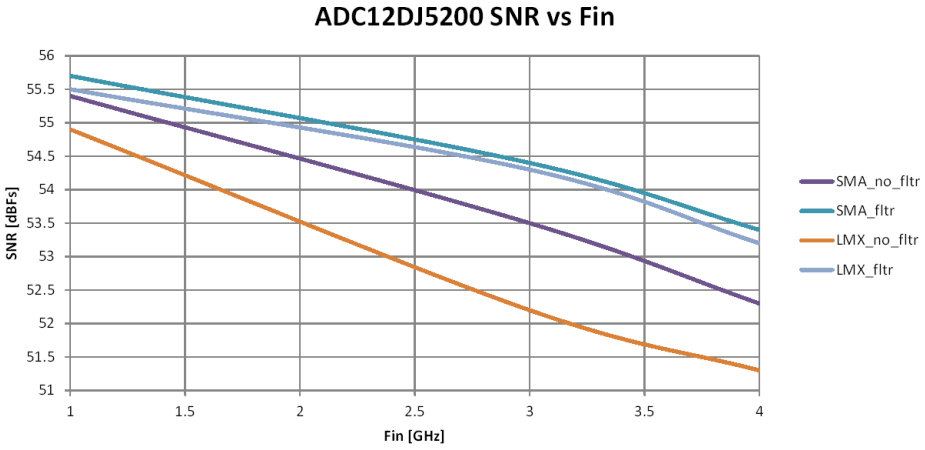

Figure 4-3. Measured SNR vs Fin With and Without Filter

Table 4-1 shows the measured SNR versus Fin without using the bandpass filter at high input frequencies, the LMX shows about a 1-dB worse SNR as compared the SMA100A. But when both the SMA100A and LMX2594 are filtered (bandpass filter) both of the clock sources have the same performance.

Table 4-1. Measured SNR vs Fin with SMA and LMX2594 with and without filter

Input Frequency (GHz)	SNR(dBFs)			
	SMA Unfiltered	SMA Filtered	LMX2594 Unfiltered	LMX2594 Filtered
1	55.4	55.7	54.9	55.5
3	53.5	54.4	52.2	54.3
4	52.3	53.4	51.3	53.2

5 References

1. Texas Instruments, *ADC12DJ5200RF 10.4-GSPS Single-Channel or 5.2-GSPS Dual-Channel 12-bit, RF-Sampling Analog-to-Digital Converter (ADC) Data Sheet*
2. Texas Instruments, *LMX2594 15-GHz Wideband PLLATINUM™ RF Synthesizer With Phase Synchronization and JESD204B Support Data Sheet*
3. Texas Instruments, *Clocking the RF ADC: Should you worry about Jitter or Phase Noise? Analog Applications Journal*
4. Texas Instruments, *Clocking Optimization for RF Sampling Analog-to-Digital Converters Application Report*
5. Texas Instruments, *Clock jitter analyzed in the time domain, Part 1 Analog Applications Journal*
6. *Clock Jitter Effects on Sampling: A Tutorial*
7. Texas Instruments, *Multi-channel JESD204B 15-GHz clocking reference design for DSO, radar and 5G wireless testers reference design*
8. Texas Instruments, *Jitter and SNR Calculator for ADCs*

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265