

# **eAVB Media Clock Synchronization Using CDCE6214-Q1 Clock Generator**

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## **ABSTRACT**

AVB (Audio Video Bridging) protocols have been widely adopted to achieve time and clock synchronization over Ethernet, especially in automotive infotainment systems. [CDCE6214-Q1](#) is a compact and ultra low-power programmable clock generator that supports output frequency tuning with less than 1-ppm step size. With the frequency margining capability, CDCE6214-Q1 is ideal for AVB media clock synchronization. This application report introduces AVB system architecture and explains media clock synchronization design with CDCE6214-Q1.

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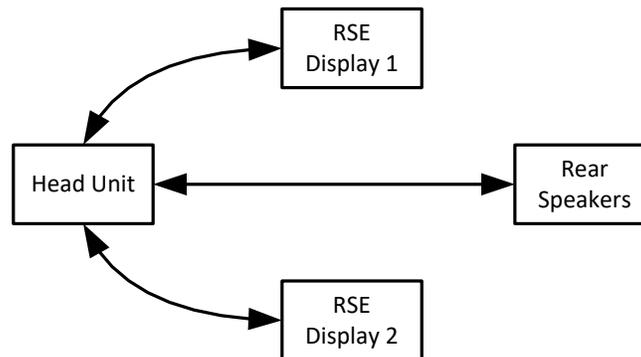
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## 1 Introduction

Modern media systems for automotive infotainment and driver assistance are composed of multiple sensors, cameras, displays, and content players. Point-to-point interconnections with shielded twisted pair or coaxial cables may not be practical for all of the required components. Ethernet is gaining more traction in the automotive audio visual market segment due to its convenience and fast transmission speed; however, standard asynchronous Ethernet networks do not carry clock synchronization information. One of the main goals of AVB protocols is to achieve time and clock synchronization over Ethernet.

Consider the example below where the live or playback audio and video are presented on two RSE (Rear Seat Entertainment) displays and multiple speakers at the same time. Speakers and RSE displays are connected to the Head Unit through Ethernet. For excellent user experience, media content should be lip synchronized, and both audio and video should be distributed to all speakers and displays synchronously.



**Figure 1. Ethernet Time Synchronization in Automotive Infotainment System**

Two types of A/V synchronization are required:

1. The A/V (audio and video) content shall start and stop playing at the same time, which requires a common time reference for multiple events to trigger simultaneously.
2. The media content should be sampled and reconstructed at the same rate for high-fidelity A/V systems.

See [Section 2](#), [Section 3](#) and [Section 4](#) to understand how to achieve the two types of synchronization and how the CDCE6214-Q1 device fits in media clock recovery.

## 2 AVB Protocols and Network Structure

AVB is a family of protocols that include:

1. IEEE 802.1AS for time synchronization. IEEE 802.1AS defines generalized Precision Time Protocol (gPTP) profile based on IEEE 1588.
2. IEEE 802.1Qav for traffic shaping.
3. IEEE 802.1Qat for stream reservation.
4. IEEE 802.1BA that specifies defaults and profiles of AVB components. IEEE 802.1BA is an umbrella standard for IEEE 802.1AS, IEEE 802.1Qav and IEEE 802.1Qat.
5. IEEE 802.1Q that specifies Virtual Bridged Local Area Networks. IEEE 802.1Qav and IEEE 802.1Qat have been incorporated to IEEE 802.1Q.
6. IEEE 1722 Layer 2 A/V transport protocol.

An example AVB system is shown in [Figure 2](#):

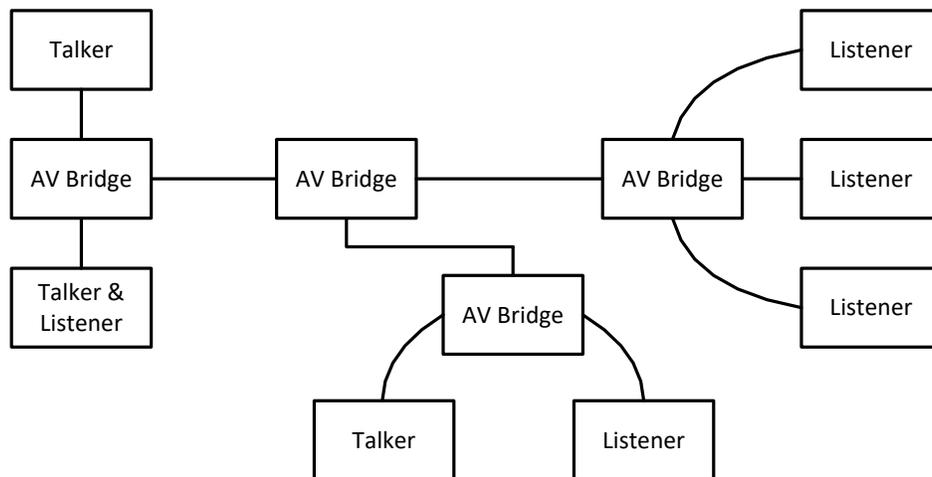


Figure 2. Example High Level AVB Network

An AVB network consists of three types of components:

1. AV Bridges. An AV Bridge is a relay device that conforms to IEEE 802.1BA. It acts as a switch that receives and forwards IEEE 802.1BA compliant data to the destination device.
2. End stations. An end station can be a Talker, Listener, or both. A Talker is an end station that is the source, transmitter or producer of a stream. A Listener is an end station that is the destination, receiver or consumer of a stream.
3. Ethernet LANs (Local Area Network). Individual LANs interconnect the Bridges, Talkers and Listeners.

To understand more about the AVB end stations see [Section 3](#).

### 3 AVB End Station Architecture

A high level system block diagram of an AVB end station (Talker and Listener) with time-sensitive applications is shown below:

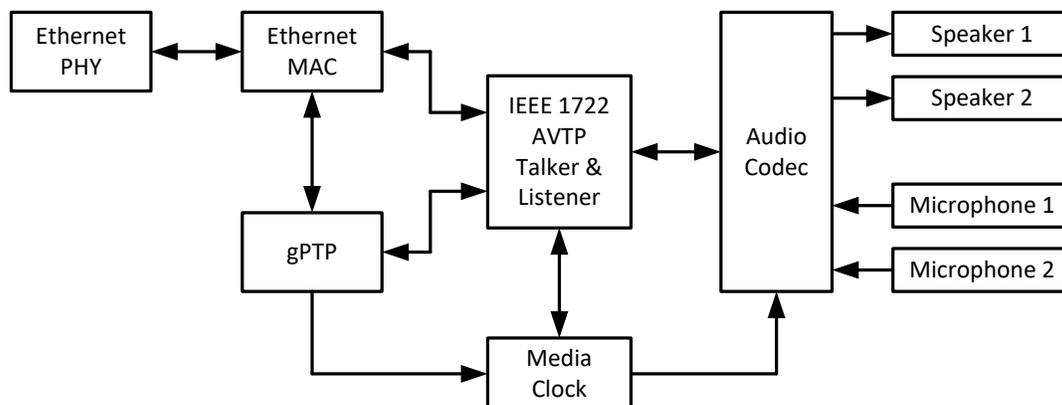


Figure 3. AVB End Station Block Diagram – Talker and Listener

An AVB end station consists of the following components:

- A gPTP (generalized Precision Time Protocol) subsystem provides a common local time reference by exchanging timestamped packets with the Grandmaster clock. A grandmaster clock is the best clock selected to provide a common time reference to all Ethernet nodes. This common time reference, as in time of day, is called *Wall Clock*.
- An AVTP (Audio Video Transport Protocol) Talker or Listener consists of an AVTP Network Interface and AVTP Stream Packetizer or Depacketizer. The AVTP Talker and Listener interconnect time-

sensitive applications across AVB nodes through the Ethernet MAC (Media Access Control) layer. For example, an analog signal collected by a microphone is sampled by the Audio Codec and becomes digital media samples. An AVTP Talker inserts timestamps with a common time reference to the data packets and produces outgoing IEEE 1722 data streams. Similarly, an AVTP Listener interprets an incoming 1722 stream and converts it to digital media samples. The media samples are fed into the Audio Codec to reconstruct the analog signal which is then amplified and played by the speakers.

- A media clock provides the clocking for the Audio Codecs. In other words, the media clock controls the rate at which the Audio Codec samples or restores an analog signal. The Media clock needs to be synchronized between sources and destinations of the media content. For example, if a single audio stream is broadcasted to multiple speakers in different end stations, all the speakers need to reconstruct the audio with exactly the same rate for high quality audio distribution. As another example, if a Listener subscribes to multiple Talkers, media clocks for all Talkers should be synchronized so that the Listener can receive 1722 streams from different sources without need of sample rate conversion.

Details of media clock recovery and synchronization are covered in the next section.

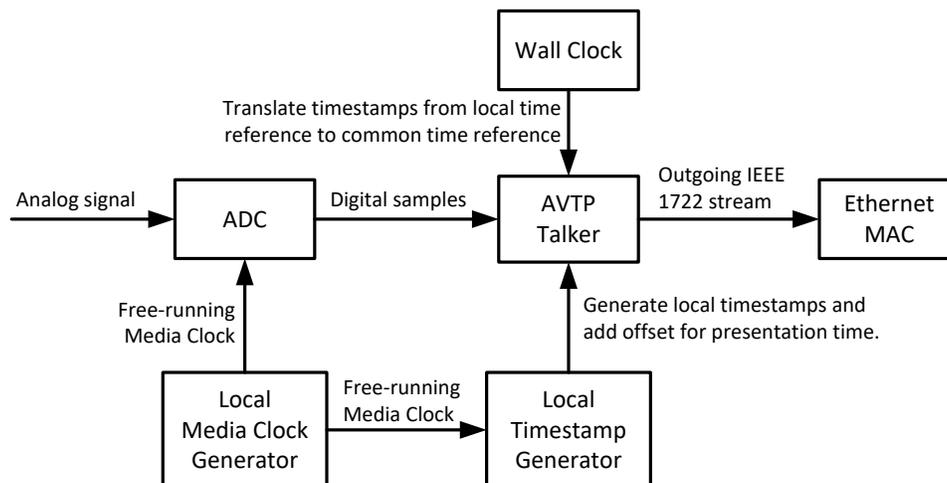
## 4 Talker, Listener, Presentation Time, and Media Clock Synchronization

In this section, the following questions are answered:

1. How to achieve the two types of synchronization.
2. How does the CDCE6214-Q1 device fit in media clock synchronization.

### 4.1 Talker and Presentation Time

A simplified Talker block diagram is shown below:



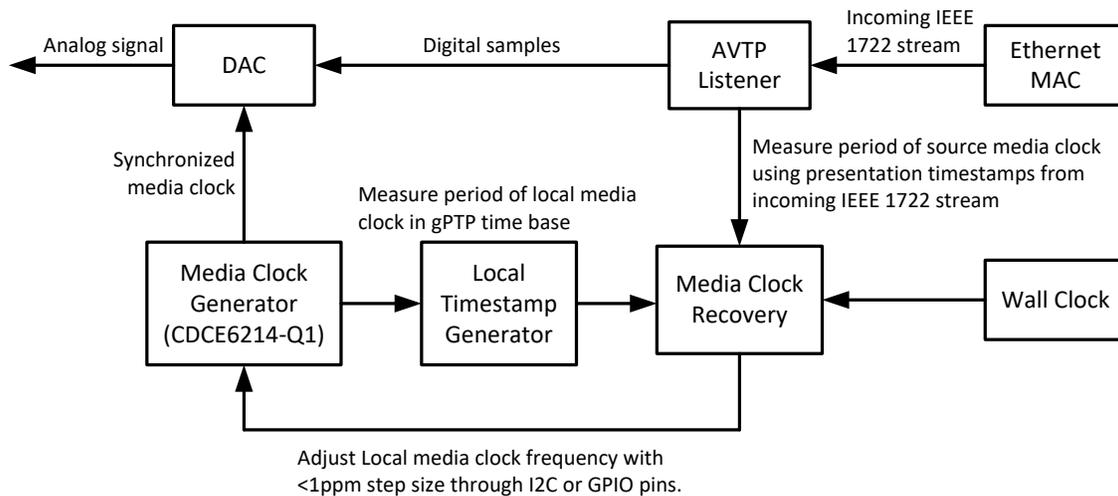
**Figure 4. AVB Talker Simplified Block Diagram**

This diagram explains how the media clock source is embedded into AVTP packets. The media clock's source can be a simple free-running local oscillator, because the media clock does not need to lock to any reference, as long as the frequency of all media clocks in the same domain are synchronized. The media clock goes into a local timestamp generator that generates timestamps every certain number of media clock rising edges. These timestamps are generated based off of a local time reference. The Wall Clock then translates the local time based timestamps to gPTP timestamps. The AVTP Talker adds a fixed offset (typically the maximum delay between the Talker and all Listeners) and generates presentation timestamps.

The AVTP Presentation Time represents the gPTP time at which a designated media sample or event is transferred to the time-sensitive application within each Listener. This enables multiple Listeners to present data at the same time, regardless of the location of the Listeners in the network. The AVTP Presentation Time tells a Listener when to start processing the stream's data (for example, playing media) and is also used to recover the stream's media clock. To understand how to use Presentation time to recover the stream's media clock see [Section 4.2](#).

## 4.2 Listener and Media Clock Synchronization

A simplified Listener block diagram is shown below:



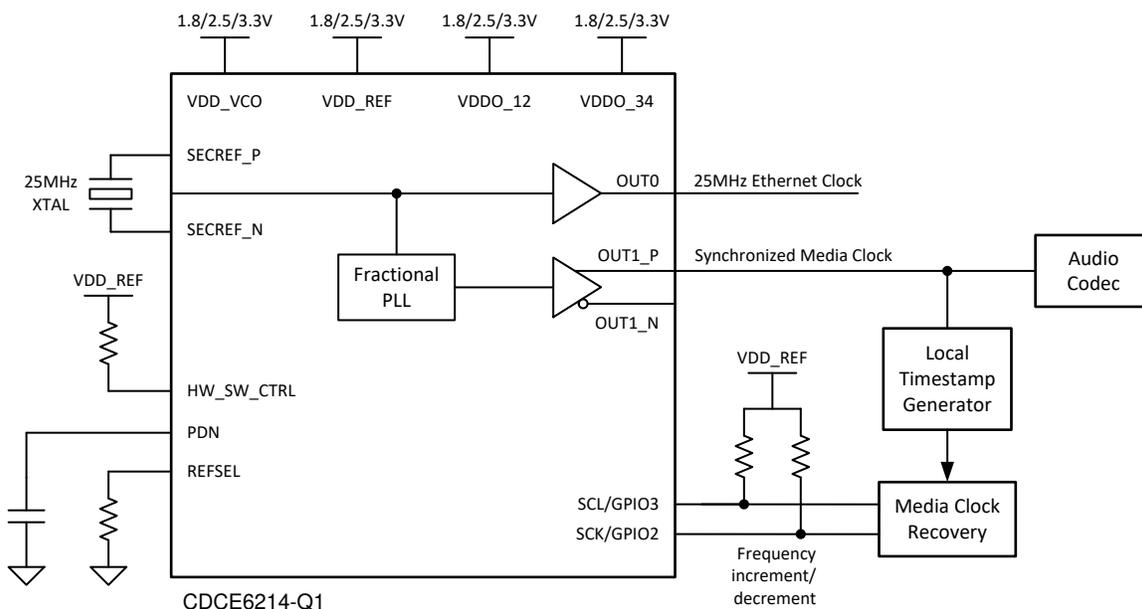
**Figure 5. AVB Listener Simplified Block Diagram**

This diagram explains how a Listener extracts presentation timestamps and recovers the source media clock from incoming 1722 streams generated by a Talker. The period of the source media clock in the gPTP time base can be estimated by the time difference between two presentation timestamps divided by the number of samples in between. Continually performing this calculation and applying appropriate filtering techniques yields an accurate measurement of the source's media clock period.

Similarly, the local media clock generator (CDCE6214-Q1) output can be timestamped with local time base which is then translated to gPTP time base, and its period can also be accurately measured. After comparing the two clock periods, the Media Clock Recovery module continually generates I2C/GPIO commands to increment or decrement output frequency of the CDCE6214-Q1 device so that the local media clock is synchronized to the source media clock.

## 5 Reference CDCE6214-Q1 Schematic and Programming Guide

A simplified CDCE6214-Q1 schematic is shown below:



**Figure 6. AVB Clocking Schematic**

CDCE6214-Q1 has integrated crystal driver circuit, so only a simple crystal resonator is needed at the input. The XTAL (crystal) selection and programming guide can be found at [CDCE6214-Q1 Crystal-Based Oscillator Design](#). The media clock can be generated out of OUT1\_P. OUT0 bypasses PLL and produces buffered output from the crystal input. This 25-MHz output can be used to clock Ethernet. The frequency increment and decrement commands coming from media clock recovery module is fed back to the CDCE6214-Q1 device through the I<sup>2</sup>C (it can also be fed through the GPIO pin control)

The frequency increment and decrement step size can be set by register R43[15:0] `FREQ_INC_DEC_DELTA`. The VCO (Voltage Controlled Oscillator) frequency step size is  $PFD\_FREQ / PLL\_DEN \times FREQ\_INC\_DEC\_DELTA$ , where `PFD_FREQ` is phase frequency detector frequency and `PLL_DEN` is the denominator of PLL fractional divider. The output frequency step size is VCO frequency step size divided by output divider. An example calculation can be found in [Table 1](#). Alternatively, the calculation can be done in [TicsPro](#).

**Table 1. Computing Divider Settings in DCO Mode**

PARAMETERS	VALUE (EXAMPLE)	DESCRIPTION
Input PFD Frequency ( $F_{PFD}$ )	25 MHz	Set according to $F_{PFD}$ .
Expected VCO Frequency ( $F_{VCO}$ )	2457.6 MHz	$F_{VCO}$ is set within the operating VCO range of 2335 MHz - 2625 MHz. $F_{VCO}$ is selected such that PSA/PSB/Output Divider is Integer.
Expected Output Frequency ( $F_{OUT}$ )	24.576 MHz	$PSA = 4, IOD = 25, F_{VCO} = PSA \times IOD \times F_{OUT}$ .
Expected step size (in ppm) ( $F_{step}$ )	0.1	Every rising edge of <code>FREQ_INC/FREQ_DEC</code> would change the output by this step size.
N-divider Value (N)	98	$INT(F_{VCO}/F_{PFD})$
Minimum Numerator value to meet 0ppb accuracy (Num)	76	These values are computed to meet accuracy requirement at output. Should be less than $2^{24}$ .
Minimum Denominator to meet 0ppb accuracy (Den)	250	
Minimum Denominator value to meet ppm step size ( $F_{DEN,min}$ )	101725.26	$1/(F_{step} \times 1e6) / (F_{VCO}/F_{PFD})$
Final Denominator value ( $F_{DEN,final}$ )	500000	$F_{DEN,final}$ should be greater than $F_{DEN,min}$ and less than $2^{24}$ . $F_{DEN,final}$ and $F_{NUM,final}$ should be integer multiple of Den and Num respectively. $F_{DEN,final}/Den = F_{NUM,final}/Num$
Final Numerator value ( $F_{NUM,final}$ )	152000	
Increment/ Decrement step size	5	This value should be less than $2^{16}-1$ . $F_{DEN,final}$ should be closest integer multiple of $F_{DEN,min}$ .

Once the step size is set, DCO mode is enabled (`R3[3] FREQ_INC_DEC_EN = 1`) and DCO register control is enabled (`R3[4] FREQ_INC_DEC_REG_MODE = 1`), the frequency can be incremented or decremented by toggling `R3[5] FREQ_INC_REG` and `R3[6] FREQ_DEC_REG`

## 6 Summary

This application note answers the two frequently asked questions on AVB synchronization:

- Multiple speakers attached to different Listeners can start and stop playing at precisely the same time by having the presentation timestamps added to the 1722 data packets. All samples are specified to release to AVTP stream depacketizer buffers at the scheduled presentation time.
- Multiple Talkers and Listeners can achieve sampling rate synchronization by comparing the local and source media clock period and fine tuning the local media clock frequency.

As described in [Section 5](#), CDCE6214-Q1 is a simple but efficient frequency adjustable PLL that can be used for media clock generation and synchronization. Besides, CDCE6214-Q1 has less than 2.1 ps integrated fractional jitter. It also provides features such as output slew rate control that can slow down the output edge rate and meet EMI requirements for the automotive industry.

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